



## 2.5V configuration by FlashLink

Ver1.0 Jan/21/2004

This application note describes how use FlashLink with Virtex2Pro/Spartan3 (from Xilinx) that have 2.5V configuration pins without 3.3V tolerant.

### [Table of Contents]

1: 2.5V Configuration pins .....	2
2: Limit High level to 2.5V .....	3
3: Conclusion .....	4

## 1: 2.5V Configuration pins

All of the configuration pins of FlashLink operates under 3.3V-level environment. But configuration pins of some FPGA such as Virtex2Pro/Spartan3 from Xilinx must be configured by 2.5V-level environment. In this case, user should build such configuration environment that FlashLink side is 3.3V-level and FPGA side is 2.5V-level.

FPGA Configuration pins of Virtex2Pro/Spartan3 connected to FlashLink is described in table -1 below.

#	Pin Name	Power Source	Power Voltage	Remarks
1	PROG_B	VCCAUX	2.5V-fixed	Not 3.3V tolerant
2	CCLK	VCCAUX	2.5V-fixed	Not 3.3V tolerant
3	DONE	VCCAUX	2.5V-fixed	Not 3.3V tolerant
4	DIN	VCCO_4	User defined	Not 3.3V tolerant if VCCO_4 is 2.5V
5	INIT_B	VCCO_4	User defined	Not 3.3V tolerant if VCCO_4 is 2.5V

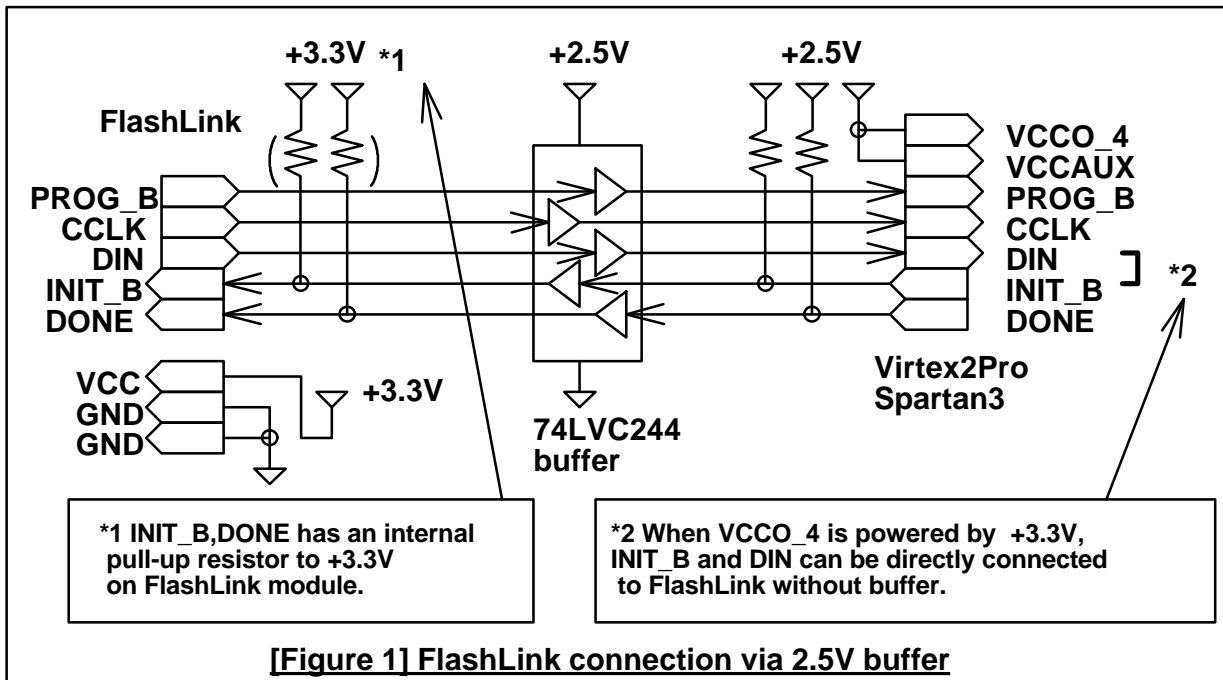
[Table 1] Configuration pins of Virtex2Pro/Spartan3

DIN and INIT\_B configuration pin depends on VCCO supply voltage of Bank 4. When 3.3V is supplied to VCCO\_4, DIN and INIT\_B can be directly connected from FlashLink to FPGA because these pins are 3.3V-tolerant at FPGA side. But when 2.5V is supplied to VCCO\_4, care must be taken that these pins are operated under 2.5V-level environment at maximum as well as PROG\_B, CCLK, and DONE.

## 2: Limit High level to 2.5V

The easiest way is to insert 74LVC244 buffer powered by 2.5V between FlashLink and FPGA. 74LVC is 3.3V-tolerant. This 74LVC244 buffer can isolate between FlashLink of 3.3V power domain and FPGA of 2.5V power domain, and can guarantee that voltage of FPGA configuration pins is 2.5V at maximum.

The connection schematic of Virtex2Pro/Spartan3 via 2.5V buffer is shown figure 1 below.



PROG\_B, CCLK, and DIN output from FlashLink can be limit to high level voltage of 2.5V via 74LVC244 buffer at the FPGA pin. 74LVC244 can accept 3.3V input even when this device is powered by 2.5V.

Also, INIT\_B and DONE pin of FPGA side can be guaranteed to 2.5V at maximum. In this case, high level noise margin of INIT\_B and DONE pin at FlashLink side is decreased, but the internal pull-up resistor in FlashLink can compensate this margin. (Pull-up resistor to +3.3V for INIT\_B and DONE signal is mounted on FlashLink module.)

74LVC244 buffer guarantees its operation when VCC power supply is over 1.65V. FlashLink starts power-up configuration about 400msec after power supply is stabled. Thus, at this time, 74LVC244 is already powered sufficient supply voltage for operation. Circuit of figure-1 operates normally under the power-up transition without problem.



### **3: Conclusion**

FlashLink can be applied to the FPGA that configuration pins are not 3.3V tolerant such as Virtex2Pro/Spartan3 by 74LVC244 buffer insertion powered by 2.5V.

© 2004 Design Gateway Co.,Ltd.