

## FlashLink Type-B DataSheet

Ver5.0 Oct/25/2002

● Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	-0.5	+4.6	V
Tstg	Storage temperature	-55	+125	Celsius
Topr	Operating temperature	-20	+85	Celsius
Vin	DC input voltage	-2.0	+5.75	V
Iout	DC output current, per pin	-25	+25	mA

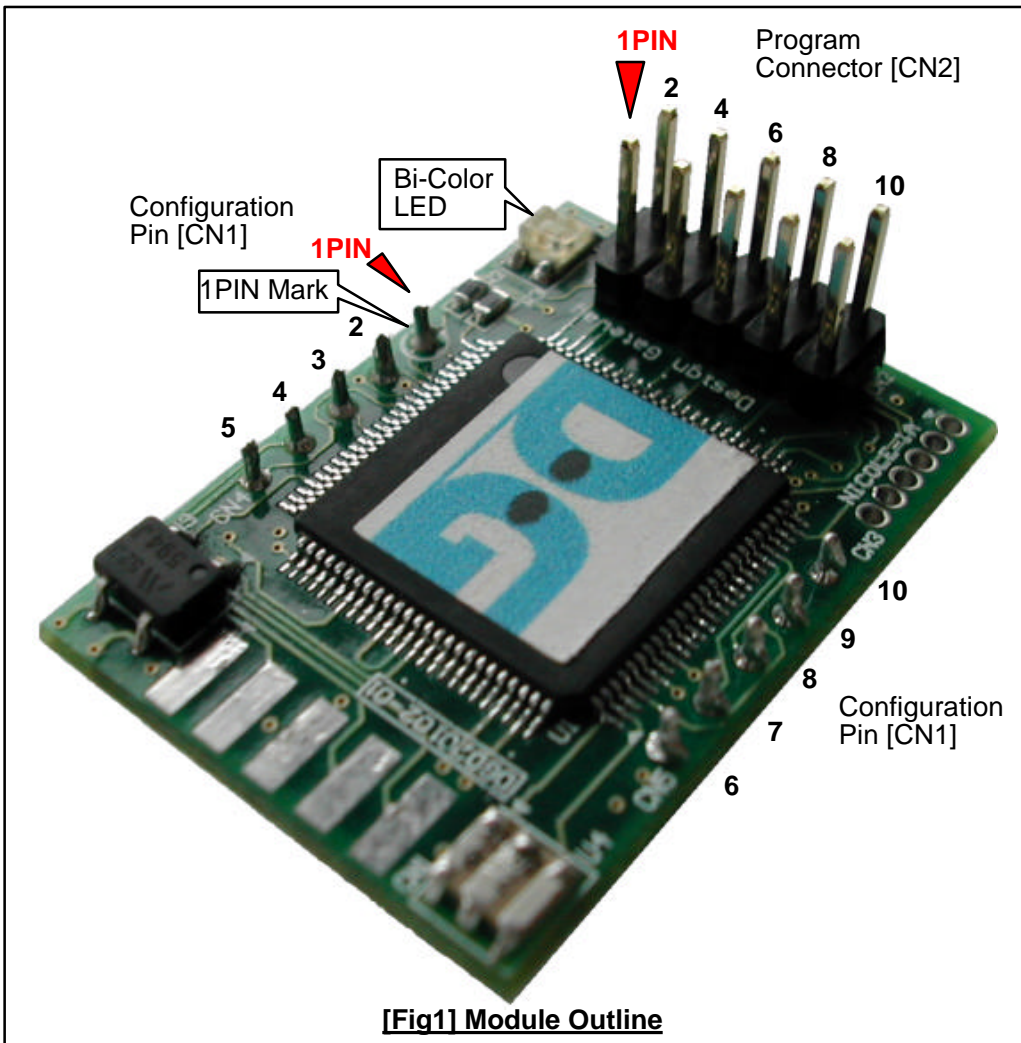
[Table1] Absolute Maximum Ratings

● Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	+3.0	+3.6	V
Topr	Operating temperature	0	+70	Celsius
Vih	High level input voltage	1.7	+5.25	V
Vil	Low level input voltage	-0.5	+0.8	V
Voh	High level output voltage	+2.4	Vcc	V
Vol	Low level output voltage	0	+0.7	V

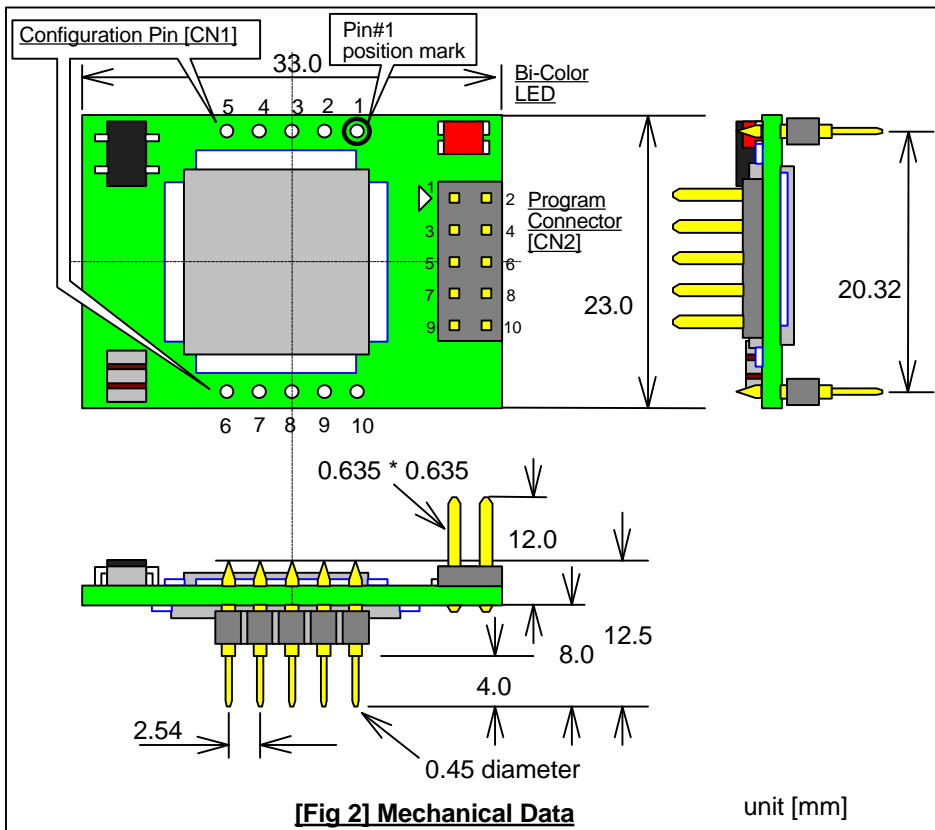
[Table2] Recommended Operating Conditions

● Module Outline

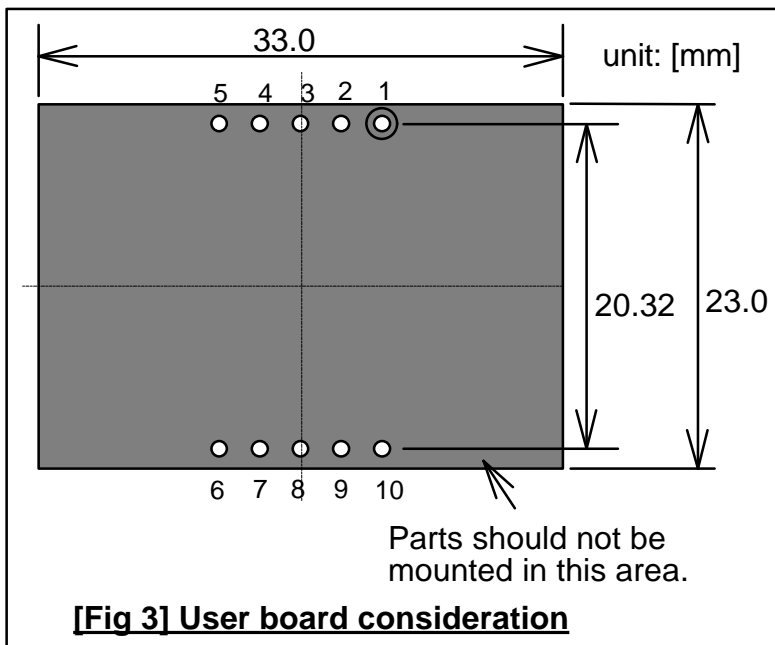


- [CN1] is a DIP pin for configuration signal between user's board and FlashLink module.  
Connect CN1 with DIP pattern of Passive-Serial signal for Altera or Slave-Serial signal for Xilinx.
- [CN2] is a program connector for communication signal between Host-PC and FlashLink module.  
Connect CN2 with ByteBlasterMV or ParallelCable3 when download data from Host-PC to FlashLink.
- [Bi-Color LED] displays a configuration status or a host communication status.

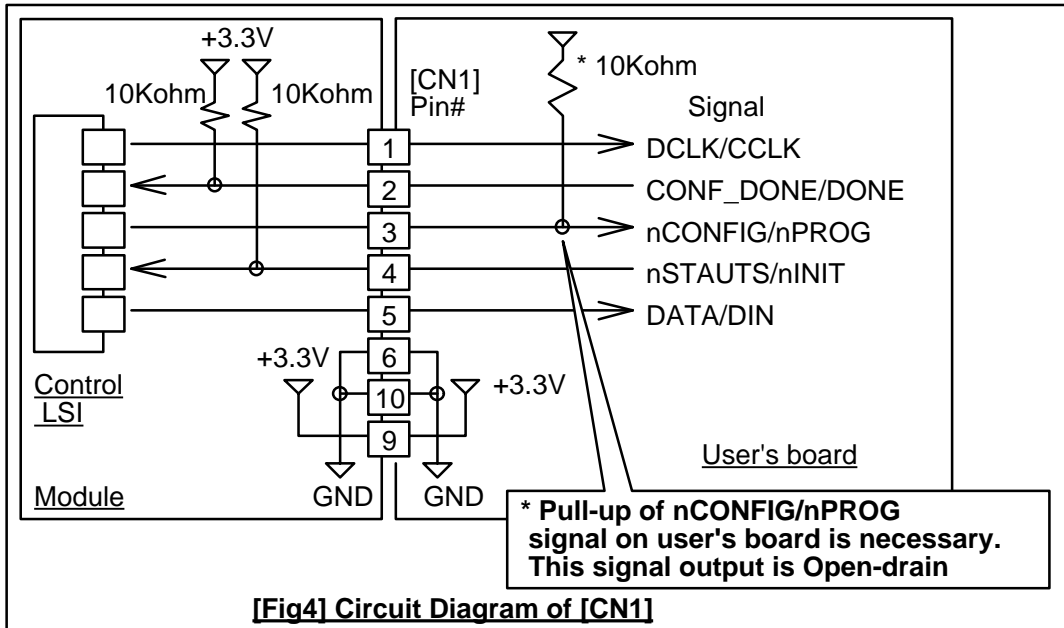
● Mechanical Data



● User board consideration



● Circuit Diagram of CN1

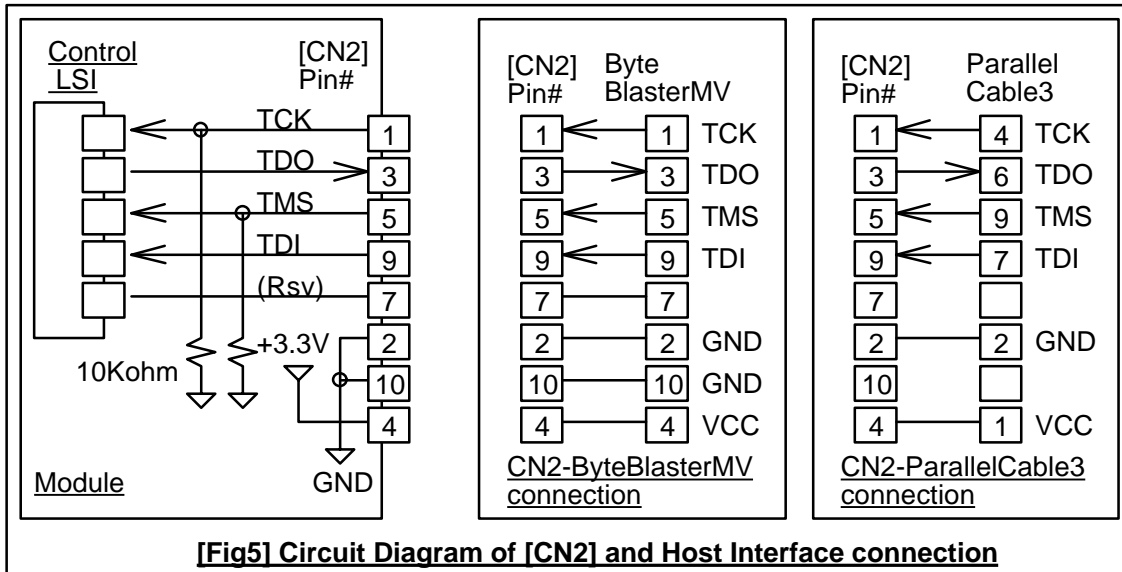


● Signal Description of CN1

Pin#	Signal	I/O	Logic	Description
1	DCLK /CCLK	OUT	Positive	Configuration Clock. Connect DCLK of Altera-FPGA. Connect CCLK of Xilinx-FPGA.
2	CONF_DONE /DONE	IN	Positive	Configuration done (finish) status. Connect CONF_DONE from Altera-FPGA. Connect DONE from Xilinx-FPGA. 10Kohm internal pull-up to +3.3V.
3	nCONFIG /nPROG	OUT	Negative	Configuration Initialize signal. This output pin is open-drain. Pull-up resistor is required on the user's board. Connect nCONFIG of Altera-FPGA. Connect nPROG of Xilinx-FPGA.
4	nSTATUS /nINIT	IN	Negative	Configuration Error status. Connect nSTATUS from Altera-FPGA. Connect nINIT from Xilinx-FPGA. 10Kohm internal pull-up to +3.3V.
5	DATA /DIN	OUT	Positive	Configuration Serial Data (Passive-Serial mode) Connect DATA of Altera-FPGA Connect DIN of Xilinx-FPGA.
6	GND	Power		Signal Ground
7	(No Connect)			
8	(No Connect)			
9	+3.3V	Power		Power Supply. +3.3V (+10% / -10%).
10	GND	Power		Signal Ground.

[Table3] Signal Description of CN1

● Circuit Diagram of [CN2]



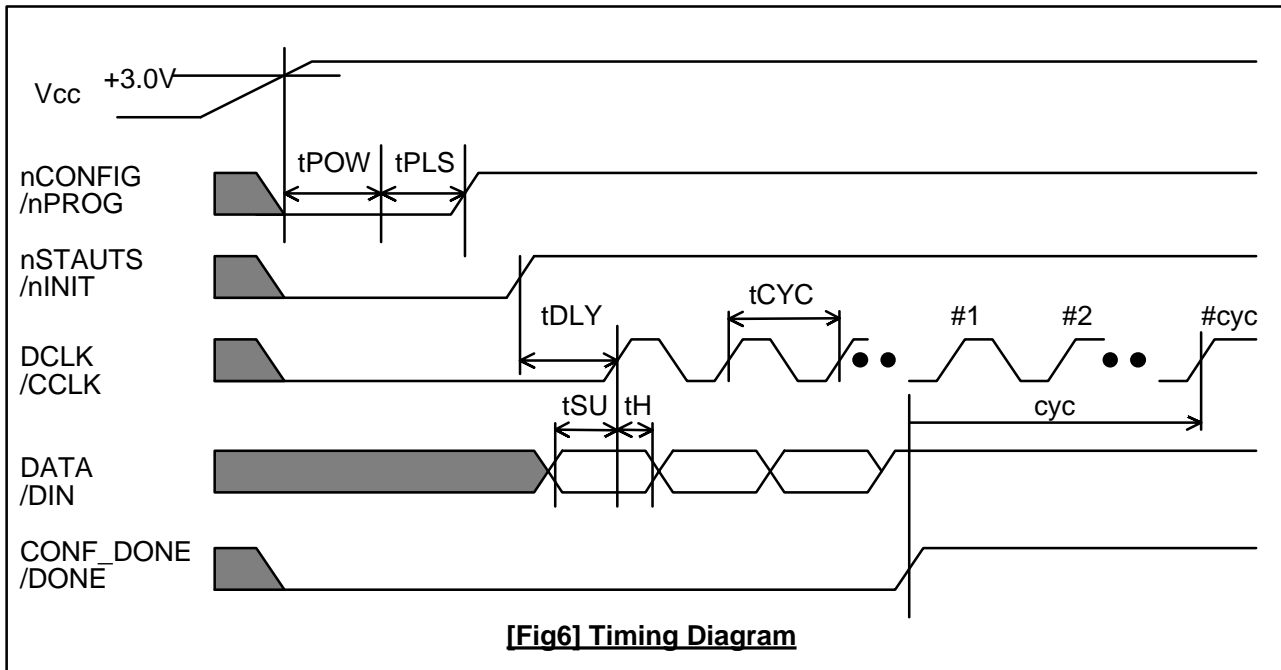
● Though each signal is labeled same name as Jtag, all signals are not compliant with Jtag standard.

● Signal Description of CN2

Pin#	Signal	I/O	Description
1	TCK	IN	Communication signal from Host-PC to FlashLink. Connect 1pin of ByteBlasterMV or 4pin of ParallelCable3. This signal is internally pulled-down with 10Kohm.
2	GND	Power	Signal Ground. Connect 2pin of ByteBlasterMV or 2pin of ParallelCable3.
3	TDO	OUT	Communication signal from FlashLink to Host-PC. Connect 3pin of ByteBlasterMV or 6pin of ParallelCable3.
4	+3.3V	Power	Power Supply. Connect 4pin of ByteBlasterMV or 1pin of ParallelCable3.
5	TMS	IN	Communication signal from Host-PC to FlashLink. Connect 5pin of ByteBlasterMV or 9pin of ParallelCable3. This signal is internally pulled-down with 10Kohm.
6	(No Connect)		
7	(Rsv)	OUT	Reserved signal. This signal is not used for communication. Connect 7pin of ByteBlasterMV
8	(No Connect)		
9	TDI	IN	Communication signal from Host-PC to FlashLink. Connect 9pin of ByteBlasterMV or 7pin of ParallelCable3.
10	GND	Power	Signal Ground. Connect 2pin of ByteBlasterMV.

[Table4] Signal Description of CN2

● Timing Characteristics



[Fig6] Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
tPOW	Power-On (over +3.0V) to configuration start	240	400	600	ms
tPLS	nCONFIG/nPROG low pulse width	8	16		us
tDLY	nSTATUS/nINIT high release to 1st data	8	16		us
tSU	Setup time of configuration data		31.25		ns
tH	Hold time of configuration data		31.25		ns
tCYC	Configuration clock cycle time		62.5		ns
cyc	DCLK/CCLK cycle count after configuration	136	256		(count)

[Table5] Timing Characteristics

(Note: Timing Characteristics are tentative and might be changed without notice.)