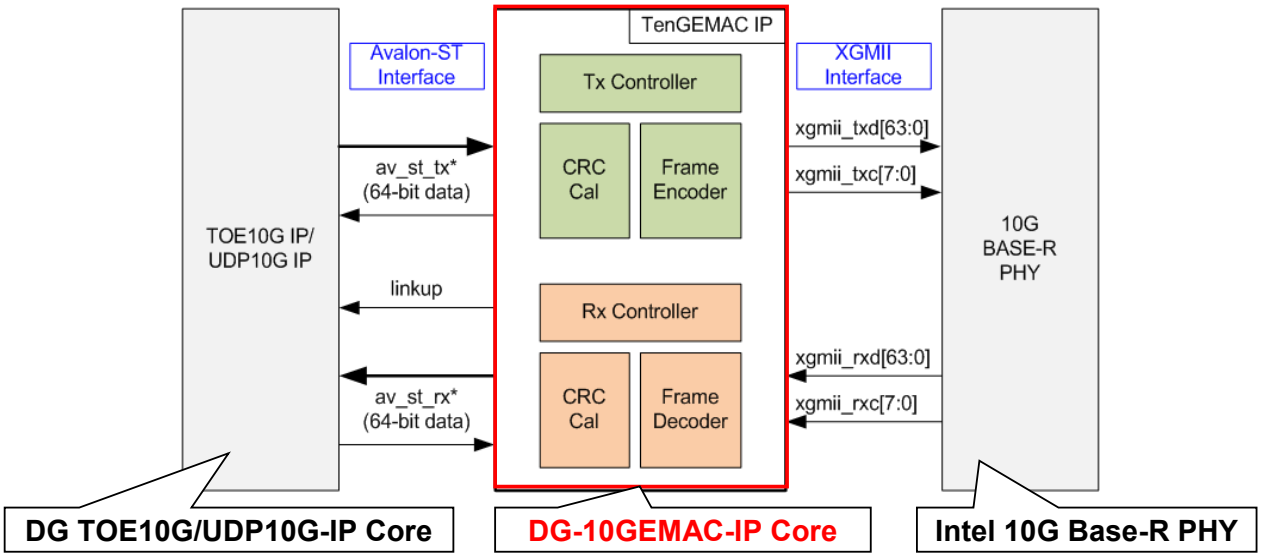
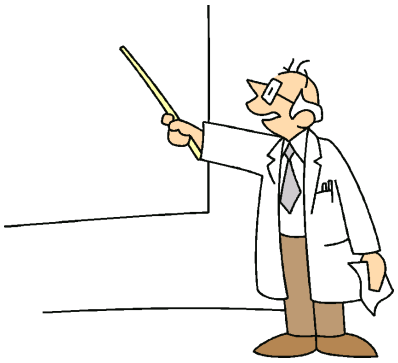
- 10GEMAC inserted between DG IP Core and 10G PHY.



DG-10GEMAC-IP Core Block Diagram

Advantage of DG-10GEMAC-IP Core

- Dedicated MAC IP Core for TOE10G-IP/UDP10G-IP.
- Fully interface compatible with Intel 10GbEMAC.
- Super low-latency, Tx=19.2nsec, Rx=44.8nsec.
- Minimized resource usage, ½ of Intel MAC Core.
- Very low price, 1/5 of Intel MAC Core.



MAC function and Interface

- Provided MAC function
  - Implement necessary MAC feature for DG IP Core.
  - FCS (CRC-32) calculation.
  - Preamble, SFD, and FCS insertion to Tx packet.
  - SFD detection and FCS check from Rx packet.
- Interface
  - PHY side interface is 64bit XGMII (156.25MHz).
  - Controller side interface is Avalon-ST.
    (Fully interface compatible with Intel 10GbEMAC)

DG-10GEMAC-IP Core Advantage 1

- **Dedicated MAC core for TOE10G-IP/UDP10G-IP**
  - Reference design using real Intel board available with combination of TOE10G-IP or UDP10G-IP Core.
  - Fully compatible with Intel 10GbEMAC.
    (Can directly swap with Intel 10GbEMAC.)
  - Very low cost with necessary feature only for DG IP Core.

DG-10GEMAC-IP Core Advantage 2

- **Super low-latency**
  - Optimized by limitation to the combination with DG IP Core.
  - Tx latency is ¼ of Intel MAC Core.
  - Rx latency is ½ of Intel MAC Core.

	Tx latency	Rx latency
Intel 10GbEMAC	76.8ns (12clk)	83.2ns (13clk)
DG-10GEMAC-IP	19.2ns (3clk)	44.8ns (7clk)

10GEMAC latency comparison (clk freq.=156.25MHz)

DG-10GEMAC-IP Core Advantage 3

- **Minimum resource usage**
  - **Drastically reduce resource consumption compared with Intel MAC by omitting MAC function that is not used in DG IP Core.**

	ALMs	Registers	Block Memory
Intel 10GbEMAC	1617	3015	2320bit
DG-10GEMAC-IP	1362	1259	0bit

10GbEMAC resource usage comparison (Arria10GX)

Cautions of DG-10GEMAC-IP Core

- **Use only with 10GbE Core from DesignGateway**
  - **Cannot connect with 3rd party network IP Core.**
- **Some restrictions**
  - **Not provide zero-padding insertion or removal.**
    (Needs to insert/remove zero-padding at user circuit if necessary.)
  - **Top byte of Rx packet must position to byte lane0 or 4.**
    (It is not the problem in normal use)

Conclusion

- **Best match with TOE10G-IP/UDP10G-IP Core**
  - **Minimum latency, resource usage, and cost.**
  - **Maximum performance**
  - **Can directly swap with Intel MAC core**
    （Immediately can swap when Intel EMAC feature become necessary.）
- **Reference design for real operation available**
  - **Quartus Project for Intel evaluation board**
  - **Can check real performance**

For more detail

- **Detailed documents available on the web site.**
  - **TOE10G-IP: https://dgway.com/TOE10G-IP_A_E.html**
  - **UDP10G-IP: https://dgway.com/UDP10G-IP_A_E.html**
- **Contact**
  - **Design Gateway Co,. Ltd.**
  - **E-mail : ip-sales@design-gateway.com**
  - **FAX : +66-2-261-2290**

Revision History

Rev.	Date	Description
1.0E	2-Jul-2019	English version initial release