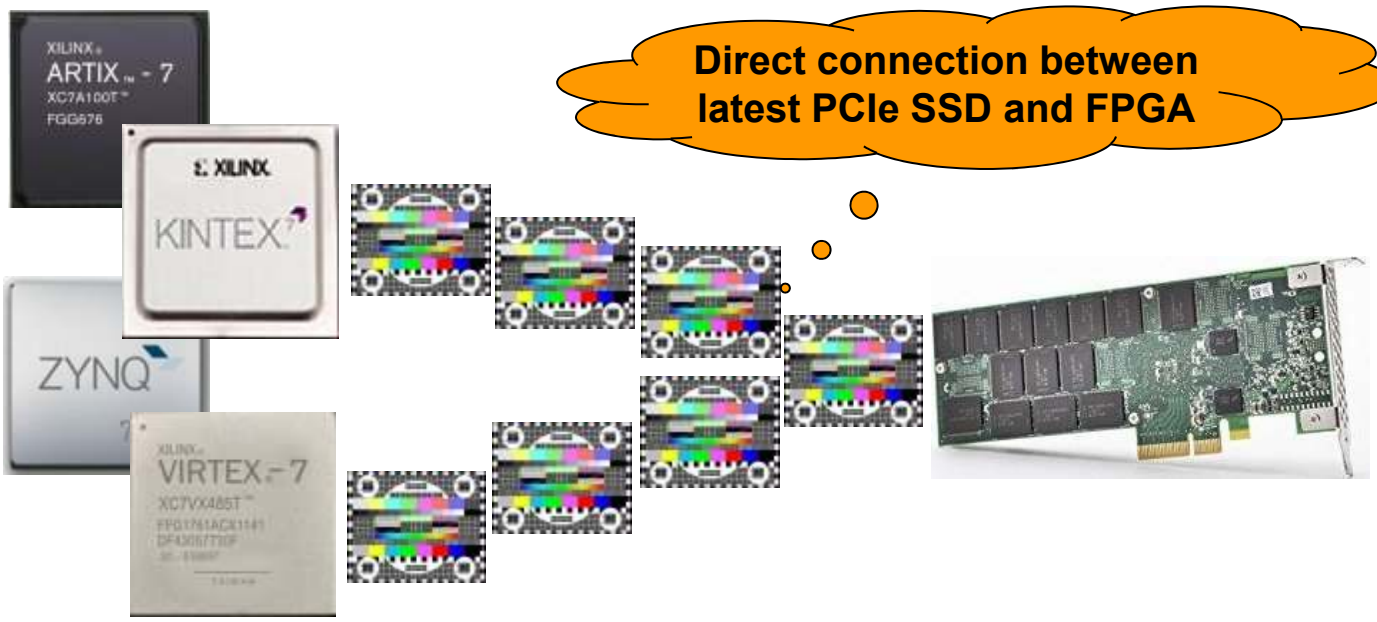
APS-IP Introduction for Xilinx

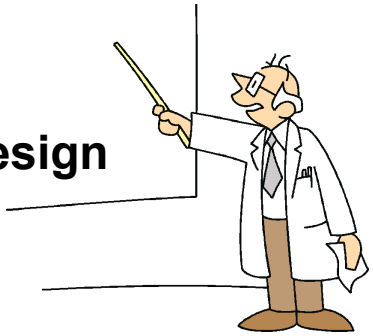
Ver1.3E



Ideal for embedded storage !

Agenda

- PCIe SSD Overview
  - SSD Trends
  - Merit of PCIe SSD for embedded system
- APS-IP Introduction
  - Summary
  - Function
  - User Interface
  - Performance and Size
  - Development Environment/Reference Design
- Application



SSD Trends

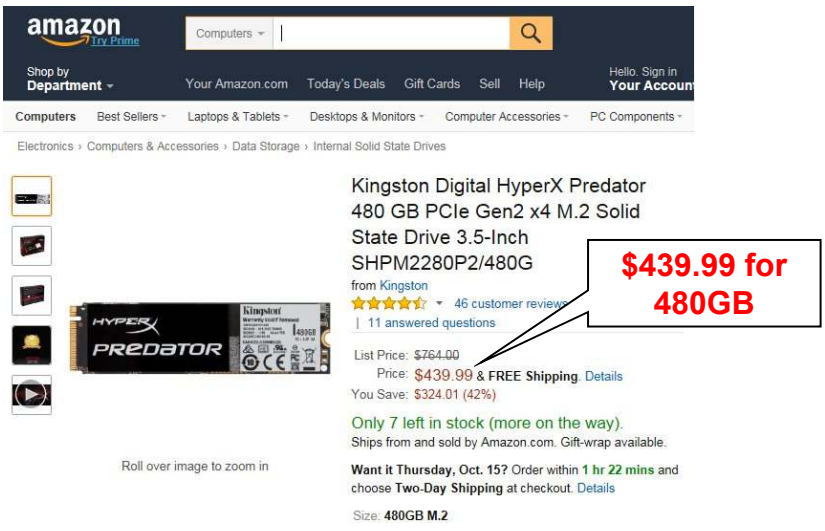
- SATA interface is now performance bottle neck
  - SSD Read/Write speed is limited to 600MB/sec SATA bandwidth
- Move to PCI Express for faster speed
  - PCIe GEN3 x4lane can provide 4GB/sec transfer speed
- M.2 form factor suitable for compact product application
  - Width=22mm, Lenth=20/42/80/120mm, DIMM-like very small outline

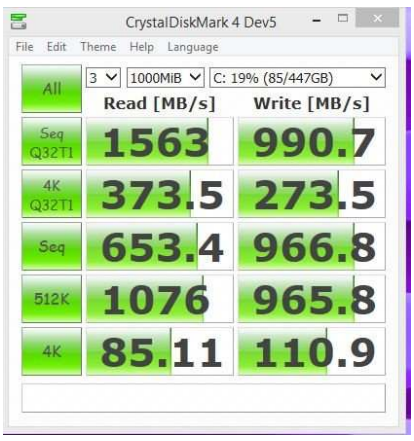
Current 2.5" SATA SSD

Latest M.2 type PCIe SSD

Merit of PCIe SSD for Embedded System 1

- High Bandwidth: 1.5GB/s for Read, 1GB/s for Write
- Cost effective: Cost difference from SATA SSD is small





(http://www.bjorn3d.com/2015/03/480gb-hyperx-predator-m-2-pcie-ssd-shpm2280p2480g/6/)

Cost and Performance of M.2 PCIe SSD (Kingston 480GB)

Merit of PCIe SSD for Embedded System 2

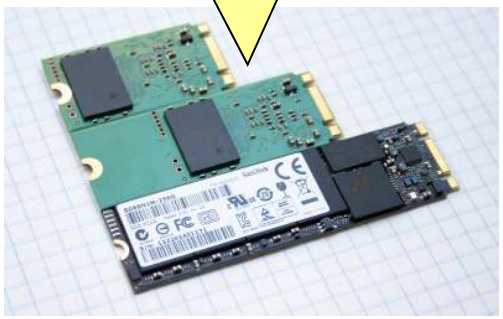
- **Various form factor**
  - HHHL(Half-Height,Half-Length) general PCIe board
  - M.2 cost saving module
  - SFF-8639 of 2.5” drive compatible size

Merit

Big Capacity

HHHL PCIe board

Small Size



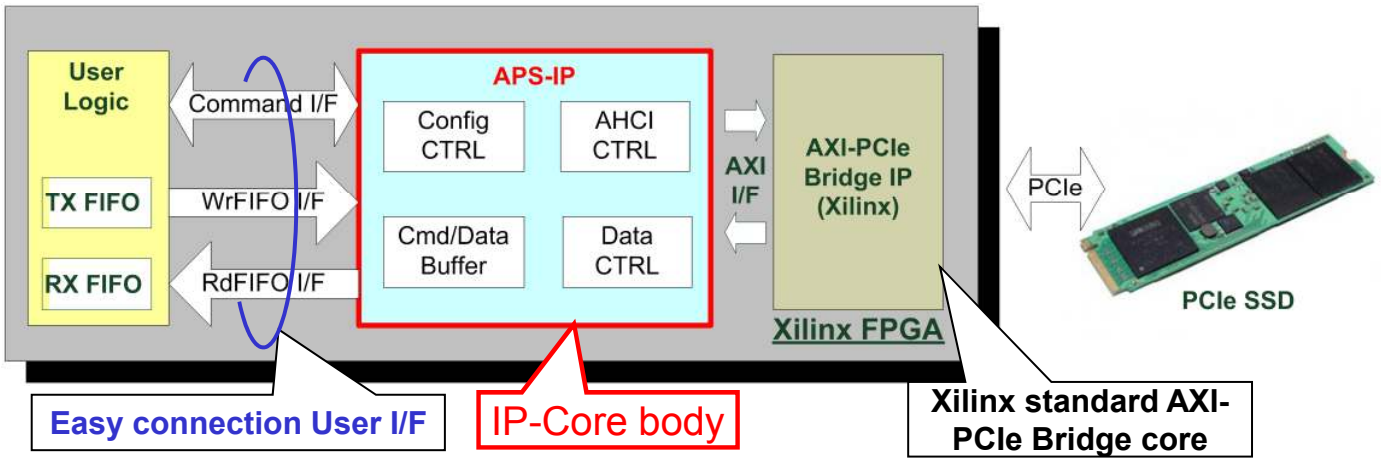
M.2 module (length=42/60/80mm)

Hot Swap

SFF-8639 package

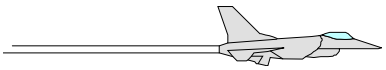
What’s APS-IP

- What’s APS-IP? -> Reduction of AHCI PCIe SSD IP Core
- Function? -> PCIe Root with full automatic SSD R/W function
- How to use? -> Just connect with user logic, no need CPU&F/W
- User Merit? -> Can develop Storage Application in short period



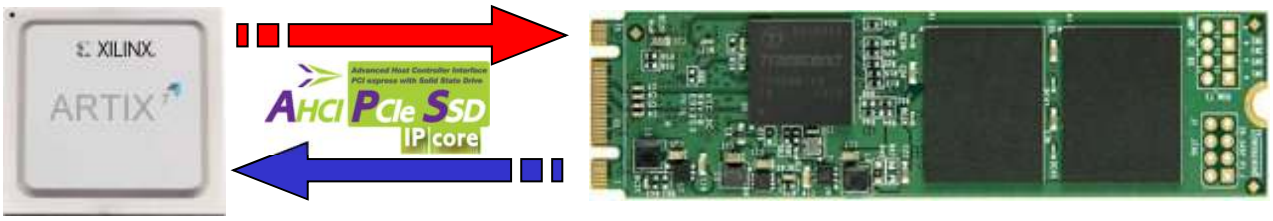
APS-IP Merit

1. **Function: Full automatic access to PCIe SSD**
   - No CPU and firmware necessary, just wired logic is enough
2. **Interface: Simple and easy connection**
   - Direct connection to Xilinx standard AXI PCIe bridge core via AXI
   - User I/F control is parameter with pulse, data is simple FIFO
3. **High Performance and Compact size**
   - Write=1262MB/s、Read=2213MB/s
   - Support PCIe GEN3 (Operation confirmed on Kintex Ultrascale)
   - Core size=482Slice,559DFF (for 7-series version)
4. **Environment: Full reference design project**
   - Full Vivado project with real board operation in the package



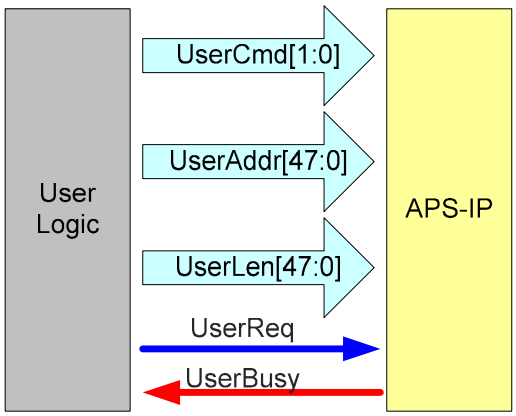
APS-IP Merit 1: Function

- **Special PCIe Root port function for SSD control**
  - PCIe Initialization: BAR Init./MSI Interrupt set/Master mode set
  - SSD Status Monitor: Intr./Status automatic check
- **AHCI Read/Write function**
  - Control AHCI register by user R/W request and execute access
  - Data transfer and flow control between PCIe and FIFO

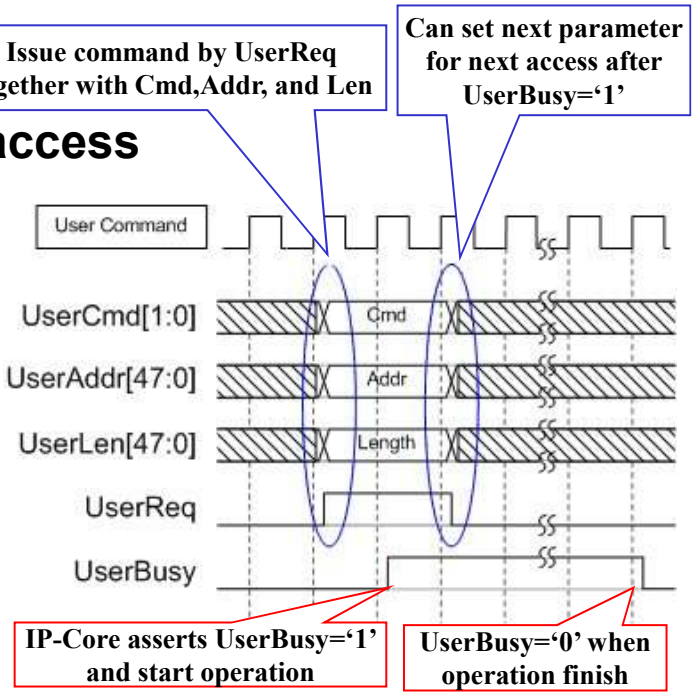


APS-IP Merit2: Command I/F

- **Easy Connection User I/F**
  - Set Command/Address/Length
  - Issue UserReq pulse
- **Full Automatic control for SSD access**
  - User only can wait UserBusy negation



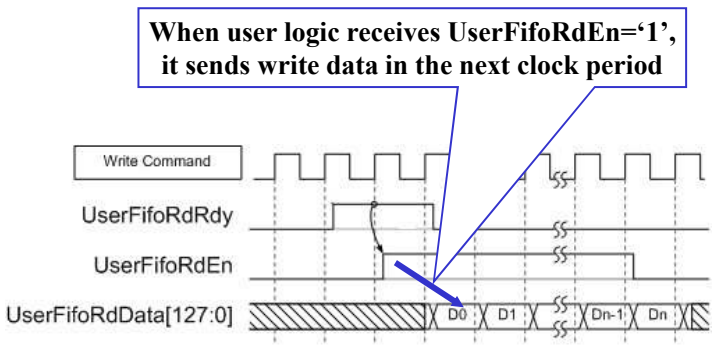
Command I/F Signals



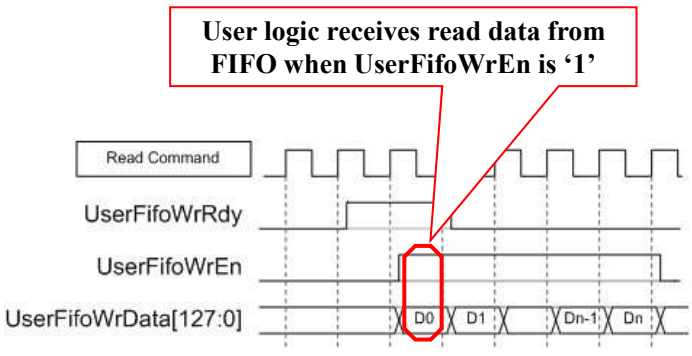
Command I/F waveform

APS-IP Merit2: Data I/F

- **Simple 128bit FIFO for each of read and write**
  - User Logic sends write data by UserFifoRdEn from IP-Core
  - User Logic gets read data with UserFifoWrEn from IP-Core



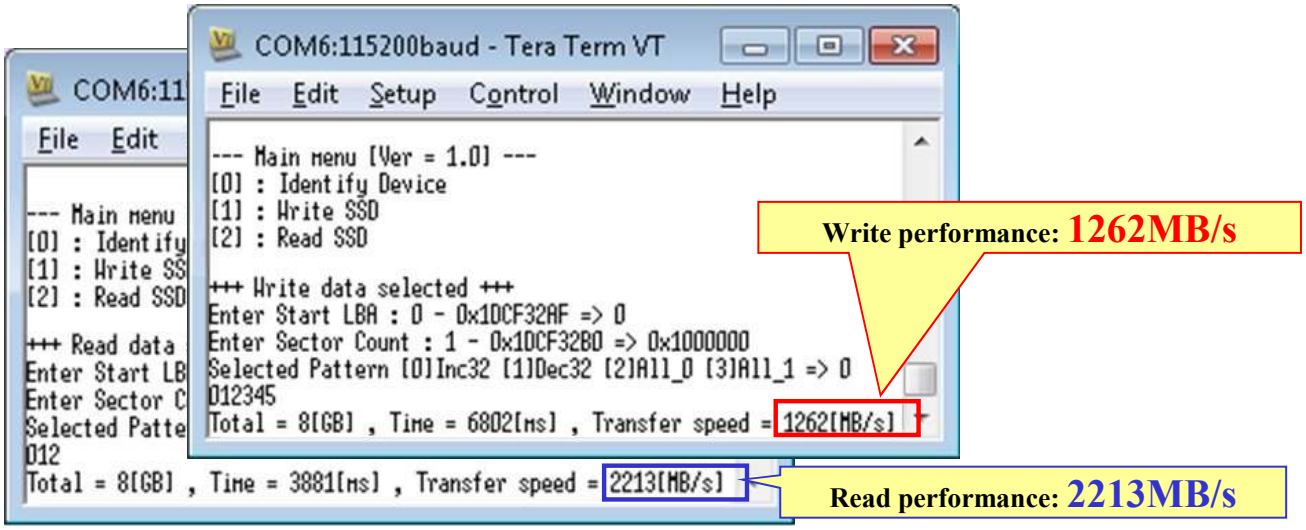
Write data waveform



Read data waveform

APS-IP Merit3: Performance

- **Automatic PCIe SSD access by pure hard-wired logic**
  - **Intelligent state machine for complete read/write command execution**
  - **Minimum over head and best performance by synchronized circuit**



Performance Evaluation Result (KCU105) **(SSD: Samsung MZ-HPV2560)**

APS-IP Merit3: Compact Size

- **Optimized size with minimum resource consumption**
  - **Includes necessary control logic and temporary buffer only**
  - **Data FIFO is not in IP-Core so user can select FIFO size**

Example Implementation Statistics for 7-Series device (PCIe Gen2)

Family	Example Device	Fmax (MHz)	Slice Regs	Slice LUTs	Slices[1]	Design Tools
Kintex-7	XC7K325TFFG900-2	125	559	1311	482	Vivado2014.4
Virtex-7	XC7VX485TFFG1761-2	125	559	1313	482	Vivado2014.4
Zynq-7000	XC7Z045FFG900-2	125	559	1311	485	Vivado2014.4

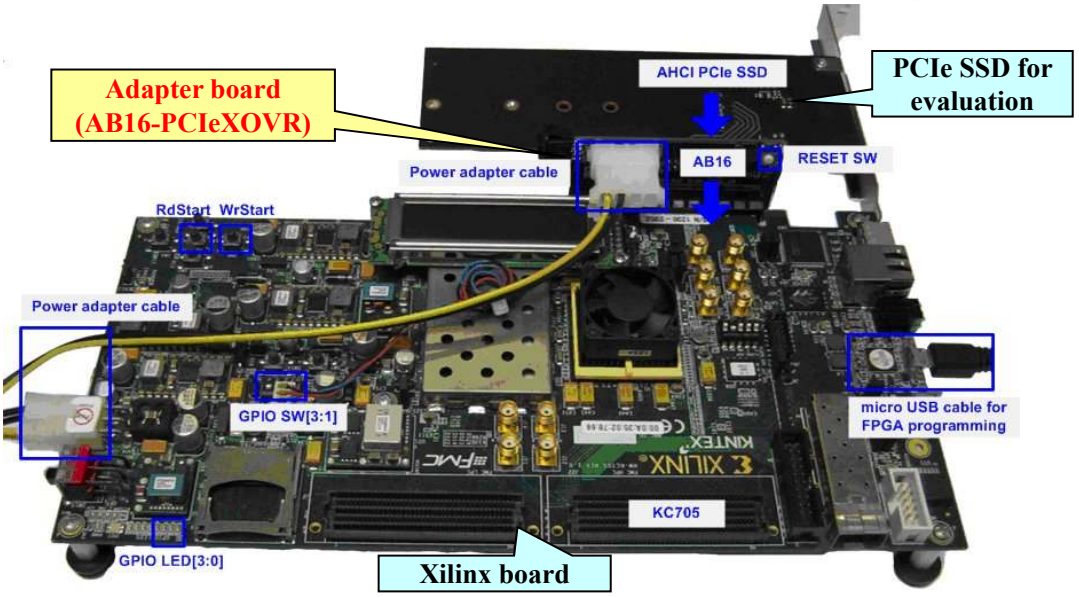
Example Implementation Statistics for Ultrascale device (PCIe Gen3)

Family	Example Device	Fmax (MHz)	LUT FF	LUT Logic	CLB	Design Tools
Kintex-Ultrascale	XCKU040FFVA1156-2E	250	1230	650	270	Vivado2015.4

APS-IP Core resource usage **(Note: AXI-PCIe bridge IP from Xilinx is not included)**

APS-IP Merit4: Environment

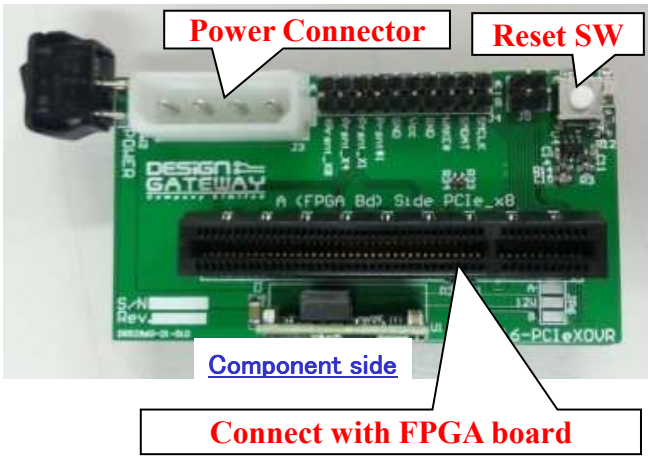
- Real operation check with Xilinx evaluation board
- Free bit-file for evaluation before IP-core purchase

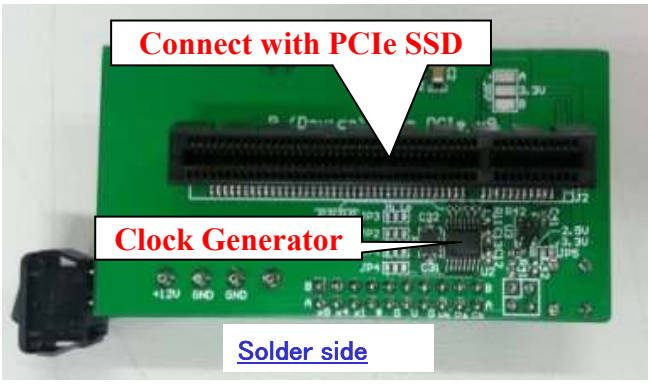


IP-Core evaluation environment using KC-705

APS-IP Merit4: Development Tool

- Adapter board for FPGA board evaluation（Part#: AB16-PCIeXOVR)
- Connect FPGA board to PCIe socket on component side
- Connect PCIe SSD to PCIe socket on solder side
- SSD R/W access via adapter board from APS-IP in FPGA





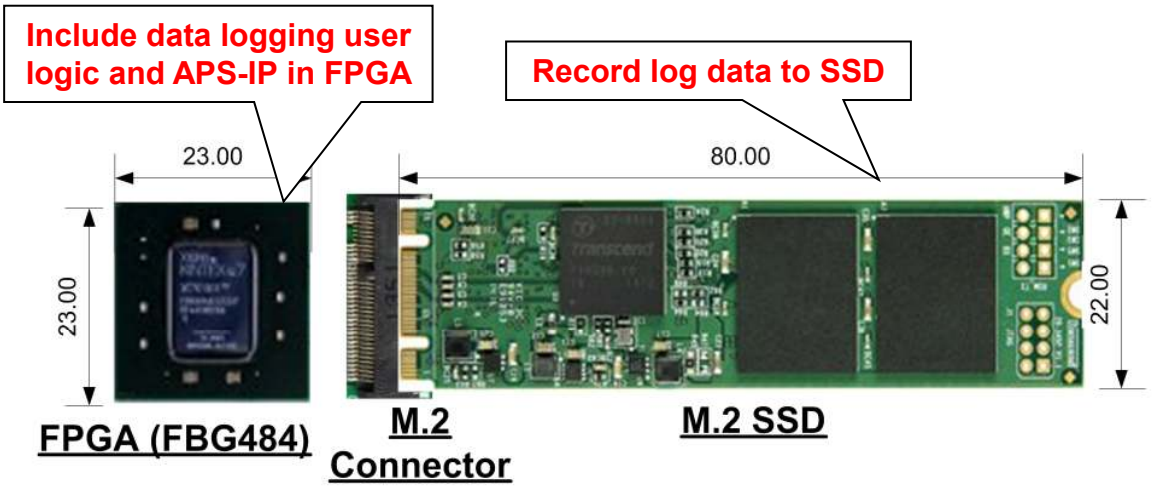
APS-IP Merit4: Reference Design

- Vivado project is attached with APS-IP deliverables
- Full source code (VHDL) except IP core
- Can save user system development duration
  - Confirm real board operation by original reference design.
  - Then modify a little to approach final user product.
  - Check real operation in each modification step.

Short-term development is possible without big turn back

APS-IP Application Example

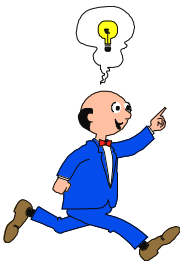
- Space-Saving FPGA data logging system
  - Latest FPGA + M.2 SSD



System space image by FBG484 FPGA and M.2 SSD (unit: mm)

For more detail

- **Detailed technical information available on the web site.**
  - http://www.dgway.com/APS-IP_X_E.html
- **Contact**
  - **Design Gateway Co,. Ltd.**
  - **sales@design-gateway.com**
  - **FAX: +66-2-261-2290**



Revision History

Rev.	Date	Description
1.0E	16-Oct-15	English Version 1st release
1.1E	19-Oct-15	Correct some spell
1.2E	13-Jan-16	Improve IP-Core and R/W performance
1.3E	23-Feb-16	Support PCIe GEN3 (Kintex Ultrascale on KCU105)