

# AHCI PCIe SSD-IP (APS-IP) Demo Instruction

Rev1.3 21-Oct-16

This document describes the instruction to run APS-IP demo on Xilinx development board and AB16-PCIeXOVR board. The demo is designed to write/verify data with AHCI PCIe SSD. User can control test operation through Serial console.

# **1** Environment Requirement

To demo APS-IP on Xilinx development board, please prepare following hardware/software.

- 1) Supported FPGA Development board (AC701/KC705/VC707/ZC706/KCU105)
- 2) PC with Xilinx programmer software (iMPACT/Vivado) and Serial console software
- 3) AB16-PCIeXOVR board + power adapter cable from AB16 delivery set
- 4) Xilinx Power adapter
- 5) AHCI PCIe SSD connecting to AB16-PCIeXOVR board
- 6) micro USB cable for programming FPGA between FPGA board and PC
- 7) mini/micro USB cable for Serial console connecting between FPGA board and PC

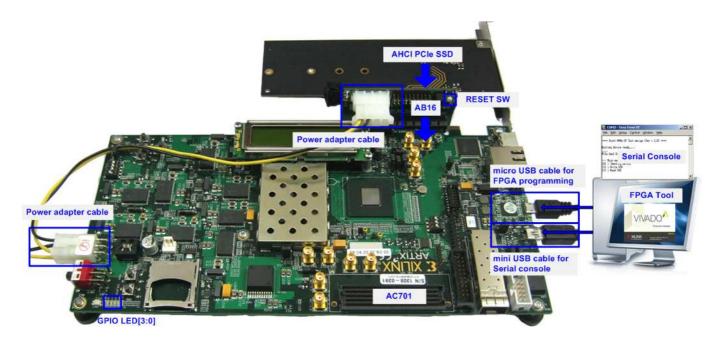


Figure 1-1 APS-IP Demo Environment Setup on AC701







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Figure 1-3 APS-IP Demo Environment Setup on VC707

VC707

GPIO LED[3:0]

VIVADO

mini USB cable for

Serial console







Figure 1-5 APS-IP Demo Environment Setup on KCU105



# 2 Demo setup

- 1) Power off system.
- 2) For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 2-1 Figure 2-2.
   SW11

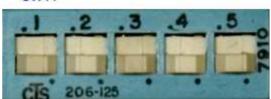
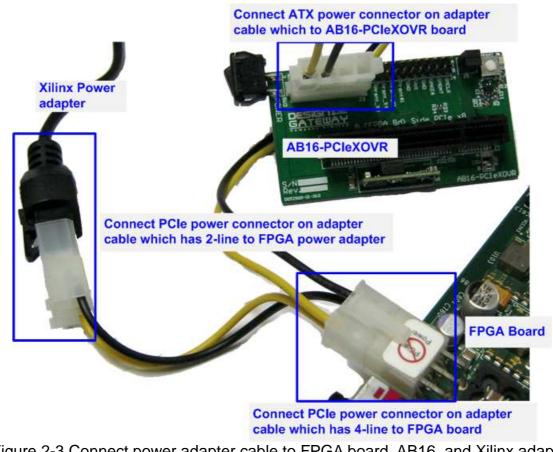


Figure 2-1 SW11 setting to configure PS from JTAG on ZC706 board



Figure 2-2 SW4 setting to use USB-to-JTAG on ZC706 board

3) Connect power adapter cable from AB16-PCIeXOVR delivery set to power connector on FPGA board, AB16-PCIeXOVR board, and Xilinx power adapter as shown in Figure 2-3.



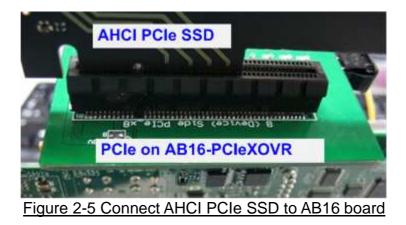


4) Connect A Side of PCIe connector on AB16-PCIeXOVR board to PCIe connector on Xilinx development board, as shown in Figure 2-4. Also check that two mini jumpers are inserted at J5 connector on AB16.



Figure 2-4 Connect PCIe connector between AB16 and FPGA board

5) Connect AHCI PCIe SSD to B Side of PCIe connector on AB16-PCIeXOVR board.



6) Connect micro USB cable from Xilinx development board to PC for JTAG programming, and connect mini USB cable from Xilinx board to PC for Serial console.



Mini USB for Serial console Figure 2-6 USB cable connection



7) Power on FPGA development board and AB16-PCIeXOVR board.

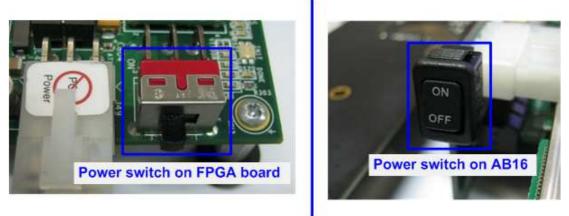


Figure 2-7 Power on FPGA and AB16 board

- 8) Open Serial console such as TeraTerm, HyperTerminal and set Buad rate=115,200 Data=8 bit Non-Parity Stop=1.
- Download bit file or bat file to configure FPGA and firmware.

   a) For ZC706 board, open ISE command prompt or Vivado TCL shell, change current directory to ready\_for\_download\_zc706, and run zc706\_APSIPTest.bat, as shown in Figure 2-8 and Figure 2-9.



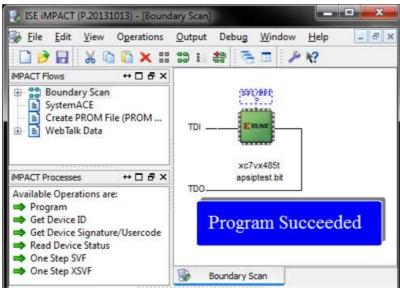
Figure 2-8 Command script for download demo file to ZC706 by ISE tool



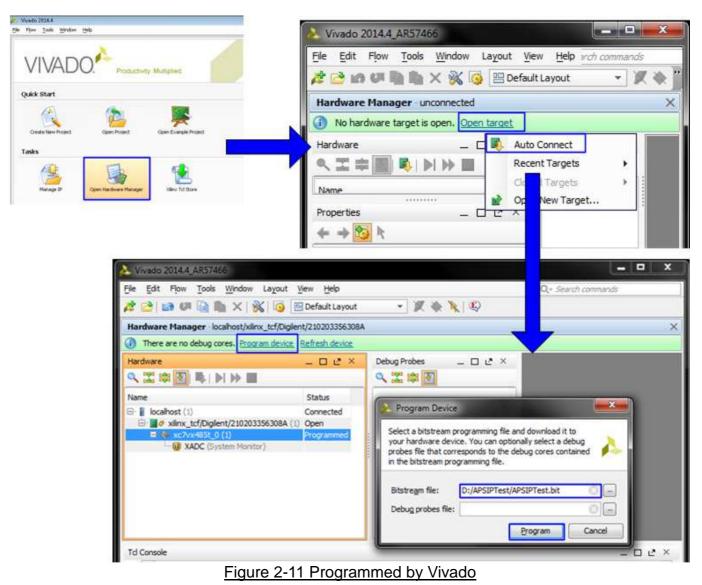
#### Figure 2-9 Command script for download demo file to ZC706 by Vivado tool

b) For AC701/KC705/VC707/KCU105 board, use iMPACT or Vivado tool to program bit file, as shown in Figure 2-10 and Figure 2-11.





## Figure 2-10 Programmed by iMPACT





10)Check LED status on Xilinx development board. The description of LED is follows.

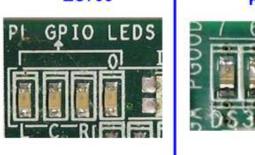
GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1/R	System is busy	Idle status
2/C	PCIe Error detect	Normal operation
3/L	Data verification fail	Normal operation
	Table	2-1 LED Definition

#### AC701

# ZC706

## KC705/VC707/KCU105





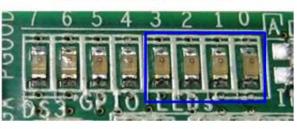


Figure 2-12 4-bit LED Status for user output

11)After programming completely, LED[0] and LED[1] will be ON during PCIe initialization process. Then, LED[1] will be OFF to show that PCIe completes initialization process and now system is ready to receive command from user. PCIe speed will be displayed on the console before Main menu, as shown in Figure 2-14.

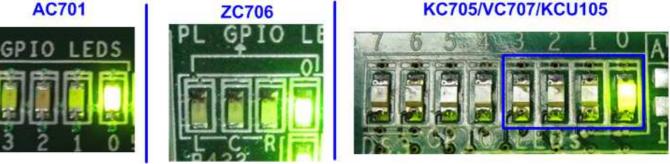


Figure 2-13 LED status after program configuration file and PCIe initialization complete

<u>File Edit Setup Control Window Help</u>	<u>File Edit Setup Control Window Help</u>
++++ Start APS-IP Test design [Ver = 1.2] ++++ Haiting device ready Wait PCIe Linkup PCIe Gen3 Device Detect PCIe speed = Gen3	++++ Start RPS-IP Test design [Ver = 1.2] ++++ Haiting device ready PCIe Gen2 Device Detect PCIe speed = Gen2
Hain nenu [Ver = 1.2] [0] : Identify Device [1] : Hvite SSD [2] : Read SSD Main menu to select operating command	Main menu [Ver = 1.2] [0] : Identify Device [1] : Write SSD [2] : Read SSD

Figure 2-14 Main menu after program configuration file and PCIe initialization complete



# 3 Test Menu

### 3.1 Identify Device

Select '0' to send Identify device command to AHCI PCIe SSD. When operation is completed, SSD capacity will be displayed on the console.

<u>File Edit Setup Control Window</u>	Help
+++ Identify Device selected +++ Model Number : SAMSUNG MZHPV256HDGL-00000 SSD Capacity= 256[GB]	Model number and Disk capacity after complete IDENTIFY DEVICE command
Main menu [Ver = 1.2] [0] : Identify Device [1] : Hrite SSD	
[2] : Read SSD	



## 3.2 Write SSD

Select '1' to send Write command to AHCI PCIe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. This input can be decimal unit or add prefix "0x" for hexadecimal unit.

2) Sector Count: Input total transfer size in sector unit. This input can be decimal unit or add prefix "0x" for hexadecimal unit.

3) Test pattern: Select test pattern of test data for writing to SSD. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

<u>File</u> <u>E</u> dit	Setup	Control	Window	Help
++ Hrite da nter Start nter Sector elected Pat 1.247 GB 2.502 GB	LBA : 0 - Count : 1	0x1DCF32AF - 0x1DCF3	280 => 0x400	0000 Input from user 131R11_1 => 0
31.250 GB 32.501 GB 33.738 GB	91 Tius	- 22(-1		Output performance
Hain nen		.21	iransier spe	60 = 1549(110/\$1

Figure 3-2 Input and result of Write SSD menu

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, number 0-9 will be printed out to the console to show that system still be alive. Finally, test performance with the size and time usage will be displayed on the console.



Figure 3-3 – Figure 3-5 show error message when user input is invalid. "Invalid input" message will be displayed on the console, and then return to main menu to receive new command.

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•
ge add

Figure 3-3 Invalid Start LBA input

<u>F</u> ile	Edit	Setup	Control	Window	Help	
ter	Start L	a selecte RA : A -	0x100E328E	=> በ		*
	a dia a		CHILDON OLIN			
nter nvali	Sector d input	Count : 1	L - UX10CF3	280 => 0x200	00000 Out-0	of-range l
nvali Ha 0] : 1] :	d input in непи	: I [Ver = 1 Y Device SD	AD-011	280] => [0x200	00000 Out-	of-range

Figure 3-4 Invalid Sector count input

File	Edit	Setup	Control	Window	Help		
		a selecte				*	
			0x1DCF32AF		0000		
nter :	Sector	Count : 1	1 - 0x10CF3	260 => DX400	0000	11	
electo	ed Patt	ern [0]Ir	1 - Ux1UCF3 nc32 [1]Dec	280 => 0x400 32 [2]All_0	(3)811_1 =>[	Out-of-	range patt
electo nvalio	ed Patt d input	ern [0]Ir	nc32 [1]Dec	280 => 0x400 32 [2]A11_0	0000 (3)All_1 => <mark>(</mark>	4 Out-of-r	range patt
electo nvalio Ha	ed Patt d input in непи	ern [0]Ir [Ver = 1	nc32 [1]Dec	280 => 0x400 32 [2]A11_0	(3)A11_1 => <mark>(</mark>	4 Out-of-r	range patt
electo nvalio Ha D] :	ed Patt d input in непи	ern [0]Ir [Ver = 1 y Device	nc32 [1]Dec	280 => 0x400 32 [2]All_0	0000 [3]All_1 => <mark>[</mark>	4 Out-of-r	range patt

Figure 3-5 Invalid Test pattern input



# 3.3 Read SSD

Select '2' to send Read command to AHCI PCIe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. The input can be decimal unit or add prefix "0x" for hexadecimal unit.

2) Sector Count: Input total transfer size in sector unit. The input can be decimal unit or add prefix "0x" for hexadecimal unit.

3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with write test. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

<u>F</u> ile	Edit	Setup	Control	Window	Help	
nter inter elect 2.21	Start L Sector	Count : 1	0x10CF32AF - 0x10CF3	280 => 0x400	0000 133811_1 =>[	Input from user
30.9 33.2	81 GB 97 GB 12 GB = 34[GE	3], Time	= 15[s] ,	Transfer spe	ed = 2214[HB	/s] Output performa
01:11:			.21			

Similar to write test if all inputs are valid, the operation will be started and test performance will be displayed when end of transfer. "Invalid input" will be displayed if any input value is out-of-range.



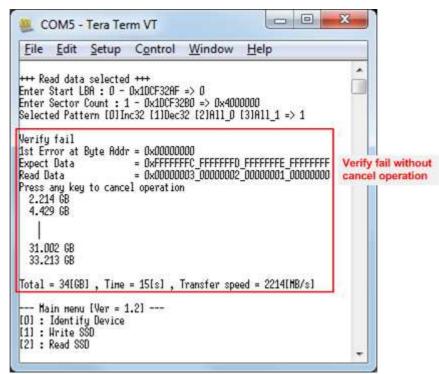


Figure 3-7 Data verification is failed, but wait until read complete

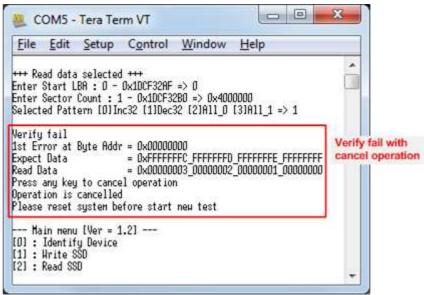


Figure 3-8 Data verification is failed, and press key to cancel operation

Figure 3-7 and Figure 3-8 shows the error message when data verification is failed. "Verify fail" message will be displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete. "RESET" button should be pressed to restart the system when user cancel the operation.



# 4 Revision History

Revision	Date	Description
1.0	25-Sep-15	Initial version release
1.1	17-Feb-16	Support KCU105 board
1.2	1-Mar-16	Add PCIe speed information
1.3	21-Oct-16	Support AC701 board