AHCI PCIe SSD-IP (APS-IP) Demo Instruction

Rev1.3 21-Oct-16

This document describes the instruction to run APS-IP demo on Xilinx development board and AB16-PCIeXOVR board. The demo is designed to write/verify data with AHCI PCIe SSD. User can control test operation through Serial console.

1 Environment Requirement

To demo APS-IP on Xilinx development board, please prepare following hardware/software.

1) Supported FPGA Development board (AC701/KC705/VC707/ZC706/KCU105)
2) PC with Xilinx programmer software (iMPACT/Vivado) and Serial console software
3) AB16-PCIeXOVR board + power adapter cable from AB16 delivery set
4) Xilinx Power adapter
5) AHCI PCIe SSD connecting to AB16-PCIeXOVR board
6) micro USB cable for programming FPGA between FPGA board and PC
7) mini/micro USB cable for Serial console connecting between FPGA board and PC

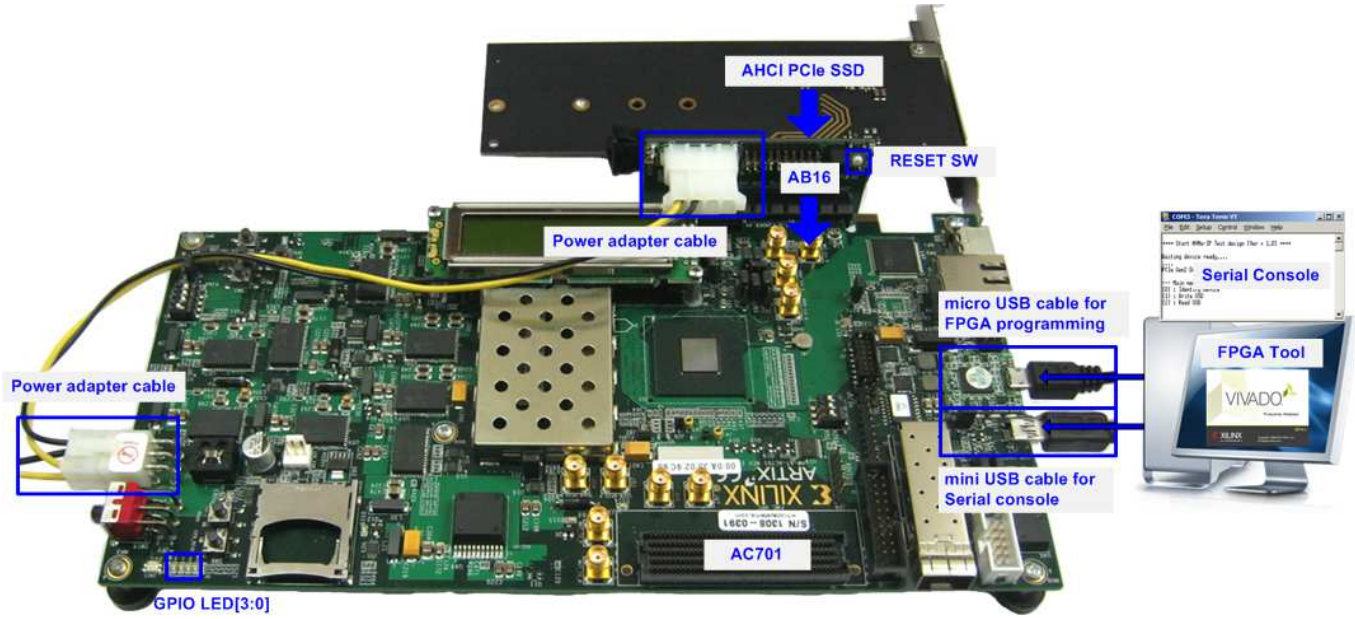

Figure 1-1 APS-IP Demo Environment Setup on AC701

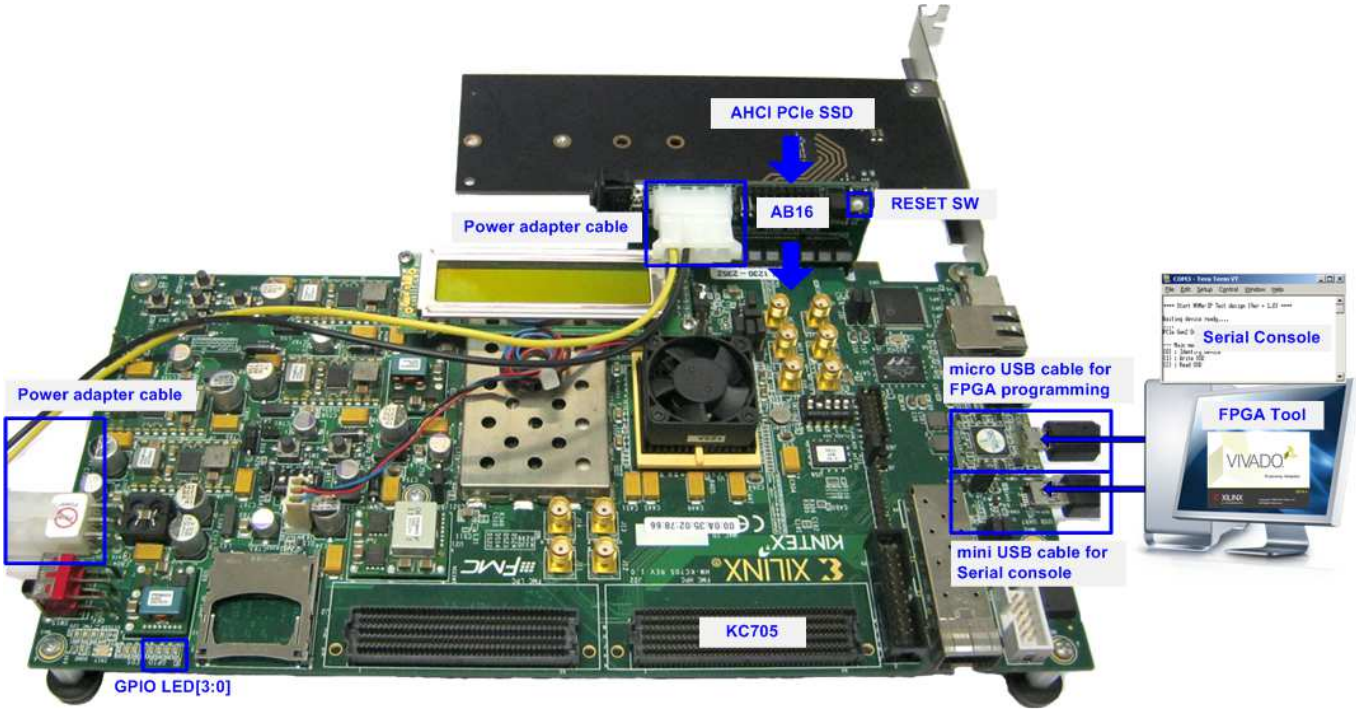

Figure 1-2 APS-IP Demo Environment Setup on KC705

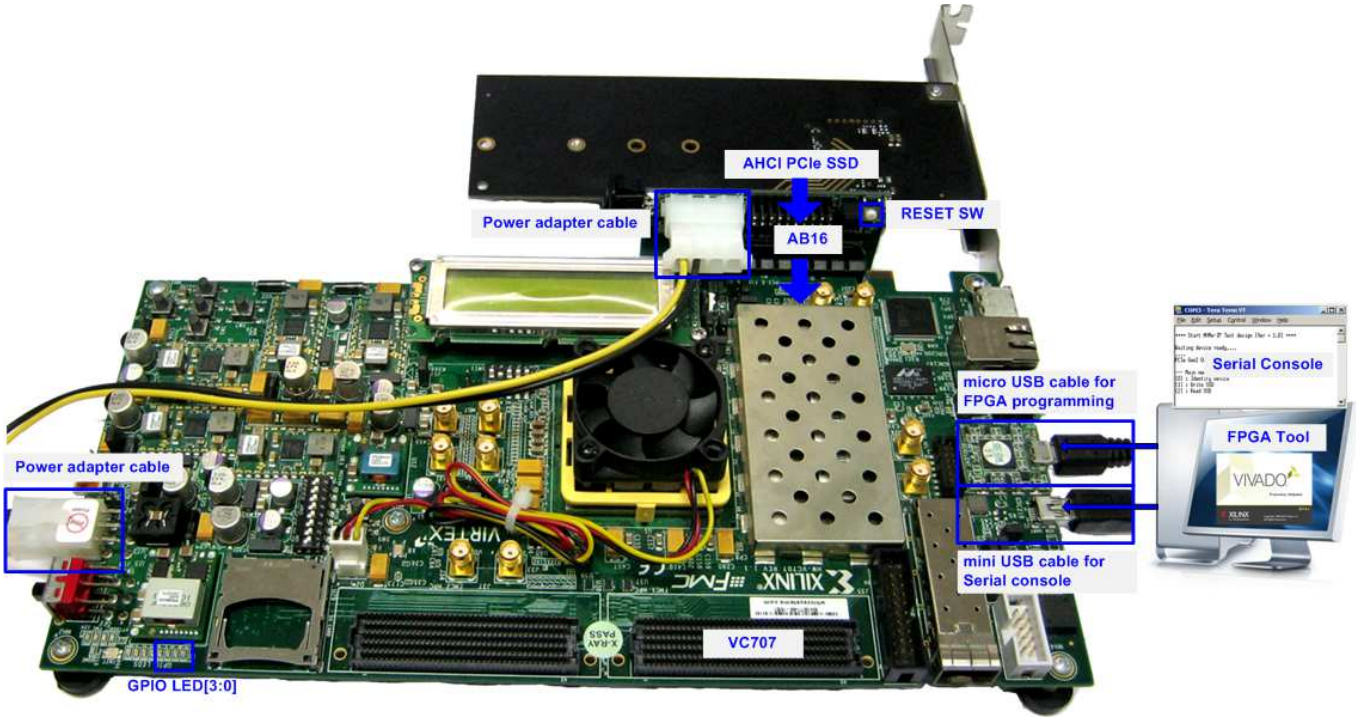

Figure 1-3 APS-IP Demo Environment Setup on VC707

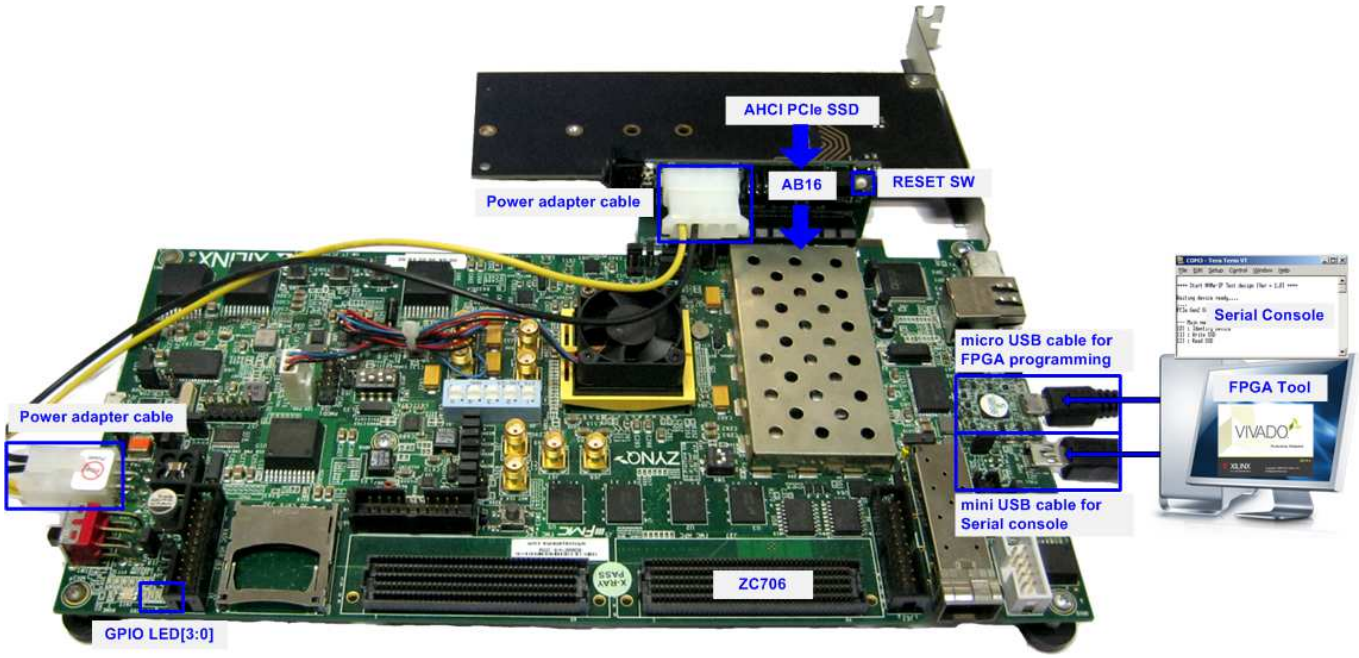

Figure 1-4 APS-IP Demo Environment Setup on ZC706

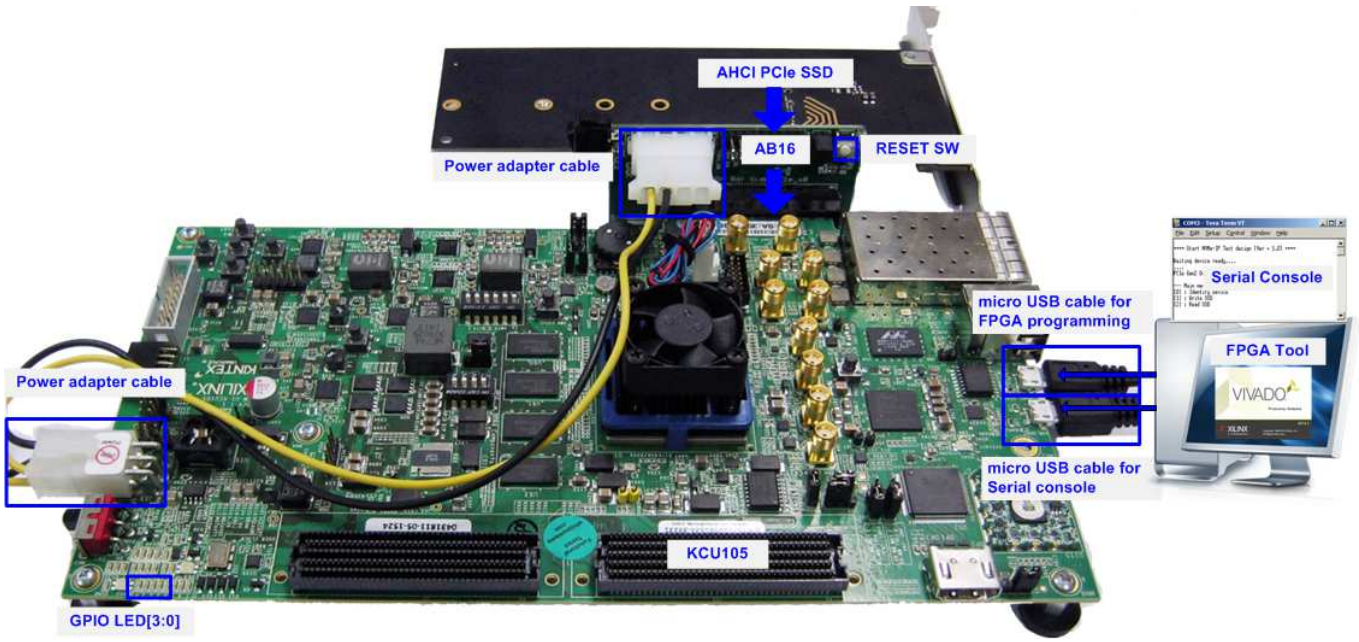

Figure 1-5 APS-IP Demo Environment Setup on KCU105

2 Demo setup

1) Power off system.
2) For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 2-1 – Figure 2-2.

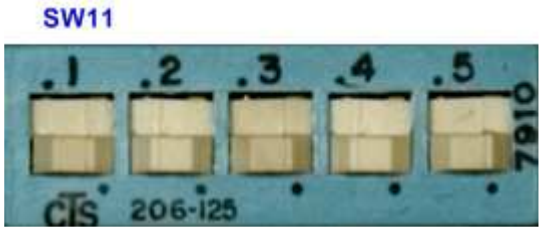

Figure 2-1 SW11 setting to configure PS from JTAG on ZC706 board

Figure 2-2 SW4 setting to use USB-to-JTAG on ZC706 board

3) Connect power adapter cable from AB16-PCIeXOVR delivery set to power connector on FPGA board, AB16-PCIeXOVR board, and Xilinx power adapter as shown in Figure 2-3.

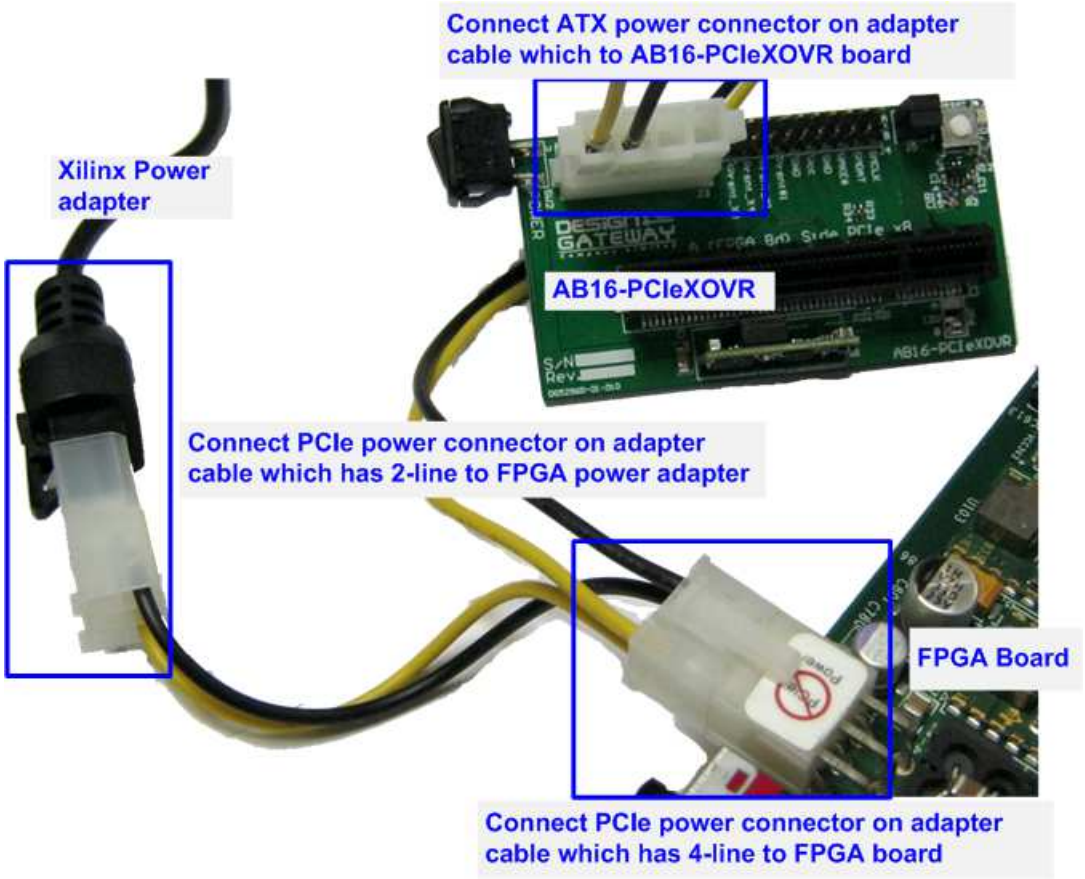

Figure 2-3 Connect power adapter cable to FPGA board, AB16, and Xilinx adapter

4) Connect A Side of PCIe connector on AB16-PCIeXOVR board to PCIe connector on Xilinx development board, as shown in Figure 2-4. Also check that two mini jumpers are inserted at J5 connector on AB16.

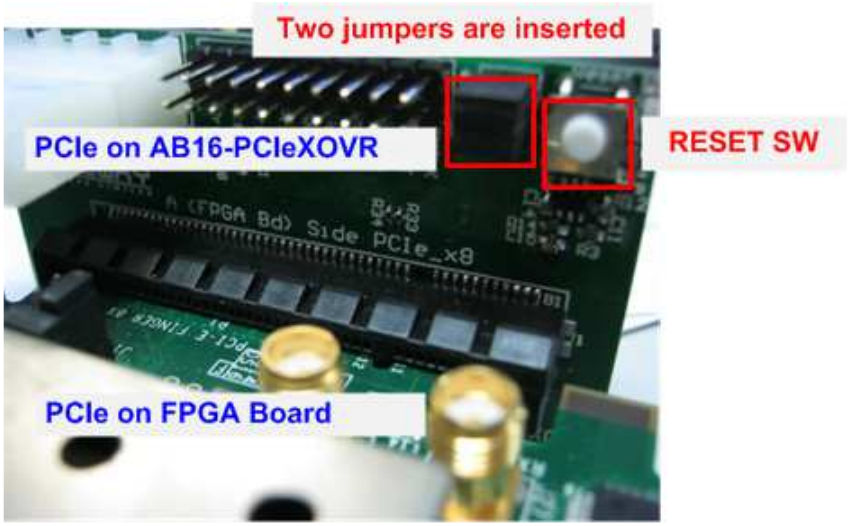

Figure 2-4 Connect PCIe connector between AB16 and FPGA board

5) Connect AHCI PCIe SSD to B Side of PCIe connector on AB16-PCIeXOVR board.

Figure 2-5 Connect AHCI PCIe SSD to AB16 board

6) Connect micro USB cable from Xilinx development board to PC for JTAG programming, and connect mini USB cable from Xilinx board to PC for Serial console.

Figure 2-6 USB cable connection

7) Power on FPGA development board and AB16-PCIeXOVR board.

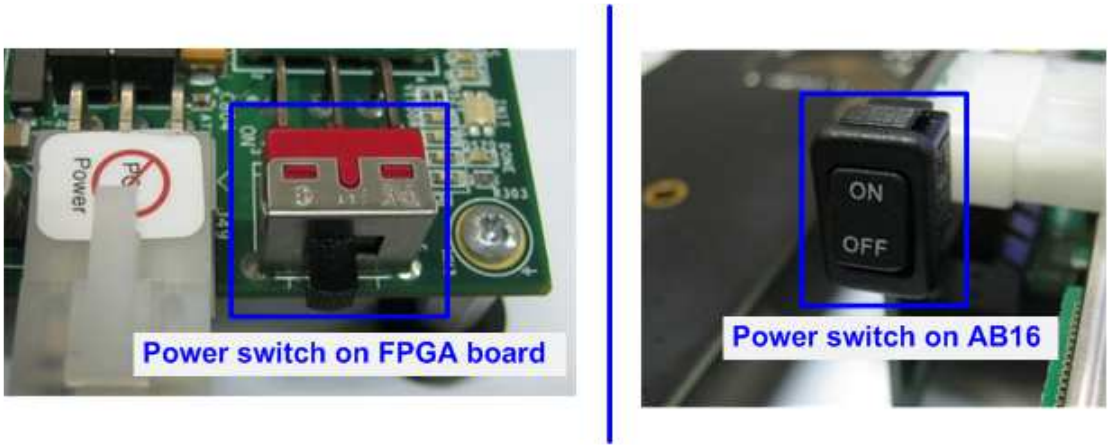

Figure 2-7 Power on FPGA and AB16 board

8) Open Serial console such as TeraTerm, HyperTerminal and set Buad rate=115,200 Data=8 bit Non-Parity Stop=1.
9) Download bit file or bat file to configure FPGA and firmware.
   a) For ZC706 board, open ISE command prompt or Vivado TCL shell, change current directory to ready_for_download_zc706, and run zc706_APSIPTest.bat, as shown in Figure 2-8 and Figure 2-9.

Figure 2-8 Command script for download demo file to ZC706 by ISE tool

Figure 2-9 Command script for download demo file to ZC706 by Vivado tool

b) For AC701/KC705/VC707/KCU105 board, use iMPACT or Vivado tool to program bit file, as shown in Figure 2-10 and Figure 2-11.

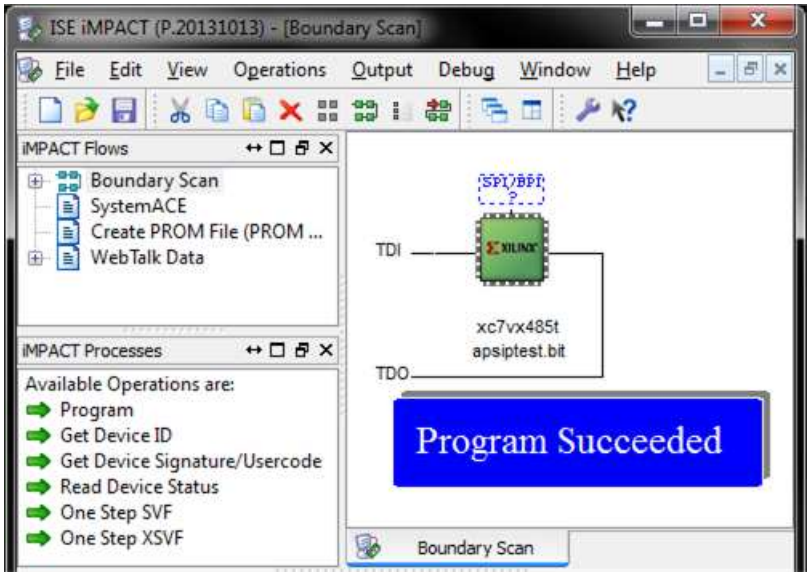

Figure 2-10 Programmed by iMPACT

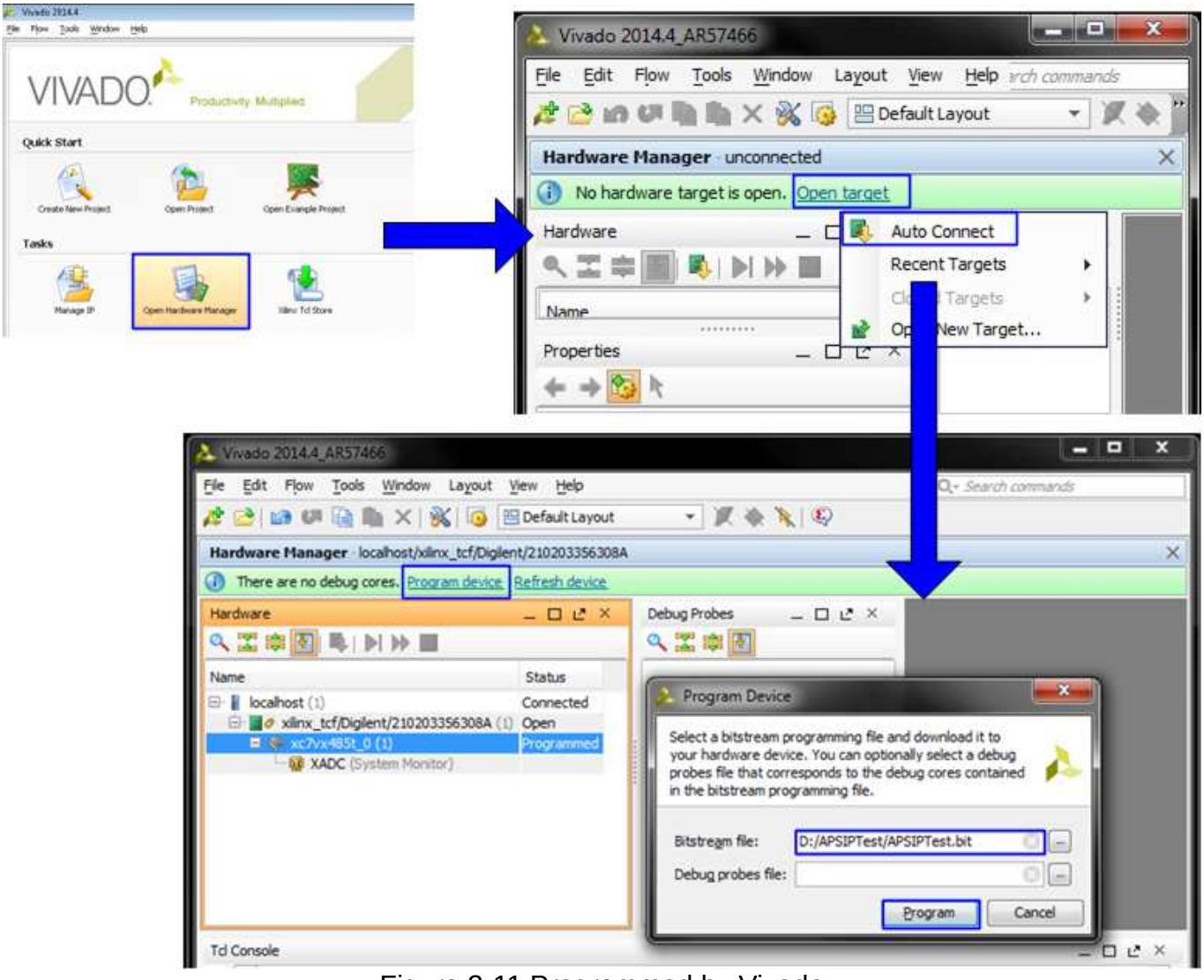

Figure 2-11 Programmed by Vivado

10) Check LED status on Xilinx development board. The description of LED is follows.

GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1/R	System is busy	Idle status
2/C	PCIe Error detect	Normal operation
3/L	Data verification fail	Normal operation

Table 2-1 LED Definition

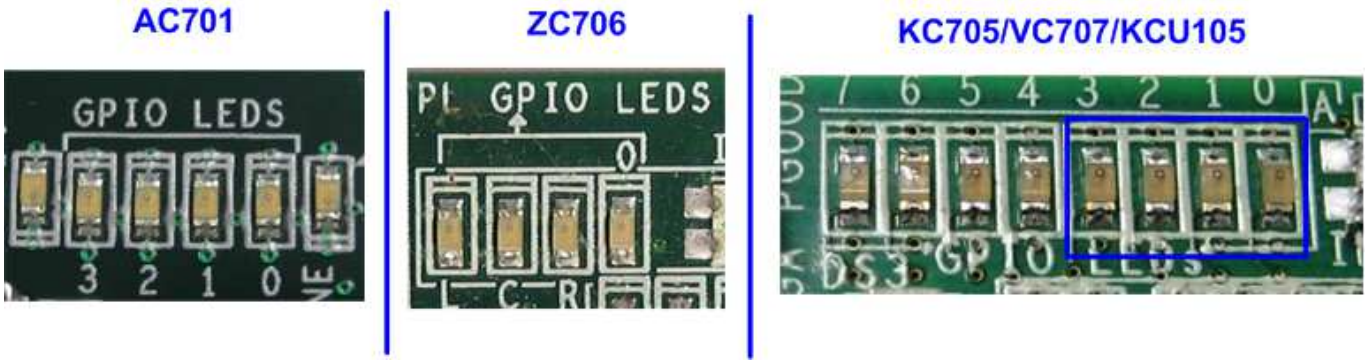

Figure 2-12 4-bit LED Status for user output

11) After programming completely, LED[0] and LED[1] will be ON during PCIe initialization process. Then, LED[1] will be OFF to show that PCIe completes initialization process and now system is ready to receive command from user. PCIe speed will be displayed on the console before Main menu, as shown in Figure 2-14.

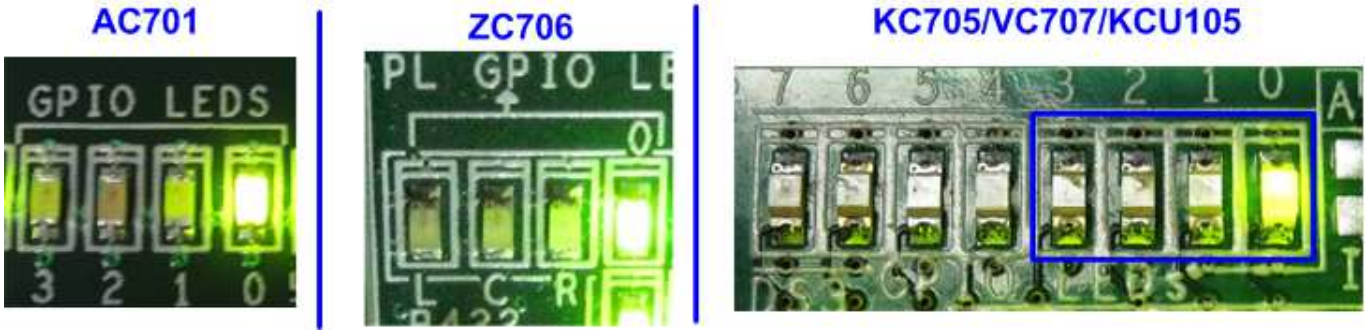

Figure 2-13 LED status after program configuration file and PCIe initialization complete

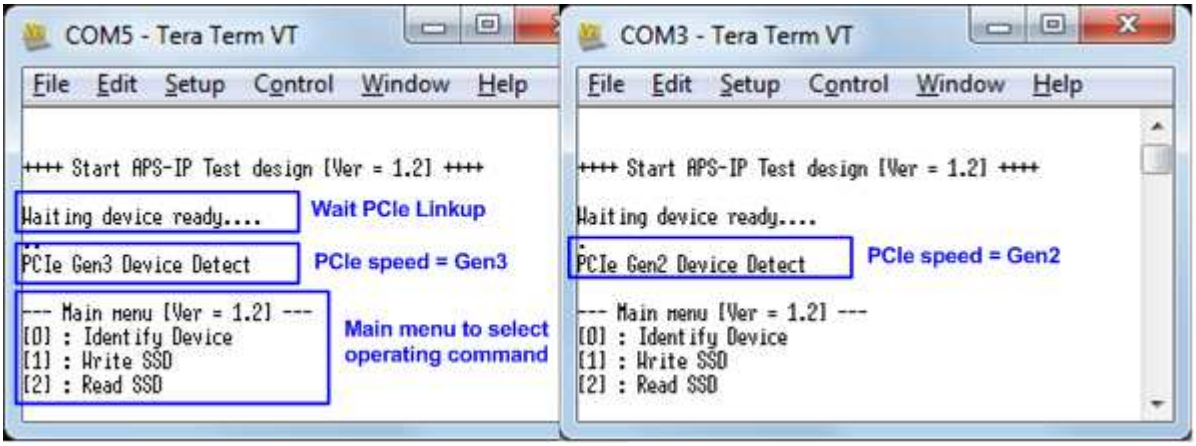

Figure 2-14 Main menu after program configuration file and PCIe initialization complete

3 Test Menu

3.1 Identify Device

Select ‘0’ to send Identify device command to AHCI PCIe SSD. When operation is completed, SSD capacity will be displayed on the console.

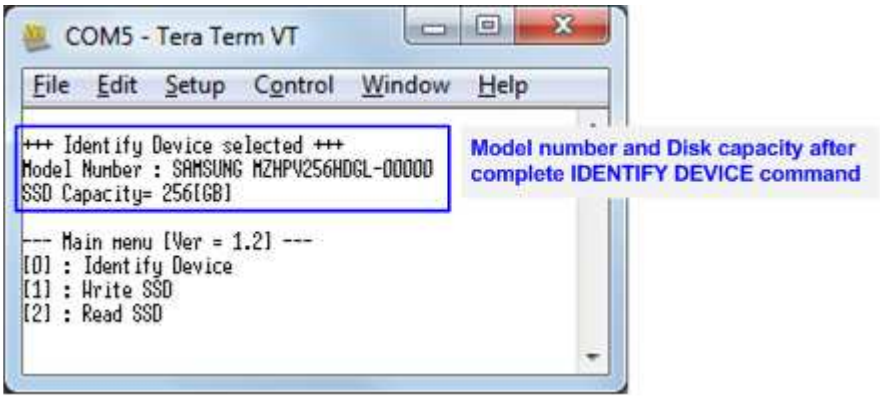

Figure 3-1 Result from Identify Device menu

3.2 Write SSD

Select '1' to send Write command to AHCI PCIe SSD. Three inputs are required for this menu.
1) Start LBA: Input start address of SSD in sector unit. This input can be decimal unit or add prefix "0x" for hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. This input can be decimal unit or add prefix "0x" for hexadecimal unit.
3) Test pattern: Select test pattern of test data for writing to SSD. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

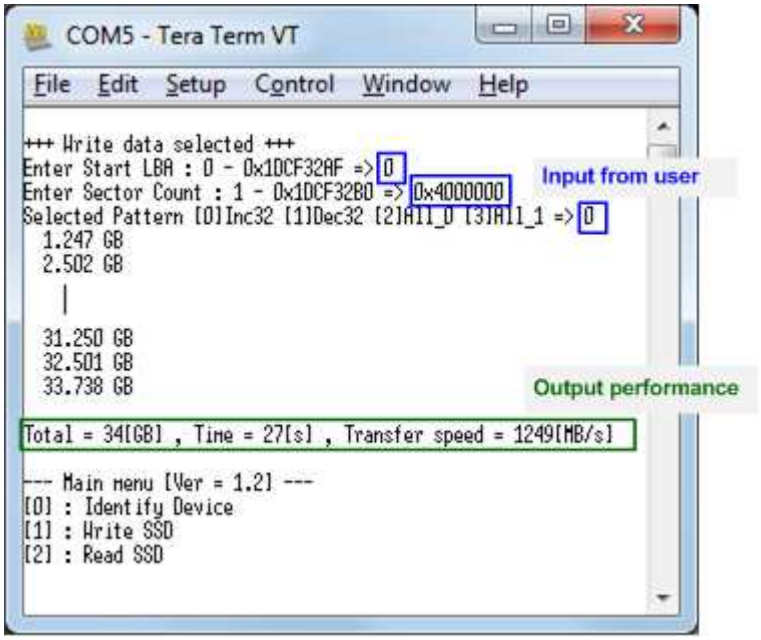

Figure 3-2 Input and result of Write SSD menu

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, number 0-9 will be printed out to the console to show that system still be alive. Finally, test performance with the size and time usage will be displayed on the console.

Figure 3-3 – Figure 3-5 show error message when user input is invalid. “Invalid input” message will be displayed on the console, and then return to main menu to receive new command.

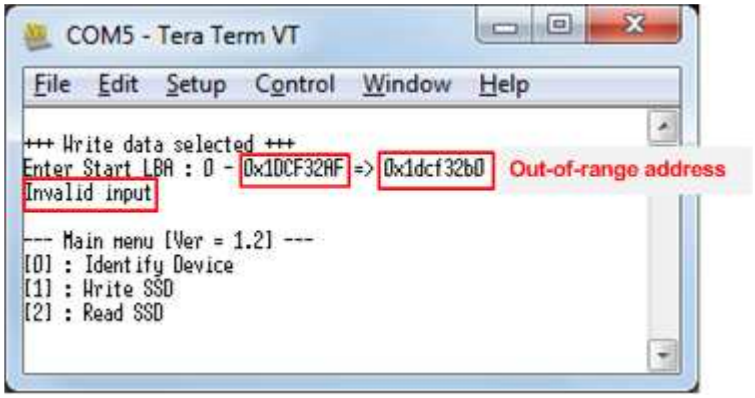

Figure 3-3 Invalid Start LBA input

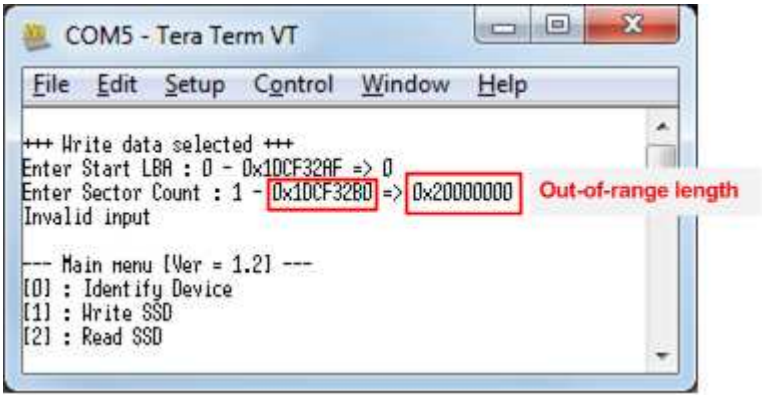

Figure 3-4 Invalid Sector count input

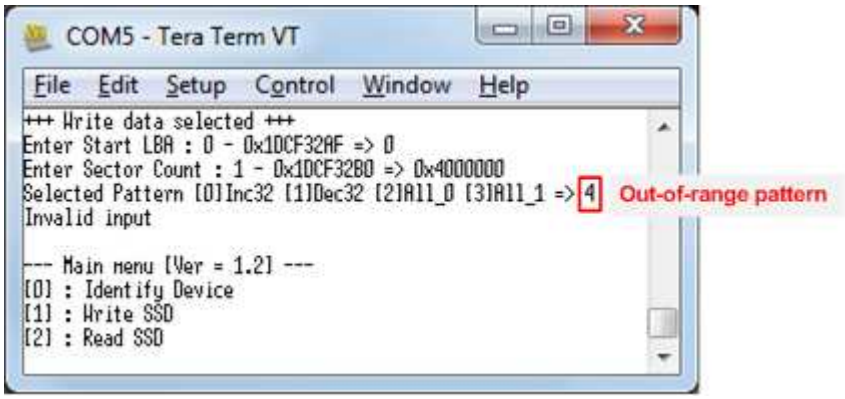

Figure 3-5 Invalid Test pattern input

3.3 Read SSD

Select ‘2’ to send Read command to AHCI PCIe SSD. Three inputs are required for this menu.
1) Start LBA: Input start address of SSD in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input can be decimal unit or add prefix “0x” for hexadecimal unit.
3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with write test. Four types can be used, i.e. 32-bit increment, 32-bit decrement, all 0, and all 1.

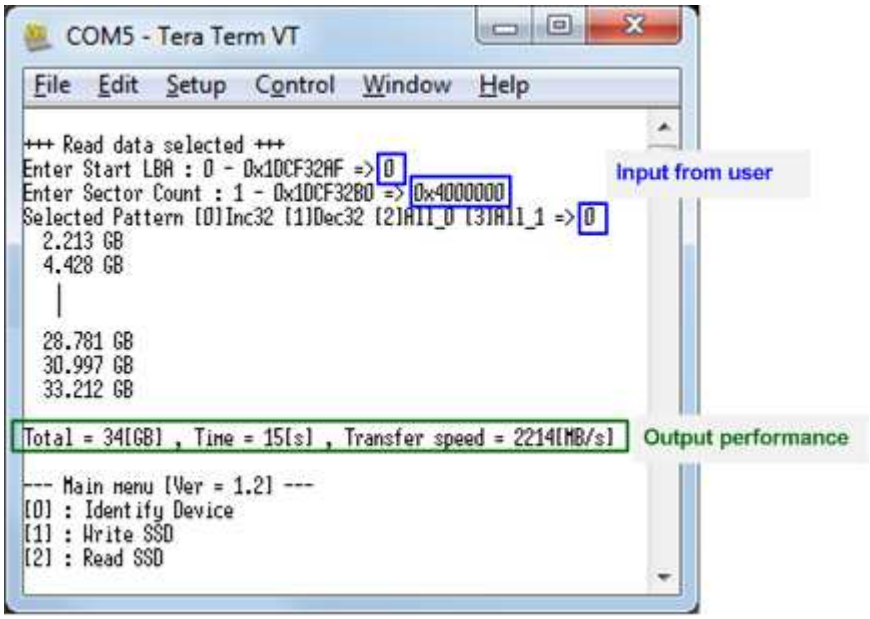

Figure 3-6 Input and result of Read SSD menu

Similar to write test if all inputs are valid, the operation will be started and test performance will be displayed when end of transfer. “Invalid input” will be displayed if any input value is out-of-range.

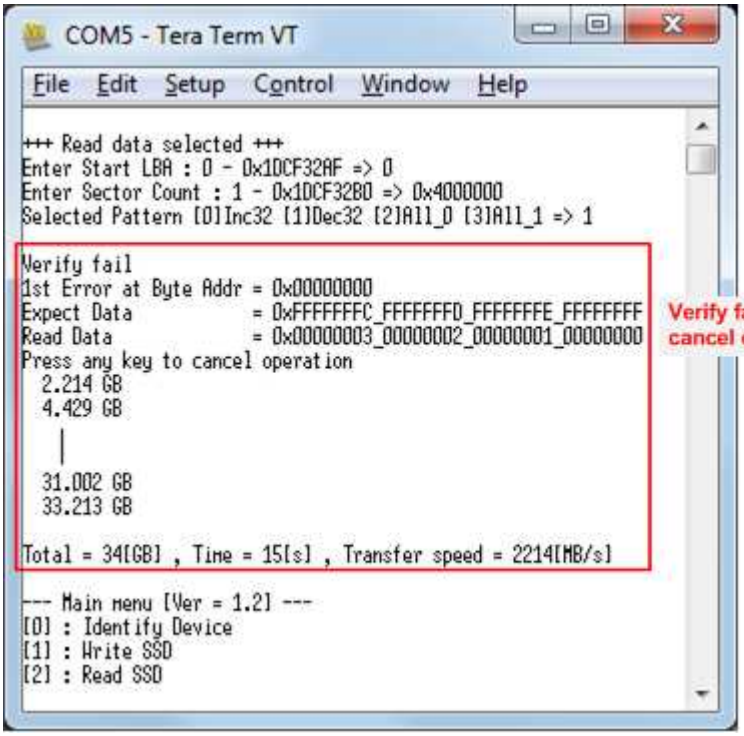

Figure 3-7 Data verification is failed, but wait until read complete

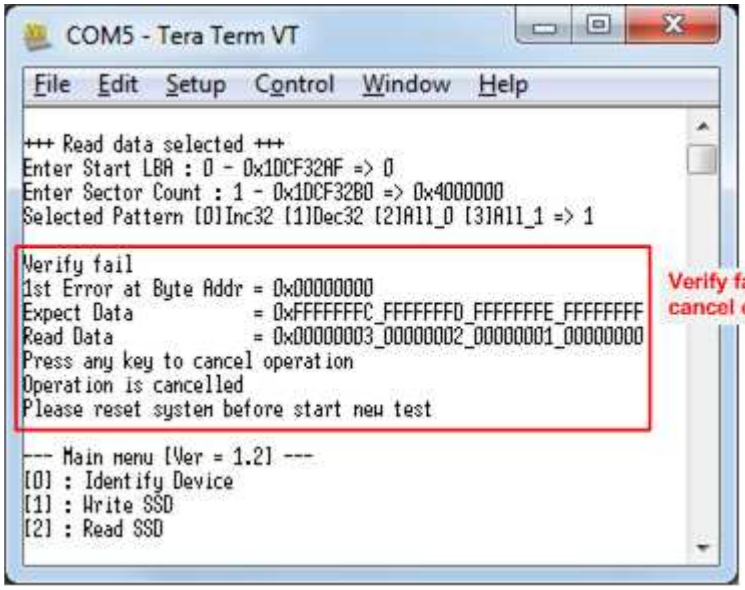

Figure 3-8 Data verification is failed, and press key to cancel operation

Figure 3-7 and Figure 3-8 shows the error message when data verification is failed. “Verify fail” message will be displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete. “RESET” button should be pressed to restart the system when user cancel the operation.

4 Revision History

Revision	Date	Description
1.0	25-Sep-15	Initial version release
1.1	17-Feb-16	Support KCU105 board
1.2	1-Mar-16	Add PCIe speed information
1.3	21-Oct-16	Support AC701 board