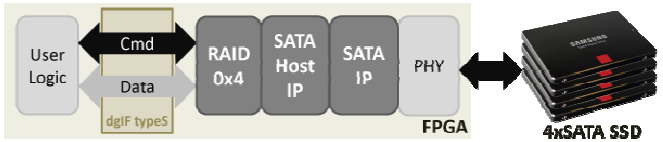
Design Gateway

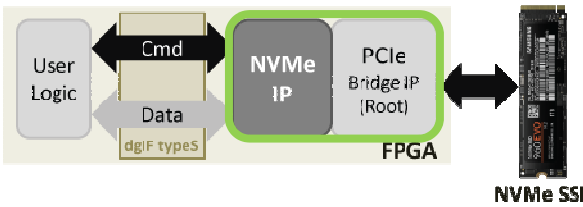
Storage and network IP core

Design Gateway Co., Ltd. is Certified Xilinx Alliance Program Member, specializes in IP cores for high performance and low resources usage solutions in data storage, networking and interface fields on FPGA. Providing various kind of reference design, ready for real board evaluation and experience technology background for supporting customer.



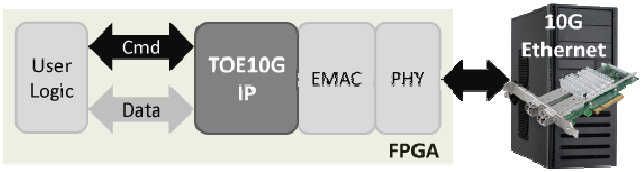
SATA-IP

Feature: SATA Core for SATA Rev3.0 protocol to transfer data with SATA-III SSD or PC.
System Integration: Optional Core for App layer/Transport layer by SATA Host-IP, AHCI-IP
Physical layer by GTH/GTX/GTP transceiver
Speed: 520 - 540 Mbyte/sec per channel
Supported Board: Demo on KCU105, ZC706, mini-ITX, VC709, VC707, KC705, AC701



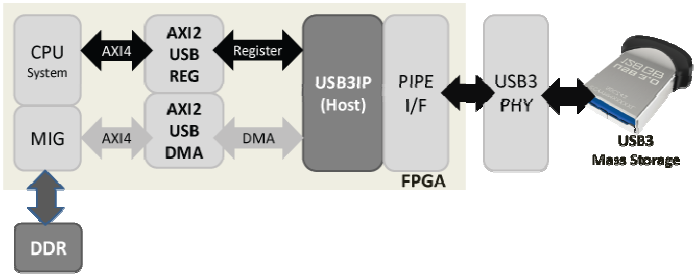
NVMe-IP

Feature: Application layer IP to transfer data with NVMe PCIe SSD.
System Integration : Lower layer by PCIe IP from Xilinx
Speed: 3200 Mbyte/sec for 4-lane Gen3 PCIe SSD
Supported Board: Demo on KCU105, ZC706, mini-ITX, VC709, VC707, KC705



TOE10G-IP

Feature: TCP offload engine with built-in TCP/IP stack for high-speed TCP/IP transfer without CPU
System Integration : Lower layer by Xilinx 10G EMAC and PCS/PMA IP
Speed: 1140 - 1170 Mbyte/sec
Supported Board: Demo on KCU105, ZC706, VC707, KC705



USB3-IP

Feature: USB Core for USB 3.0 protocol to transfer data with USB 3.0 device or PC
System Integration Upper protocol layer by CPU
Physical layer by external PHY IC
Speed: 330 - 350 Mbyte/sec on Device demo
Supported Board: Demo on ZC706, KC705, ML605, SP605