Ultimate IP cores
for Storage & Networking Solution

FPGA Design Solutions Network
intel®
Platinum

DesignGateway is the Platinum Partner of Intel® FPGA Design Solution Network

Features of Gigabit IP core series

■ **Ultimate IP**
High performance, High reliability,
Compact resource, Simple user interface

■ **Support the Latest Devices**

■ **Ready to Evaluate on Real FPGA Boards**
Able to evaluate IP core performance before purchasing
and watch performance demo on Youtube

■ **Reference Design Attached with IP core License**
Able to start development from the design bit by bit
to shorten time and reliable development

■ **Rich Technical Documents**
All technical information are available on official website

IP core Security & Configuration

FPGA logic Security System

High-speed
FPGA configuration module

IP Lock

SD LINK

DESIGN GATEWAY COMPANY LIMITED

NVMe IP core

Directly connect PCIe SSD without external memory!!

32G bps Gen3 x 4Lane

**NVMe IP core** interfaces Ultra high-speed PCIe SSD without CPU and external memory. It is the best solution for applications which require ultra high-speed performance with compact system. The IP core license includes the reference design for Intel FPGA boards to shorten development time and reduce the cost.

Free evaluation sof files for Intel FPGA boards are available. You can evaluate IP core performance before purchasing.

Evaluation on Intel® Arria® 10 SX FPGA Development Kit with Intel® NVMe PCIe SSD

Block diagram
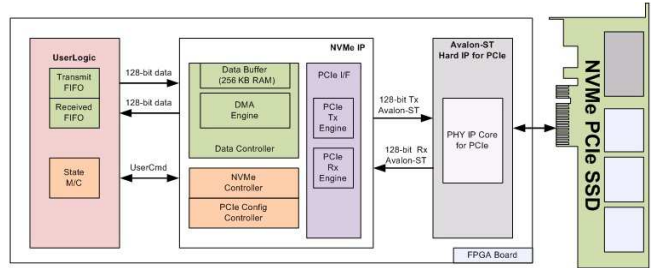
Features

- **Implement application layer to access PCIe SSD without CPU and external memory**

- **Support PCIe Gen3**, theoretical upper limit 4GB/sec

- **Small** resource, the best solution for building a compact system

- **FAT32** access without CPU * with optional FAT32-IP

- **Free evaluation before purchasing**

Reference Designs are available for practical applications
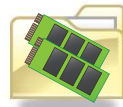
2ch RAID

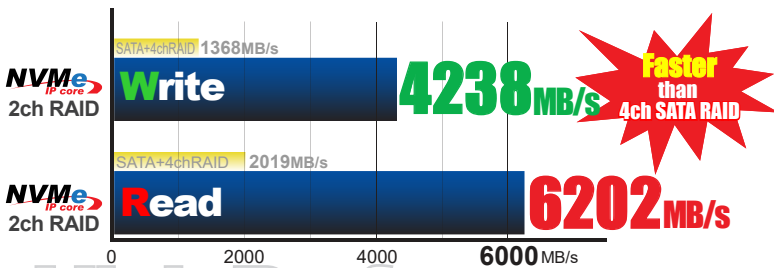Easy to apply for high-end products such as ultra high-speed data recorder

Linux driver

Suitable for high-speed data recording and stand-alone data analysis on SoC

Performance / Application

Able to build Gen3 PCIe SSD 2ch RAID system!!

NVMe 2ch RAID
SATA+4chRAID 1368MB/s
Write 4238 MB/s

Faster than 4ch SATA RAID

NVMe 2ch RAID
SATA+4chRAID 2019MB/s
Read 6202 MB/s

0   2000   4000   6000 MB/s

* SATA IP with Plextor PX-256M5S 4pcs
* NVMe IP with Samsung 960Pro 2pcs

The best solution for Compact Ultra High-speed storage system!!

19mm
80mm
19mm

Intel Arria 10 FPGA+SoC
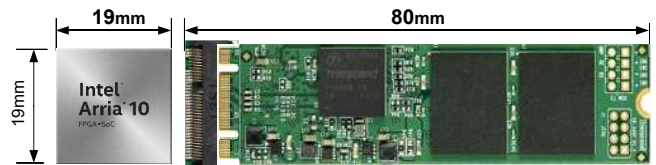
Arria® 10 SX(UBGA484)
NVMe IP + user logic

M.2 SSD
for data storage

System space image by 484pin UBGA package FPGA with M.2 SSD

Product Line up

IP core

NVMe-IP-A10SX	1 project Netlist License for **Arria® 10 SX**	PCIe Gen3
NVMe-IP-A10GX	1 project Netlist License for **Arria® 10 GX**	PCIe Gen3
NVMe-IP-A5GX	1 project Netlist License for **Arria® V GX**	
NVMe-IP-FAT32-A	**FAT32 file system** for NVMe-IP. Purchase with NVMe-IP core	

Please ask us about Multi-License, Evaluation License and Maintenance support License.
For more detail and technical information on our web site http://www.dgway.com/NVMe-IP_A_E.html

Accessories for evaluation

AB16-PCIeXOVER	PCIe Crossover Adapter board for NVMe IP evaluation	
AB17-M2FMC	M.2-FMC adapter board for NVMe-IP evaluation Able to connect 2 NVMe SSDs. * SSD is not included.	

You Tube Designgateway IP core 検索

IP core Evaluation Demo are available on youtube

Design Gateway Co.,Ltd.

SATA IP
Serial ATA Transport&Link Layer IP Core

6G bps

high-reliability & high-performance IP core proven by NASA!!

SATA IP core provides link layer to implement SATA channel to Intel® FPGAs. It supports SATA3 (6Gbps) and matches with SATA3 SSDs. It can connect with SSD/HDD without external PHY chip. The IP core license includes the reference design for Intel® FPGA boards to shorten development time and reduce the cost.
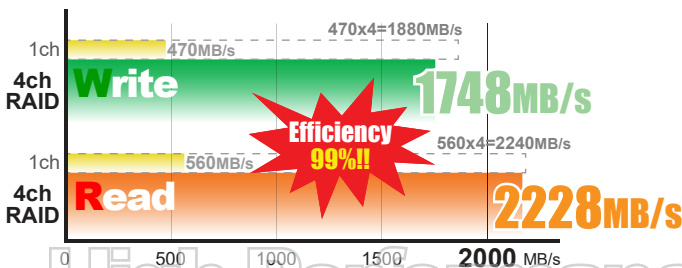
Block diagram

NIOSII	Avalon2SATA	SATA-IP	SATA2PHY	
CPU	Avalon Bus / TX FIFO / RX FIFO	FIS Packet / FIS I/F / RX Elastic Buffer / CRC / Scrambler / Descrambler	16-bit Data / ALTGX & ALT_RECONFIG / PHYRstCtrl / OOBControl	SATA-II/III HDD/SSD
Application Layer	Transport Layer (Reference Design)	Link Layer (IP core)	PHY Layer (Reference Design)	

Evaluation on Intel®Arria® 10 SX FPGA Dev. Kit with AB09-FMCRAID + SATA3 SSD x 4ch RAID

Features

- **Compliant with SATA 3.0 6Gbps**
- **Support both Host and Device**
- **AHCI** for Linux boot up from SoC devices
- **FAT32** access without CPU
  * with optional HCTL-IP and FAT32-IP
- **Free evaluation before purchasing**
  IP core Evaluation Demo are available on youtube
- **Reference Design is contained with IP core license**

Enhanced development support

Project Design of Evaluation sof file
bundled with IP core!!
All Source code except IP core

Confirm core operation with original reference design
Modify a little to approach final user product.
Check real operation in each modification step

Completed!!
No risk to back to rebuild, able to develop for **short term** !

Suitable for RAID System

High-Efficiency Loss less RAID system !!

1ch 470MB/s
4ch RAID **Write** 470x4=1880MB/s **1748MB/s**
Efficiency 99%!!
1ch 560MB/s
4ch RAID **Read** 560x4=2240MB/s **2228MB/s**

0   500   1000   1500   **2000** MB/s

IP core Evaluation Demo are available on youtube

You Tube | Designgateway IP core | 検索

Able to build RAID system by Small Resource !!

Fitter Resource Utilization by Entity

Compilation Hierarchy Node		ALMs needed [=A-B+C]
|nios_sata3		12960.0 (4.9)
|qsys:u0		11766.3 (0.0)
|MMMt2SATA128:mmmt2sata128_0|		1738.6 (276.2)
|sata_lt_ll:u_SATAIP|	ch0	1350.7 (0.9)
|MMMt2SATA128:mmmt2sata128_1|		1685.1 (253.3)
|sata_lt_ll:u_SATAIP|	ch1	1321.0 (1.0)
|MMMt2SATA128:mmmt2sata128_2|		1694.3 (255.2)
|sata_lt_ll:u_SATAIP|	ch2	1328.0 (1.0)
|MMMt2SATA128:mmmt2sata128_3|		1706.1 (253.3)
|sata_lt_ll:u_SATAIP|	ch3	1342.1 (1.0)
|sata3phy:u_sata3phy|		1099.6 (0.0)
|OOBComCtrl:\u_CHO_3:0:u_OOBComCtrl0|		18.5 (18.5)
|OOBComCtrl:\u_CHO_3:1:u_OOBComCtrl0|		17.4 (17.4)

Compact

Only 1321 ALMs !!
ALMs per channel
ALMs for PHY part (4ch)

On Arria® V GX (5AGXFB3H4F, ALMs=136,880), the recource usage for 1 channel (SATA-IP + Avalon Bridge + PHY) is,, **Only 1%!!**

High Performance

Product Line up

IP core

SATA-IP-S5GX	1 project Netlist License for **Stratix® V GX**
SATA-IP-S4GX	1 project Netlist License for **Stratix® IV GX**
SATA-IP-A10SX	1 project Netlist License for **Arria® 10 SX**
SATA-IP-A5ST	1 project Netlist License for **Arria® V ST**
SATA-IP-A5GX	1 project Netlist License for **Arria® V GX**
SATA-IP-C5SX	1 project Netlist License for **Cyclone® V SX**

Additional Option

SATA-IP-HCTL-A	**HOST IP** for SATA-IP. Purchase with SATA-IP core
SATA-IP-AHCI-A	**AHCI function for LinuxOS**. Purchase with SATA-IP core
SATA-IP-FAT32-A	**FAT32 file system** for SATA-IP. Purchase with SATA-IP core
SATA-IP-exFAT-A	**exFAT file system** for SATA-IP. Purchase with SATA-IP core
AB09-FMCRAID	FMC-SATA(10ch) adapter board for SATA-IP evaluation
AB12-HSMCRAID	HSMC-SATA(8ch) adapter board for SATA-IP evaluation

For more detail and technical information on our web site www.dgway.com/SATA-IP_A_E.html

Please ask us about Multi-License, Evaluation License and Maintenance support License.
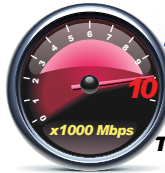
TOE 10G IP core
TCP Offloading Engine IP Core

10GbE TCP/IP Stack Implementation by All HW Logic without CPU

10G bit Ether

10GbE TCP Off-loading Engine(TOE10G-IP) IP core is the epochal solution implemented without CPU. Generally, TCP processing is so complicated that expensive high-end CPU is required. TOE10G-IP built by pure hardwired logic can take place of such extra CPU for TCP protocol management. This IP product includes reference design which helps you to reduce development time. DesignGateway provide demo binary file for Intel®FPGA boards. You can evaluate TOE10G-IP core on real board before purchasing.
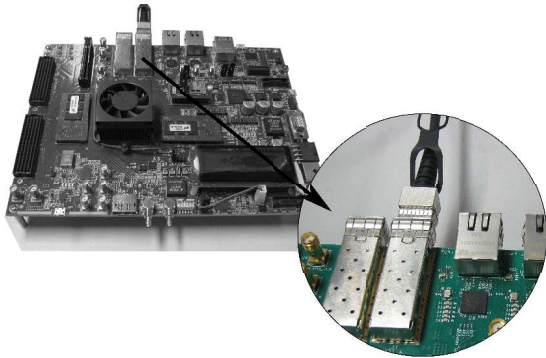
Block diagram
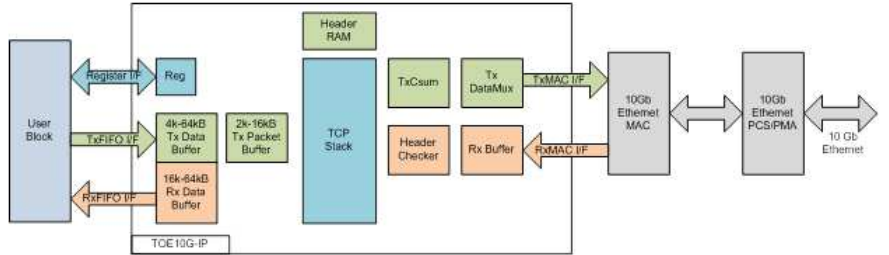
Free evaluation on Intel®Arria® 10 SX FPGA Dev. kit is available **before** purchasing IP core

Features

- **Over 1200MByte/sec** real transfer speed
- Support **Full Duplex**
- Fully hard-wired TCP/IP protocol control to build **CPU-less** network system
- Support Multi-Session
- Free evaluation **before** purchasing

Performance

Transmission — 1238 MB/s
Reception — 1238 MB/s

| 0 | 300 | 600 | 900 | 1200 | 1500 |

for *1Gbit Ethernet*

TOE 1G IP core
TCP Offloading Engine IP Core
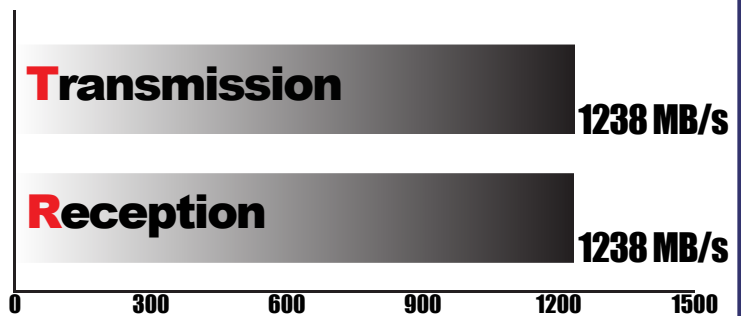
1Gbit TCP Off-loading All Hardware Logic without CPU

Accelerates TCP communications, broadcasting and automotive "ALL-TCP/IP"!!

Product Line up

TOE10G-IP core

TOE10G-IP-A10	1 project Netlist License for **Arria® 10**

For more detail and technical information on our web site www.dgway.com/TOE10G-IP_A_E.html
Please ask us about Multi-License, Evaluation License and Maintenance support License.

TOE1G-IP core

TOE1G-IP-A10	1 project Netlist License for **Arria® 10**
TOE1G-IP-A5	1 project Netlist License for **Arria® V**
TOE1G-IP-S4	1 project Netlist License for **Stratix® IV**

For more detail and technical information on our web site www.dgway.com/TOE1G-IP_A_E.html

You Tube — Designgateway IP core — 検索

IP core Evaluation Demo are available on youtube

UDP 10G IP core
User Datagram Protocol IP Core

UDP 1G IP core
User Datagram Protocol IP Core

Ideal for network applications that require broadcast and low latency!!

- All hardware logic to achive CPU-less system
- Minimum overhead and very low latency
- Support Full Duplex
- Free evaluation before purchasing

UDP10G-IP-A10	1 project Netlist License for **Arria® 10**
UDP1G-IP-A10	1 project Netlist License for **Arria® 10**
UDP1G-IP-A5	1 project Netlist License for **Arria® V**
UDP1G-IP-C5	1 project Netlist License for **Cyclone® V**

For more detail and technical information on our web site
www.dgway.com/UDP10G-IP_A_E.html and www.dgway.com/UDP-IP_A_E.html

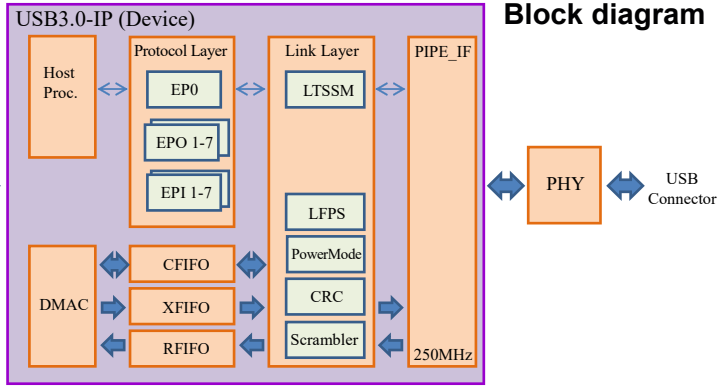## Design Gateway Co.,Ltd.

USB 3.0 IP

Universal Serial Bus 3.0 Host & Device Controller IP Core

Easy to apply to FAT32 Data Recorder System!!

USB3.0 IP core complaints with the USB 3.0 specification Revision1.0. This IP core provides link layer and protocol layer. Physical layer interfaces to PHY chip by TI. Mass storage class reference design for Intel® FPGA board is included in the IP core license. You can start your development from the design step by step and shorten development time and reduce the cost.

Evaluation on Cyclone® IV GX FPGA Dev. kit
with AB08-USB3HSMC

Block diagram

USB3.0-IP (Device)

Host Proc. | Protocol Layer: EP0, EPO 1-7, EPI 1-7 | Link Layer: LTSSM, LFPS, PowerMode, CRC, Scrambler | PIPE_IF

FPGA user logic

DMAC | CFIFO | XFIFO | RFIFO

PHY — USB Connector

250MHz

Features

Line up both Host & Device

Ready to start Dev. on real board!!
Provide reference design for Intel® FPGA boards

Host IP   FAT32 File access demo

Reference Designs for practical applications

Device IP   FAT32 Data recording demo

- Complaint with USB 3.0 5Gbps
- Support All transmission taps

Reference Designs are available for practical applications

- **FAT32 Data recording Design for USB3.0 Device IP core**

PC recognizes USB device as FAT32 external storage without any driver for Windows or Linux!!

Able to shorten development time for high-speed data recoeding/analysis system!!
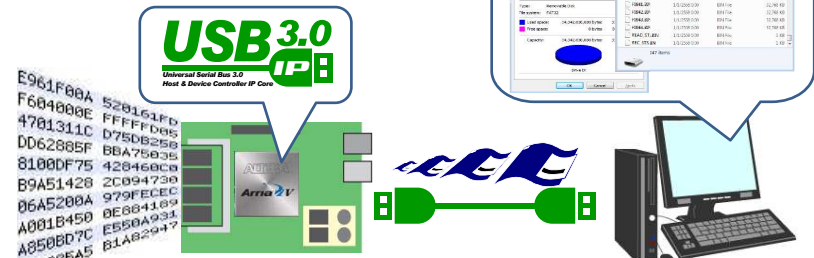
FPGA records data and transfers it through USB3.0.
At PC side, it is recognized as FAT32 files.

No risk to back to rebuild, able to develop for short term !

Product Line up

IP core

USB3H-IP-A5	**Host IP.** 1 project Netlist License for **Arria® V**
USB3H-IP-C5	**Host IP.** 1 project Netlist License for **Cyclone® V**
USB3H-IP-S4	**Host IP.** 1 project Netlist License for **Stratix® IV**
USB3H-IP-C4	**Host IP.** 1 project Netlist License for **Cyclone® IV**
USB3H-IP-A2	**Host IP.** 1 project Netlist License for **Arria® II**
USB3D-IP-A5	**Device IP.** 1 project Netlist License for **Arria® V**
USB3D-IP-C5	**Device IP.** 1 project Netlist License for **Cyclone® V**
USB3D-IP-S4	**Device IP.** 1 project Netlist License for **Stratix® IV**
USB3D-IP-C4	**Device IP.** 1 project Netlist License for **Cyclone® IV**
USB3D-IP-A2	**Device IP.** 1 project Netlist License for **Arria® II**

Accessories for evaluation

AB08-USB3HSMC   **HSMC-USB3.0 adaptor board**
USB3.0 TypeA to A cable (1m) is contained

Please ask us about Multi-License, Evaluation License and Maintenance support License.
For more detail and technical information on our web site www.dgway.com/USB3-IP_A_E.html

You Tube   Designgateway IP core   検索

IP core Evaluation Demo are available on youtube
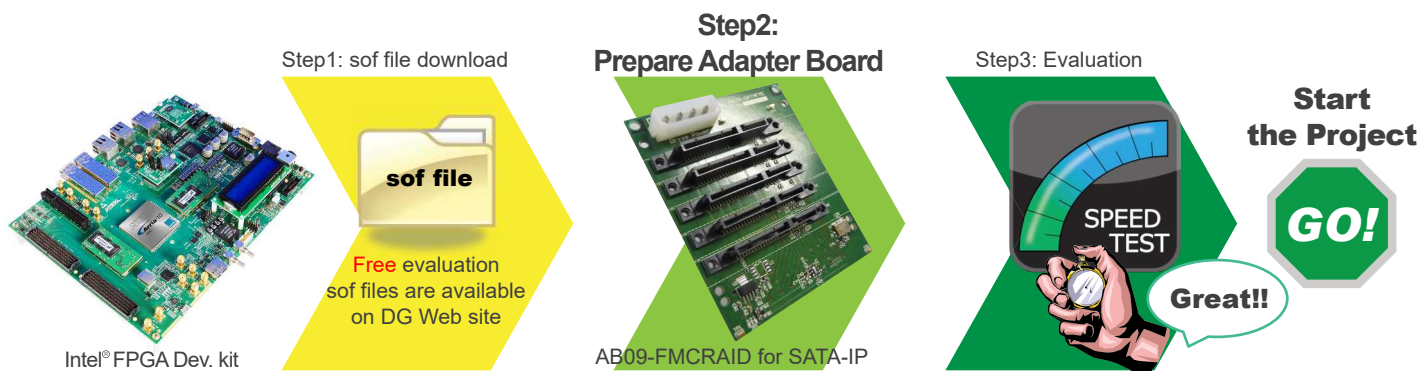
Design Gateway Co.,Ltd.

AB Series

Adapter Boards For IP Core Evaluation

AB Series is Extension Adapter Boards for Gigabit IP core evaluation. AB Series support Intel® FPGA boards. By using AB Series, Gigabit IP cores work on Intel® FPGA boards.
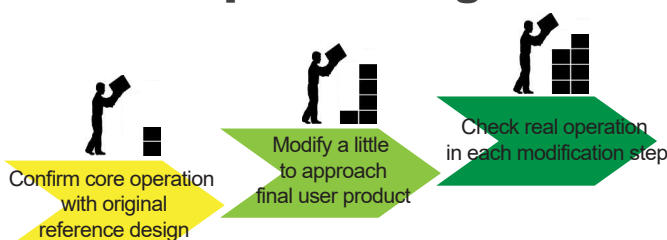
For Evaluation **before** Purchasing

Step1: sof file download

sof file

Free evaluation sof files are available on DG Web site

Intel® FPGA Dev. kit

Step2: Prepare Adapter Board

AB09-FMCRAID for SATA-IP

Step3: Evaluation

SPEED TEST

Great!!

Start the Project

GO!

Easy and Quick Evaluation on Intel® Board with Adapter Board

Able to confirm core operation and make good decision before purchasing !!

For Development **after** purchasing

Reference Design for Intel® FPGA board is **included** in IP core license.,

Confirm core operation with original reference design

Modify a little to approach final user product

Check real operation in each modification step

Completed!!

No risk to back to rebuild, able to develop for **short term** !

E n h a n c e d   d e v e l o p m e n t   s u p p o r t

Product Line up

Part Number	Description	IP core	FPGA Board
AB08-USB3HSMC	**HSMC-USB3.0 adaptor board** USB3.0 TypeA to A cable (1m) is contained	M USB3.0	Intel® Stratix® V GX Stratix® IV GX Arria® 10 SX/GX Arria® V GX Arria® II GX Cyclone® V GX Cyclone® IV GX Development kit ReFLEX CES Alaric Instant-DevKit
AB09-FMCRAID	**FMC-SATA(10ch) adapter board** **for SATA-IP with RAID evaluation**	M SATA IP	
AB12-HSMCRAID	**HSMC-SATA(8ch) adapter board** **for SATA-IP with RAID evaluation**	M SATA IP	
AB16-PCIeXOVER	**PCIe Crossover Adapter board for NVMe-IP evaluation**	M NVMe IP core	
AB17-M2FMC	**M.2-FMC adapter board for NVMe-IP evaluation.** **Able to connect 2 NVMe SSDs.** * SSD is not included.	M NVMe IP core	

M **Purchasing available on Mouser**

For more detail and technical information on our web site http://www.dgway.com/ABseries_E.html

AB-LF-V2.3EA

Design Gateway Co.,Ltd.

IPLock

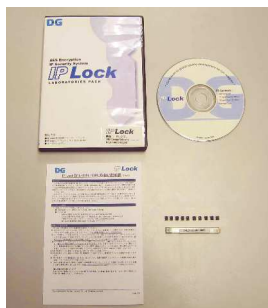## Protect Intellectual Property from illegal copy

AES 128

IPLock is FPGA logic security system which used very reliable AES encryption technology. IP properties in FPGA are protected from illegal copy by only including IP Lock in FPGA and connecting with encryption controller chip.

Features

- **Strong security by AES-128 encryption**
- **Change & encrypt true random authentication data**
- **Immediately stop user logic without the chip**
- **Just 2 line connection between FPGA and IP Lock**
- **Laboratories Pack for prototype, already written unique ID**
- **Writer Set & Blank Encryption chip for mass production**

Compile your FPGA user logic with IPLock core

IP Lock

FPGA

Place IPLock security chip on your FPGA board

Laboratories Pack for prototype

Contents of Laboratories pack. Encryption chips unique ID inside

Laboratories Pack contains encryption chips which are already written unique ID at shipment by Design Gateway. No one can rewrite this fixed ID key. To avoid duplication, each Laboratories pack have different unique ID key, so user must use IP Lock core with encryption chips in same package. Design Gateway provide encryption chip 10 pcs package (IPL-010L) and 30 pcs package (IPL-030L). This product is suitable for prototype and small lot usage.

IPL-010L	IP core netlist + encryption controller chip (unique ID inside) 10pcs pack
IPL-030L	IP core netlist + encryption controller chip (unique ID inside) 30pcs pack

Writer Set for mass production

IPLock Writer and IPL-CHP

Writer pack is suitable for mass production. User can write any ID key to blank encryption chip by using IP Lock write. User can set and write optional ID key for each products or lot. Writer pack contains blank chip 3 pcs. For mass production, The Writer pack is used with Blank Chip

You Tube Designgateway IPlock 検索
IPLock Demo is available on youtube

IPL-003WR	IPLock Writer, IPLick core + IPL-CHP 3pcs (Blank Encryption chip)
IPL-CHP	Blank Encryption chip for IPL-003WR (MOQ 100pcs)

Easy to protect your IP core & logic data !

Step1: Prepare SOIC-8 pattern for security chip on your board

Step2: purchase IPLock for FPGA logic protection

Step3: Compile your FPGA logic with IPLock core

Step4: Put IPLock security chip on FPGA board

Step5: Complete IP core protection!

Protected!!

M **Purchasing available on Mouser**

For more detail and technical information on our web site http://www.dgway.com/IPLock_E.html

Design Gateway Co.,Ltd.

SD LINK

Convenient and High-Speed Configuration Module via microSD
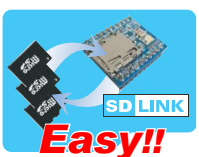
SDHC microSD bundled

3sec!! Ultra High-Speed Programming!!

Just 3 second to program 20MBytes (=160Mbit) configuration data.
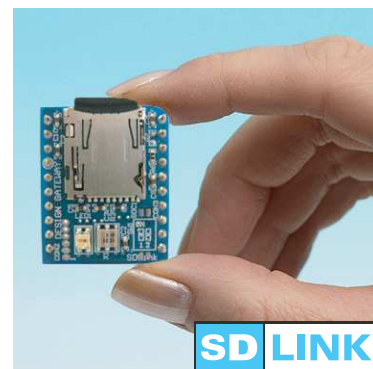(comparison with on board flash, it takes about 7 minutes...)

8 FPGAs!! Only one SDLink can configure up to 8 FPGAs at same time.

Just swap microSD to update & change circuit data immediately!!

Easy!! Convenient update without Programming tools, Download cable and System suspended.

SDLink is a high speed FPGA configuration module which stores data on microSD card. FPGA configuration data is easily updated by just swapping microSD card.
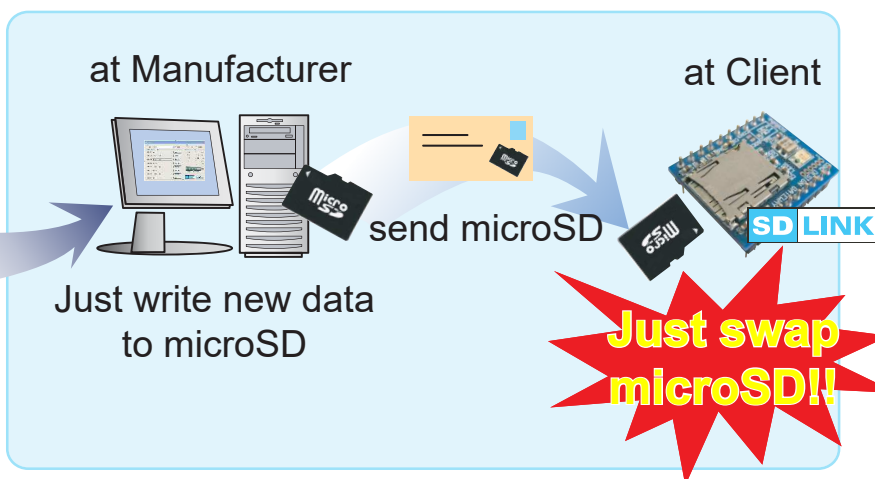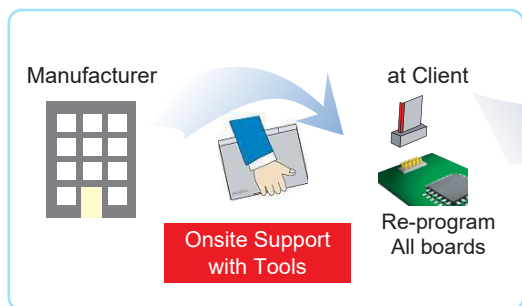
High-Capacity
High-Speed Configuration   Convenient field update
Tool free   High-Speed Programming   Easy to swap

Practical example

Re-programming or update after releasing product

Normal case

Manufacturer → at Client

Onsite Support with Tools

Re-program All boards

In case of SD LINK

at Manufacturer

Just write new data to microSD

send microSD

at Client

SD LINK

Just swap microSD!!

Product Line up

| SL001 | SDHC microSD 1pc bundled | **M** Purchasing available on Mouser |

For more detail and technical information on our web site http://www.dgway.com/SDLink_E.html

You Tube | Designgateway SDLink | 検索

SDLink Demo is available on youtube

IP-LF-V2.3EA