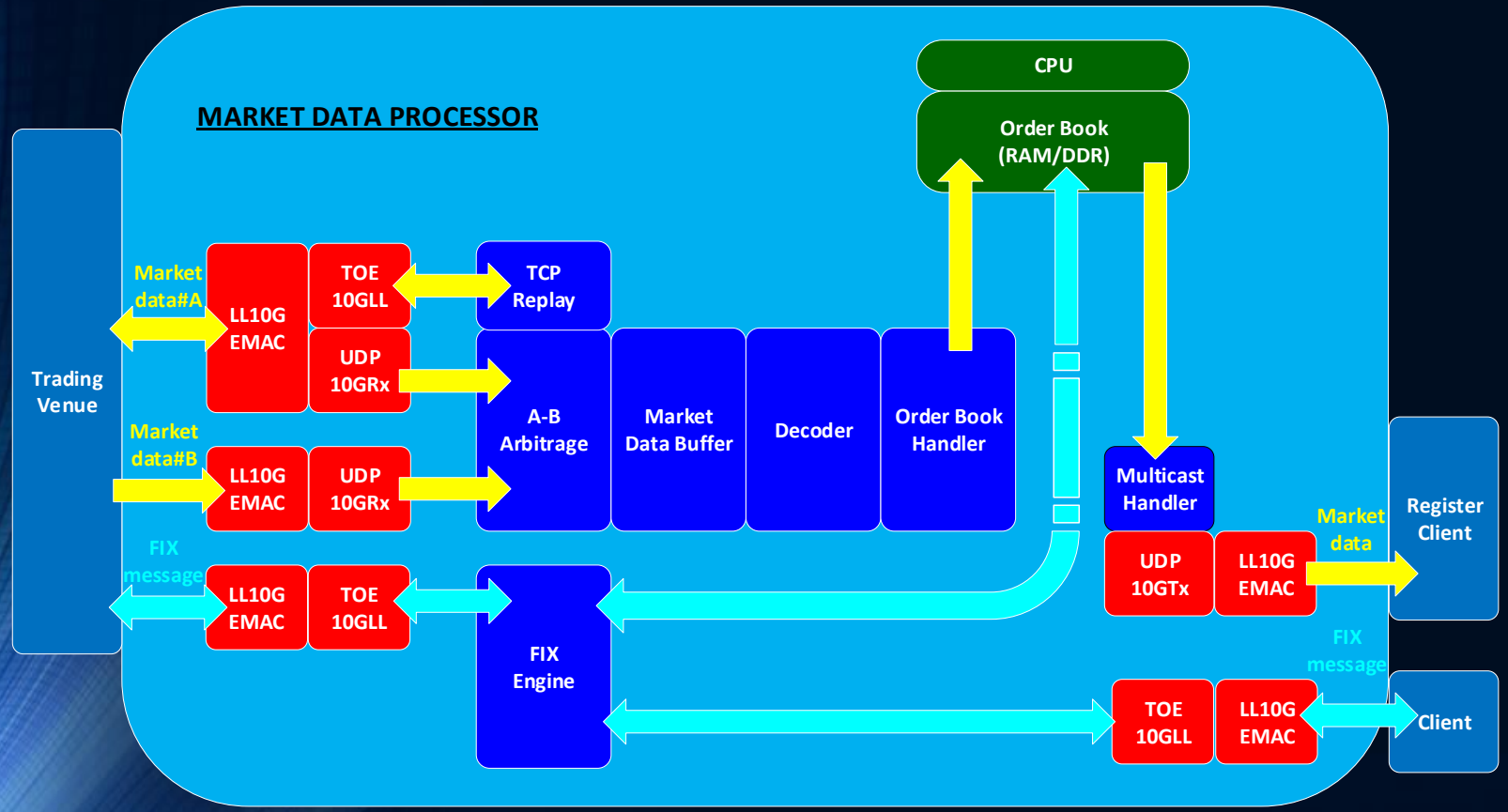
Super Low Latency Networking IP for Fintech

DG's Low Latency Networking IP

- ✓ **Highly integrated and optimized**
  - Design from scratch, tightly integrated with FPGA transceiver
- ✓ **Suitable for Fintech Application**
  - HFT, Market Data Processing, Tick-To-Trade systems
- ✓ **Total solutions for FPGA & Accelerator**
  - 10G EMAC + UDP + TOE IP available with demo

Example FinTech Implementation on FPGA

Market Data Processor is possible to implement on Intel FPGA device to shorten low latency and very fast response to Market data transactions.



DG's related IP Cores

- LL 10GEMAC IP
- UDP10GRx-IP
- UDP10GTx-IP
- TOE10GLL-IP

DG's customization services

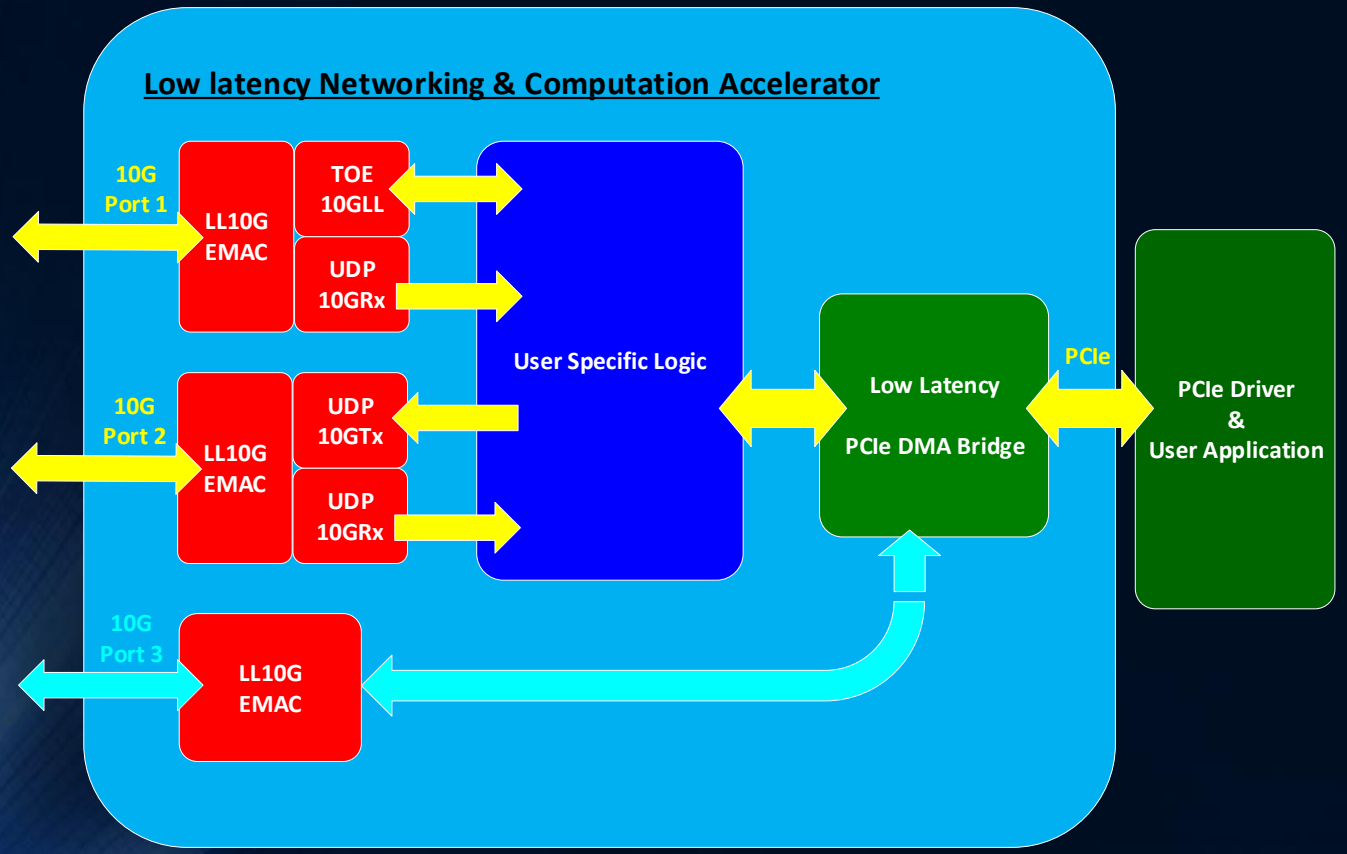
- User logic and IP cores interface implementation based on customer requirements
- High layer protocol handling by pure hardware logic such as
  - *FIX/FAST Encoder/Decoder*
  - *Trade/Order Handler on FPGA*

Customer own development

- Algorithm/ User Application

Example Application for Intel FPGA Accelerator Card

Our low latency Networking IP can support Intel FPGA device on Accelerator Card such as Arria 10 and Agilex.
We can provide FPGA logic customization support for customer's specific application & requirements.



DG's related IP Cores

- LL 10GEMAC IP
- UDP10GRx-IP
- UDP10GTx-IP
- TOE10GLL-IP

DG's customization services

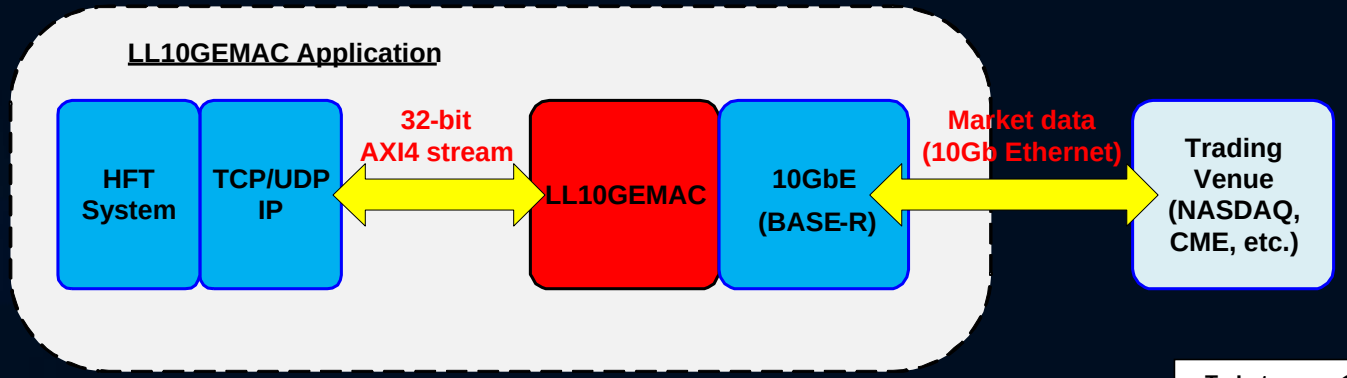
- User logic and IP cores interface implementation based on customer requirements
- High layer protocol handling by pure hardware logic

Customer own development

- PCIe Driver for Host OS
- Algorithm/ User Application

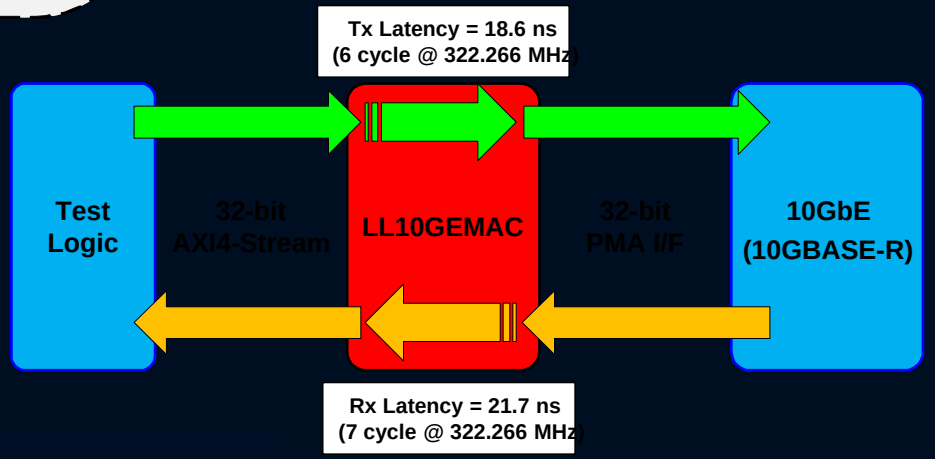
LL 10GEMAC-IP

Designed for low latency networking application such as
HFT, Market Data Processing, Tick-To-Trade systems



Features

- TX Latency: 18.6ns (32bit, 6 cycles @ 322.265625MHz)
- RX Latency: 21.7ns (7 cycles @ 322.265625MHz)
- Compare with Intel 10G Ethernet Subsystem (MAC + PCS)
  - Lower latency
  - Lower FPGA resource usages
  - Lower cost



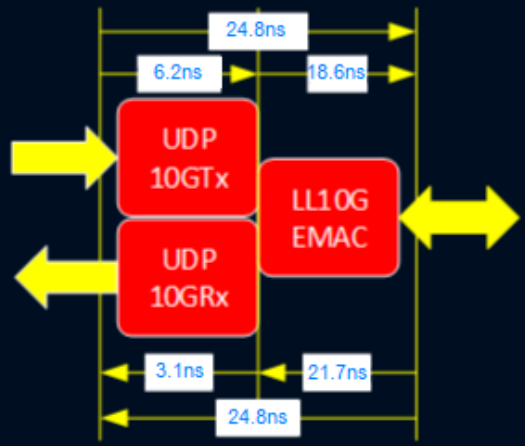
Best fit for DG's Low Latency Networking IP Cores
https://dgway.com/Lowlatency-IP_A_E.html

✓ **Round-trip latency < 70ns!**

DG's Low Latency UDP10G Rx/Tx-IP

UDP10G Rx/Tx-IP Features

- Unicast/Multicast support
- Support 4 sessions (More sessions can be customized)
- Direct connection with DG's LL 10GEMAC-IP
- Join/Leave group by IGMPv2 protocol
- CPU less and no external memory required
- HDL design for minimized resource and latency
- Estimated Rx Latency: 3.1 ns
- Estimated Tx Latency: 6.2 ns (packet size < 45 bytes)*, *measured from the last data received from user and the first data sent to EMAC, @ 322.265625MHz*

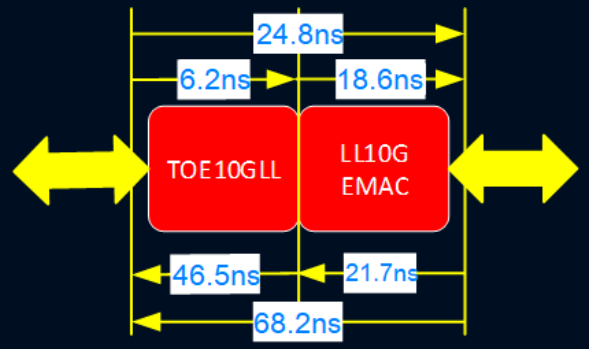


*RX Latency from EMAC input to IP output : 24.8 ns
*TX Latency from IP input to EMAC output : ~24.8 ns
* The latency does not include 10GBASE-R IP latency

DG's Low Latency TOE10G-IP

TOE10GLL-IP Features

- Support 1 session (More sessions can be customized)
- Direct connection with DG's LL 10GEMAC-IP
- CPU less and no external memory required
- HDL design for minimized resource and latency
- Estimated Rx Latency: 46.5 ns
- Estimated Tx Latency: 6.2 ns (packet size < 45 bytes),
  measured from the last data received from user and the first data sent to EMAC, @ 322.265625 MHz



*RX Latency from EMAC input to IP output : 68.2ns
* TX Latency from IP input to EMAC output : 24.8ns
* The latency does not include 10GBASE-R IP latency

Intel FPGA device family support

- Device family: Arria 10, Stratix 10 and Agilex device
- Transceiver: Intel 10BASE-R Transceiver PHY
- Recommended device speed grade: -1
- Example support FPGA device
  - 10AX115S2F45I1SG (Tested on Intel Arria 10 GX board)

Contact

Design Gateway Co., Ltd.

89/13 Amornpan 205 Building Tower1,

Ratchadapisek 7 Alley (Nathong),

Din Daeng, Bangkok, 10400, Thailand

Tel : +66(2)-1034327

URL: http://www.design-gateway.com

Email: ip-sales@design-gateway.com