

1	Test environment setup	1
2	Revision History	5

# FPGA Setup for LL10GEMAC-IP Loopback Test

Rev1.0 30-Jun-23

This document describes how to setup FPGA board and prepare the test environment for running LL10GEMAC-IP loopback demo for measuring the latency time. User sets test parameter on FPGA board and monitors the hardware status via NiosII command shell. More details of the demo are described as follows.

#### 1 Test environment setup

Before running the test, please prepare following test environment.

- FPGA development board: Arria 10 GX Development Kit
- (Optional) SFP+ Loopback cable for external loopback mode
- micro USB cable for FPGA programming and JTAG UART, connecting between FPGA board and PC.
- QuartusII programmer for programming FPGA and NiosII command shell, installed on PC

<u>Note</u>: The latency time in the test depends on clock phase shift characteristic when the board boots up. Reset button is designed to reset the system which will change clock phase shift characteristic. Therefore, the user can press Reset button and may get the different latency time on the test.



Figure 1-1 LL10EMAC-IP demo on Arria10 GX



The step to setup test environment by using FPGA and PC is described in more details as follows.

- 1) Turn off power switch and connect power supply to FPGA board.
- 2) Connect micro USB cable between FPGA board and PC for FPGA configuration and JTAG UART.





### Figure 1-2 Power and USB connection

- 3) (Optional for running external loopback mode) Plug-in SFP+ Loopback cable.
- 4) Turn on power switch on FPGA board.



- 5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
  - a) Click "Hardware Setup..." to select USB-BlasterII[USB-1].
  - b) Click "Auto Detect" and select FPGA device.
  - c) Select FPGA device icon.
  - d) Click "Change File" button, select SOF file in pop-up window, and click "open" button
  - e) Check "program"
  - f) Click "Start" button to program FPGA
  - g) Wait until Progress status is equal to 100%

Eile Edit View Processing Tools Window Help     Search Intel FPGA     g) Wait until Progress = 100%     a) Click Hardware Setup -> USB-1     g) Wait until Progress = 100%     a) Click Hardware Setup   USB-Blasteril [USB-1]      Mode:        TAG        Progress:     100% (Successful)        Progress:     100% (Successful)        Progress:           Progress:   Progress:   100% (Successful)    Progress:   100% (Successful)      Progress:   100% (Successful)      Progress:   100% (Successful)      Progress:   100% (Successful)      Progress:   100% (Successful)      Progress:   100% (Successful)    Progress: Progress: Progress: Progress: Progress: Progre					
a) Click Hardware Setup -> USB-1   (a) Click Hardware Setup -> USB-1 (b) Wait until Progress = 100% (c) Wait until Progress = 100%					
Enable real-time       f) Click "Start" button         f) Click "Start" button       File         Device       Checksum         Usercode       Program/         Verify       Blank-         Example       D:/Download/LL10GEMACLpTest.sof         10AX115S2F45       307DEC29         Stop       b)         Select FPGA Device       5M2210Z         00000000 <none>         e)       Check "Program"         d)       Click "Change File" button -&gt; Select</none>					
f       Click "Start" button         f       File       Device       Checksum       Usercode       Program/       Verify       Blank-       Exact         Image: Stop       b       D:/Download/LL10GEMACLpTest.sof       10AX115S2F45       307DEC29       307DEC29       Image: Stop					
File       Device       Checksum       Usercode       Program/       Verity       Blank-       Exit         Image: Stop       D:/Download/LL10GEMACLpTest.sof       10AX115S2F45       307DEC29       307DEC29       Image: Check					
D:/Download/LL10GEMACLpTest.sof       10AX115S2F45       307DEC29       307DEC29         b) Select FPGA Device       5M2210Z       00000000 <none>       e) Check "Program"         Click "Change File" button -&gt; Select       00000000       <none>       e) Check "Program"</none></none>					
b) Select FPGA Device 5M22102 00000000 <none> e) Check "Program"</none>					
Delete      d) Click "Change File" button -> Select					
d) Click "Change File" button -> Select					
Mdd File LL10GEMACLpTest.SOF					
Change File c) Select FPGA Device					
E Save File TDI					
Add Device					
10AX11552F45 5M2210Z					
Image: Second state					
Message Message ID					
① Device 1 contains JTAG ID code 0x02E660DD       209017         ① Configuration succeeded 1 device(s) configured       209007					
① Successfully performed operation(s)209011① Ended Programmer operation at Wed Mar 17 16:49:27 2021209061					
St. Curter (7) Processing					
System (7) Processing					

#### Figure 1-3 FPGA Programmer



- 6) On Nios II command shell,
  - a. Type "nios2-terminal".
  - b. Input '0' or '1' to initialize demo in external loopback mode or internal loopback mode.

\$ nios2-terminal	<ul> <li>♦ : User Input</li> <li>♦ : User Output</li> </ul>
nios2-terminal: connected to hardware target using JTAG	UART on cable
nios2-terminal: "USB-BlasterII [USB-1]", device 1, insta	nce 0
nios2-terminal: (Use the IDE stop button or Ctrl-C to te	rminate)
+++ LL10GEMAC Loopback Test [IPVer = 2.0] +++	)' or '1' to select
Input Coopback Mode : [0]External [1]Internal => 0	ck mode

Figure 1-4 Message after system boot-up

c. After User select mode, the system initialization begins. Then, the main menu is displayed on NiosII command shell after the initialization is finished.

Input Loopback Mode : [0]E>	<pre>xternal [1]Internal =&gt; 0</pre>					
Start Reset Reset Complete	Message is displayed when IP initialization					
Ethernet Link Up						
Loopback Test menu [0] : Change Loopback Mode Main Menu [1] : LL10GEMAC Loopback Test						

Figure 1-5 Initialization complete

Note: When running Internal loopback mode, SFP+ Loopback module is not used.



## 2 Revision History

Revision	Date	Description
1.0	26-Mar-21	Initial version release