LL10GEMAC IP Demo Instruction

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Rev1.1 30-Jun-23

1 Overview

This document describes the instruction to run loopback demo on FPGA development board. The demo is designed to run LL10GEMAC IP loopback test for measuring the round-trip latency time. User sets test parameters on FPGA board and monitors the hardware status via console. More details of the demo are described as follows.

2 Test menu

2.1 Change Loopback mode

Select '0' to change loopback mode parameter in the demo.

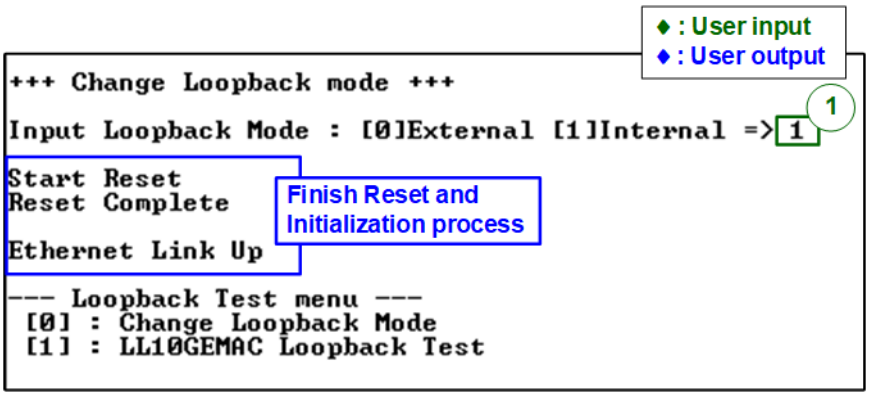

Figure 2-1 Example test result

User can select to run by two modes.
0: External loopback mode by using SFP+ loopback module
1: Internal loopback mode by using Near-End PMA loopback by transceiver

After user selecting, the reset signal is sent to the IP. Finally, "Ethernet Link Up" is shown after IP completes initialization process.

2.2 LL10GEMAC Loopback Test

Select '1' to start the test operation. The example test result when running external loopback and internal loopback test is shown in Figure 2-2.

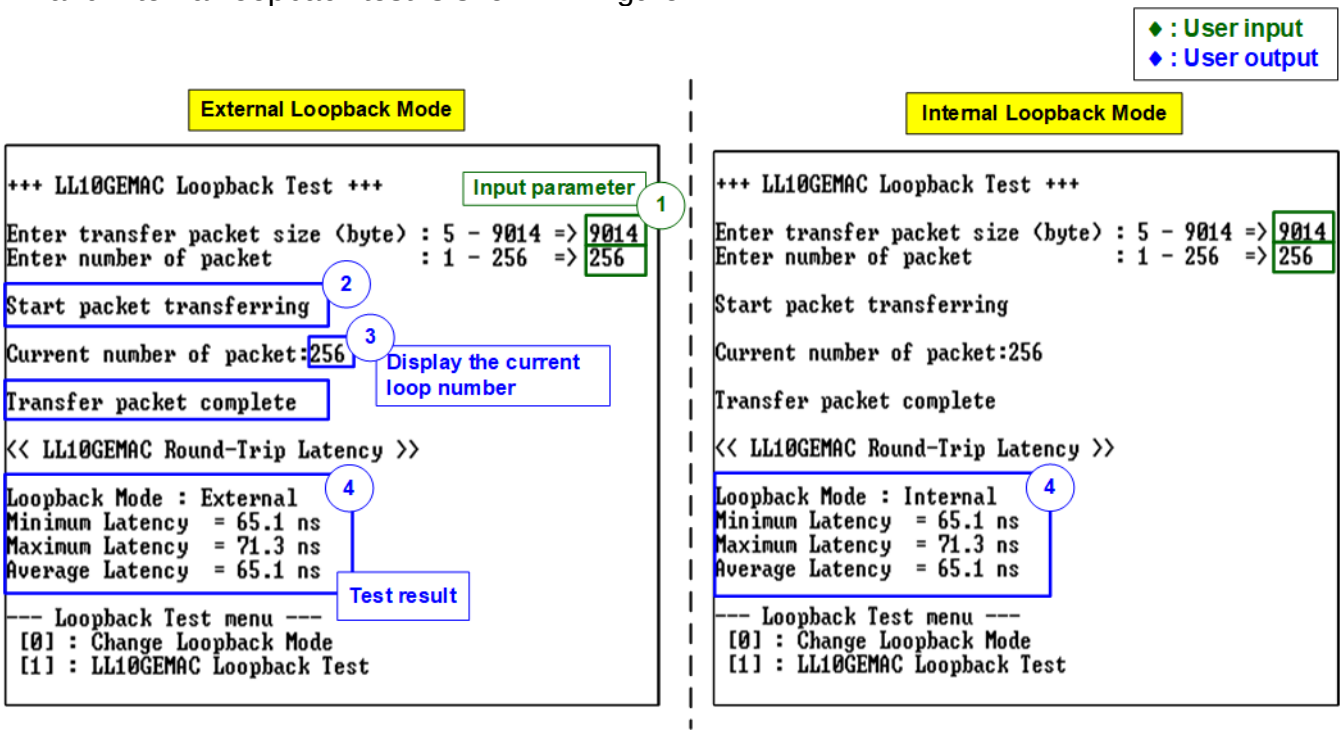

Figure 2-2 Test result when running loopback test

User inputs test parameters for sending packet in the console. The sequence to run the test is shown as follows

1) Input two parameters under loopback test menu
   a) Input packet size: Unit of packet size is byte. Valid value is 5-9014. The input is decimal unit when user inputs only digit number. User can add "0x" to be a prefix for hexadecimal unit
      Note: If the packet size is less than 60 bytes, zero padding is filled by LL10GEMAC-IP
   b) Input number of packets: Valid value is 1-256. The input is decimal unit when user inputs only digit number. User can add "0x" to be a prefix for hexadecimal unit
2) If all inputs are valid, the "Start packet transferring" is displayed on console.
3) During transferring packet, the console displays current number of packets which are completely transferred.
4) After the packet transfer is completed, "Transfer packet complete" is displayed. The latency times are calculated and displayed on console.
   - Minimum latency: the maximum value of round-trip latency time of all tests.
   - Maximum latency: the minimum value of round-trip latency time of all tests.
   - Average latency: the average value of round-trip latency time of all tests.

Note:

- *The latency time is calculated from the clock cycle which is equal to 3.1 ns. The resolution of the result is limited to 3.1 ns. Therefore, the different latency time when running external loopback and internal loopback is equal to 0 ns or 3.1 ns.*
- *The latency time of each test round depends on the characteristic of 64B/66B encoding/decoding and gearbox at running time. When setting to run many rounds, the test shows minimum value, maximum value, and average value to show the statistics of the latency time.*
- *The minimum latency time may show different value when running the test. The transmitted data and received data of EMAC are run in different clock domain. So, the latency time depends on the different phase shift between transmit data clock domain and received data clock domain. As shown in* Figure 2-3*, when the different phase shift of received data is slightly different from transmit data clock, the different latency time of internal loopback and external loopback can be detected. The different value is equal to 3.1 ns which is the resolution of the timer in the demo design. The phase shift is changed when the board is reset by reset button on the board.*

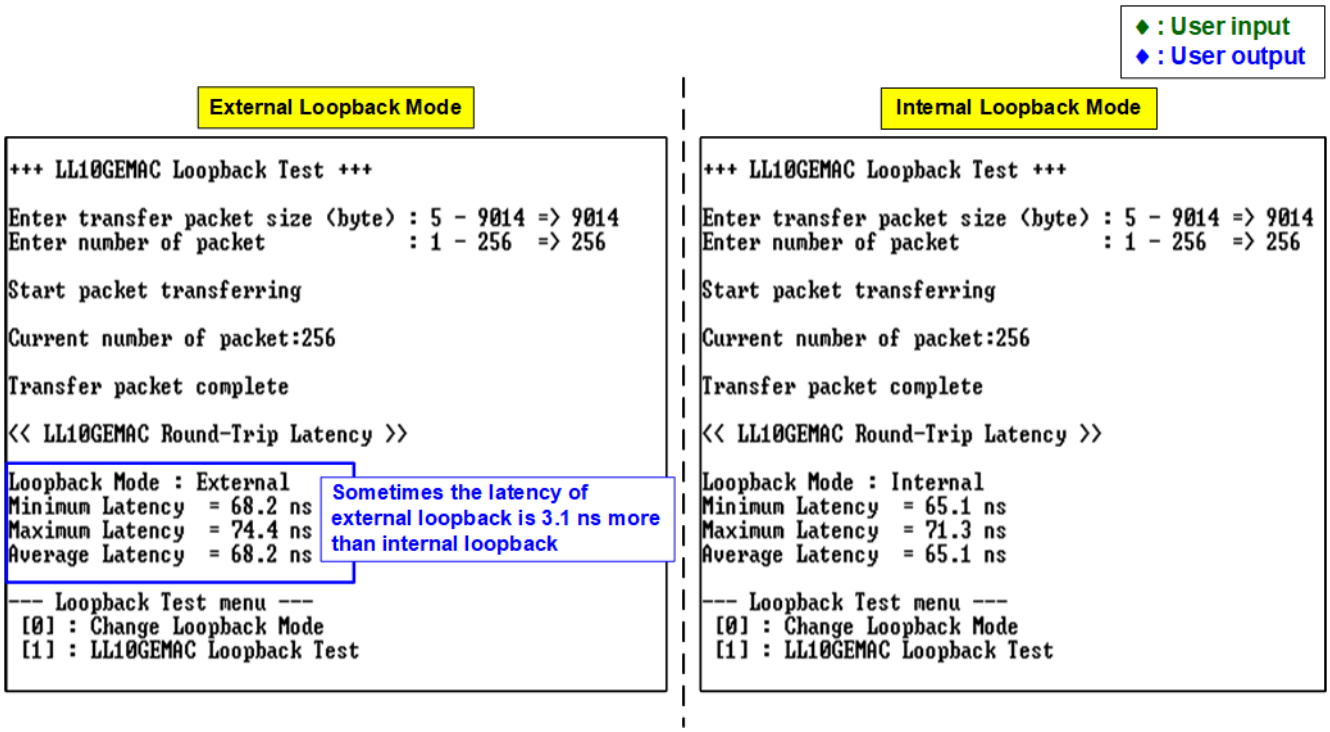

Figure 2-3 Different latency time found when running internal and external loopback

If the input is invalid, “Out-of-range input” is displayed and the operation is cancelled, as shown in Figure 2-4.

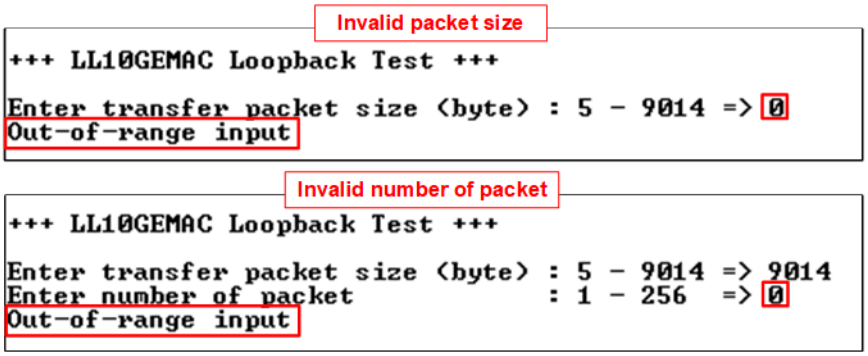

Figure 2-4 Error from invalid input

3 Revision History

Revision	Date	Description
1.0	21-May-20	Initial version release
1.1	29-Apr-21	Remove FPGA setup part and update test menu