FPGA Setup for UDP10GRx-IP demo

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This document describes how to setup FPGA board and prepare the test environment for running UDP10GRx-IP demo. The demo is designed for transferring data from 10G Ethernet card that is installed on TestPC to the FPGA development board. “trans_udp_multi” is test application that is run on TestPC to send UDP packet to the FPGA development board via 1-4 sessions. The hardware including UDP10GRx-IP is designed to receive UDP data with or without data verification. The user interface for controlling the hardware via JTAG UART through NiosII command shell, run on TestPC. More details of the demo are described as follows.

1 Environment Setup

Please prepare following test environment.

1) FPGA development board (Arria10 GX development board)
2) PC with 10 Gigabit Ethernet support or 10 Gigabit Ethernet card
3) 10 Gb Ethernet cable:
   - 10 Gb SFP+ Passive Direct Attach Cable (DAC) which has 1-m or less length
   - 10 Gb SFP+ Active Optical Cable (AOC)
   - 2x10 Gb SFP+ transceivers (10G BASE-R) with optical cable (LC to LC, Multimode)
4) microUSB cable for JTAG connection, connecting between FPGA board and PC
5) “trans_udp_multi.exe” which is test application provided by Design Gateway, prepared on PC
6) QuartusII Programmer and NiosII command shell, installed on PC

Note: Example of test environment is shown as follows.
[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html
[2] 10-Gigabit SFP+ AOC (AOC-S1S1-001)
https://www.10gtek.com/10gsfp+aoc
[3] PC: Motherboard ASUS Z170-K, 32 GB RAM, 64-bit Windows7 OS

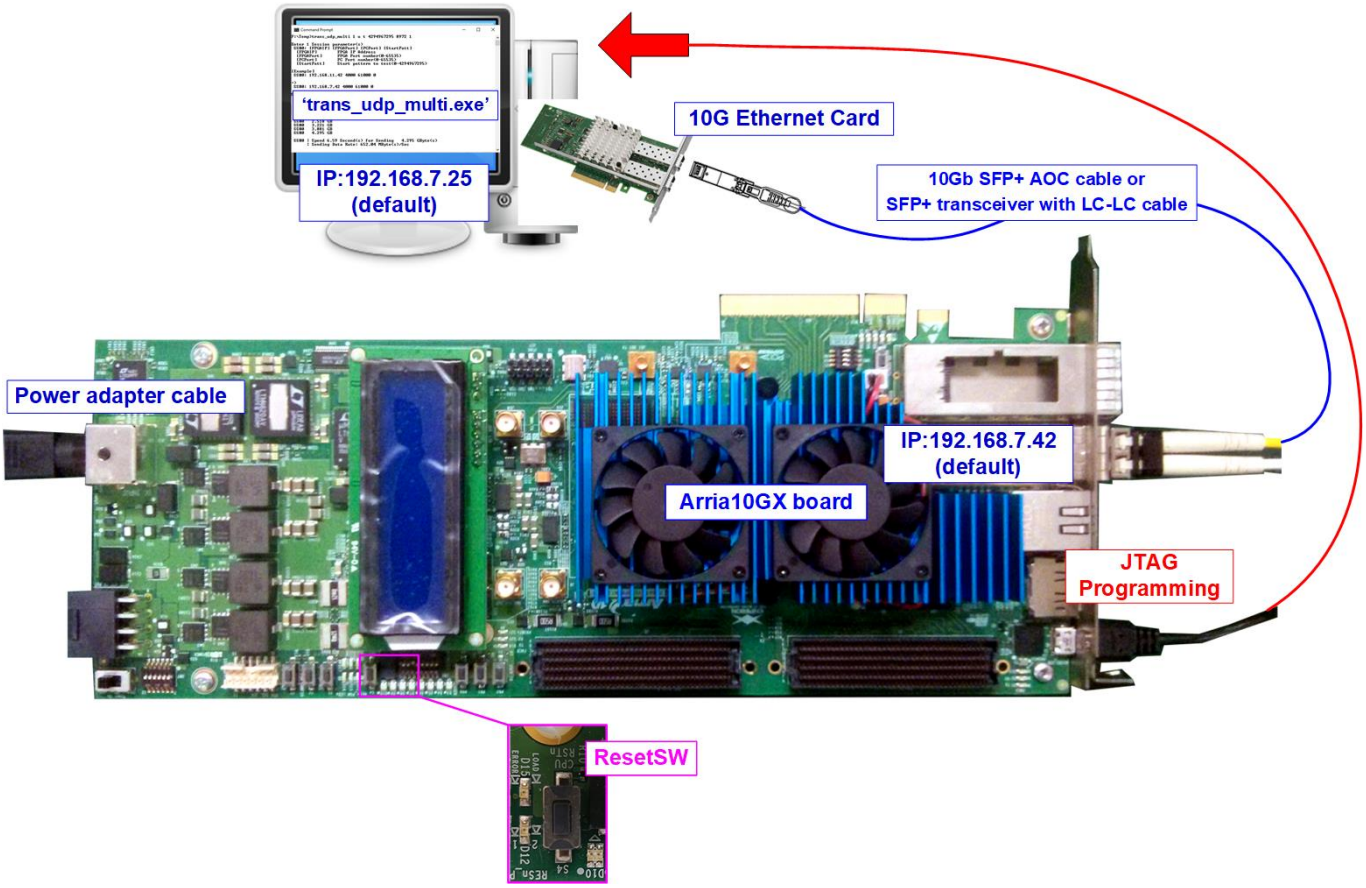

Figure 1-1 UDP10GRx IP demo on Arria10 GX development board

2 FPGA board setup

1) Turn off power switch and connect power supply to FPGA board.
2) Connect micro USB cable between FPGA board and PC for JTAG programming and JTAG UART.
3) Connect 10 Gb Ethernet cable (10 Gb SFP+ DAC (Length<1m), AOC, or SFP+ transceiver with LC-LC cable) between FPGA board and PC.
4) Turn on power switch on FPGA board.
5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
   a. Click “Hardware Setup…” to select USB-BlasterII[USB-1].
   b. Click “Auto Detect” and select FPGA (10AX115S2).
   c. Select Arria10 device icon.
   d. Click “Change File” button, select SOF file in pop-up window, and click “open” button.
   e. Check “program”.
   f. Click “Start” button to program FPGA.
   g. Wait until Progress status is equal to 100%.

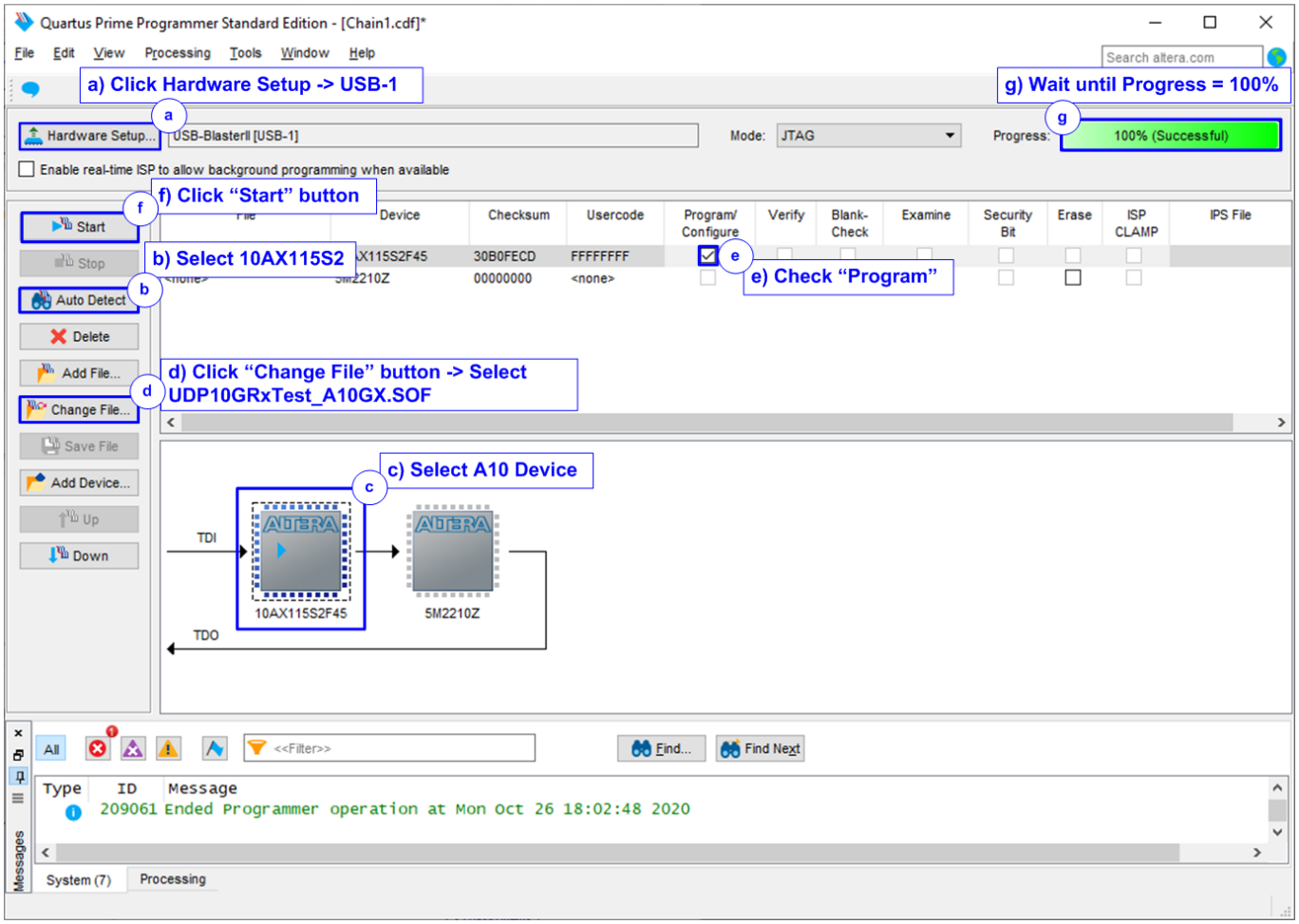

Figure 2-1 FPGA Programmer

6) Open NiosII command shell.
   a. Type “nios2-terminal.exe”, then press enter.
   b. The default parameter is displayed on the console.

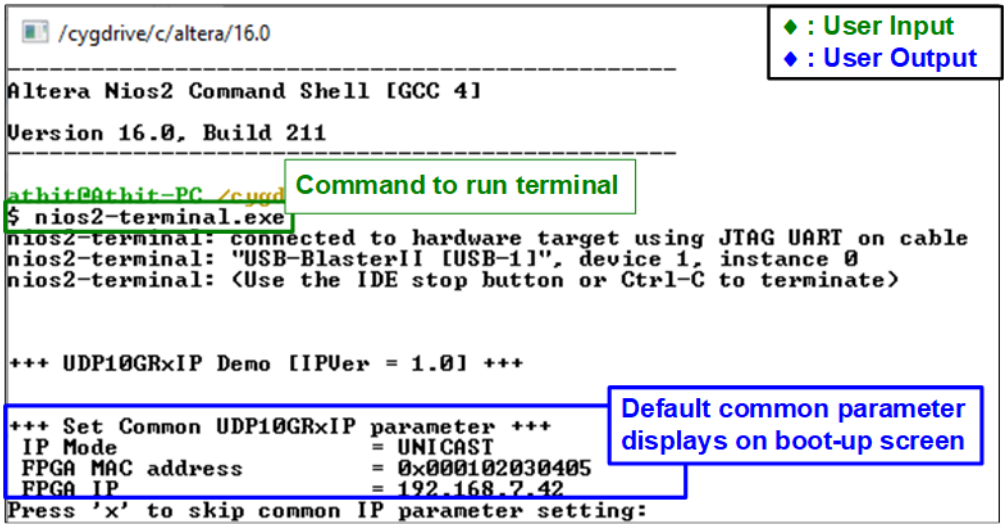

Figure 2-2 Display default common parameter

7) If user enters 'x' for all inputs, the IP will run initialization process by using default parameters. The default mode is Unicast that enables one session, session#0, as shown in Figure 2-3. To change some parameters, please see more details of Menu [1] "Set UDP10GRxIP parameter" in "dg_udp10giprx_instruction_en" document, available on our website. After finishing system initialization, main menu is displayed on NiosII command shell.

Note: Transfer performance in the demo depends on Test PC resource in Test platform.

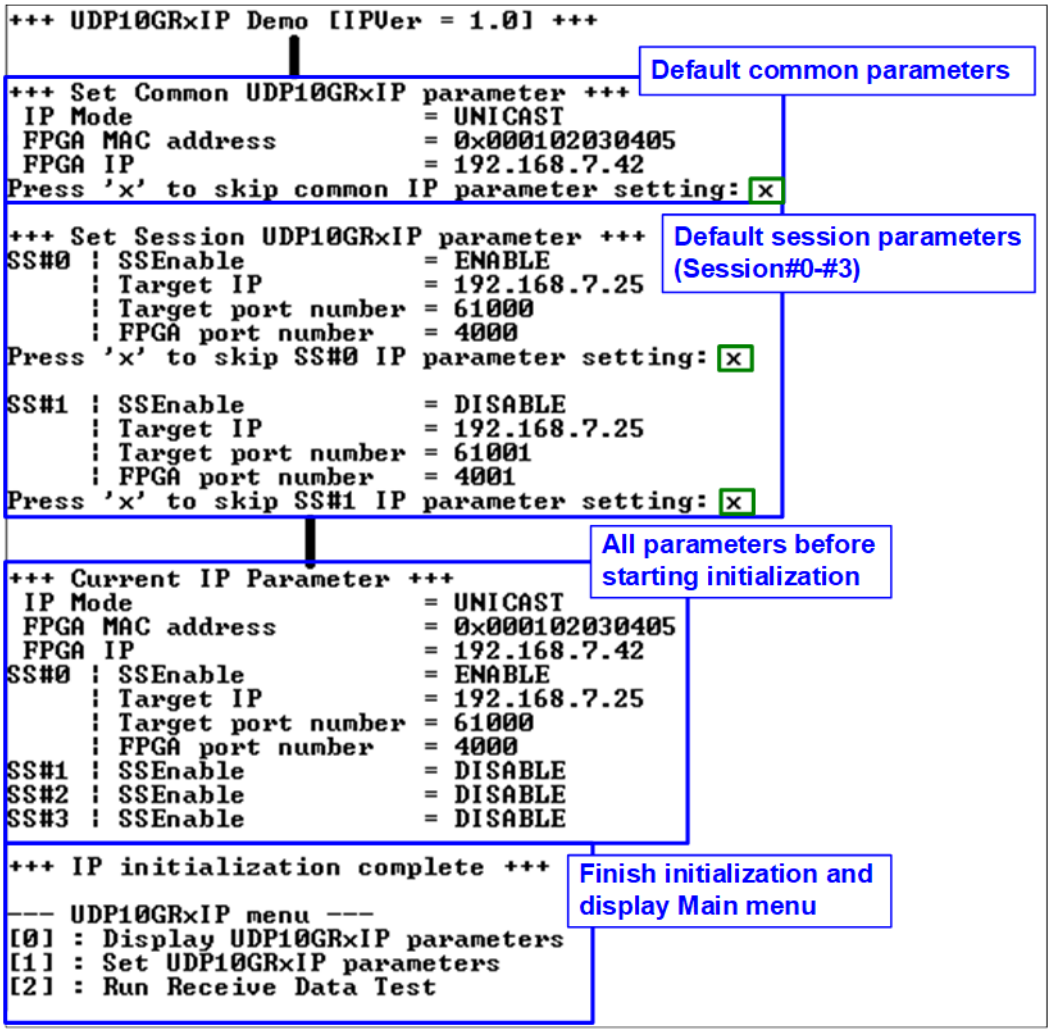

Figure 2-3 Input parameter setting and display main menu

3 Revision History

Revision	Date	Description
1.0	22-Apr-21	Initial version release