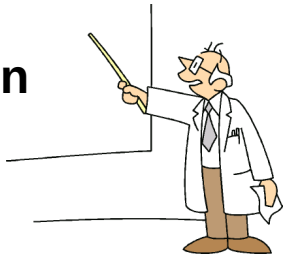
NVMe-IP Introduction for Xilinx

Ver1.6E

Optimal Solution for Recording Application!

Agenda

- NVMe SSD Overview
  - SSD Trends
  - Merit of NVMe SSD for embedded system
- NVMe-IP Introduction
  - Summary
  - Function
  - User Interface
  - Performance and Size
  - Development Environment/Reference Design
- Application



SSD Trends 1

- SATA interface is now performance bottle neck
  - SSD Read/Write speed is limited to 600MB/sec SATA bandwidth
- Move to PCI Express for faster speed
  - PCIe GEN3 x4lane can provide 4GB/sec transfer speed
- M.2 and BGA package suitable for compact application
  - M.2: Wid=22mm, Len=20/42/80/120mm DIMM-like small outline
  - BGA: 20mm x 16mm x 1.5mm, 1gram package

Current 2.5" SATA SSD

Latest M.2 type PCIe SSD

BGA type SSD

SSD Trends 2

- Host Controller Standard moves from AHCI to NVMe
  - Latest standard to extract maximum performance of SSD
  - Extended Queue size, 65536 concurrent command process
  - Most OS provides NVMe driver

FMS2015 "Annual Update on Interfaces" presentation

Merit of NVMe SSD for Embedded System 1

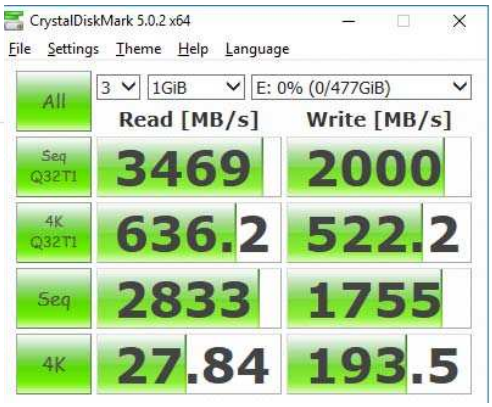
- **High Bandwidth: 3.2GB/s for Read, 2.1GB/s for Write**
- **Cost effective: Cost difference from SATA SSD is small**

$299.99 for 512GB

Samsung
Samsung 960 PRO Series - 512GB PCIe NVMe - M.2 Internal SSD (MZ-V6P512BW)
138 customer reviews | 119 answered questions
Was: $324.00
Price: $299.99 & FREE Shipping. Details
You Save: $24.01 (7%)
In Stock.
Want it Wednesday, May 24? Order within 11 hrs 26 mins and choose One-Day Shipping at checkout. Details
Ships from and sold by Amazon.com. Gift-wrap available.
Capacity: 512 GB

1TB	2TB	512 GB
$579.99	$1,191.38	$299.99

(Amazon.com 23-May-2017)



http://benchmarkreviews.com/41954/samsung-960-pro-nvme-ssd-review/6/

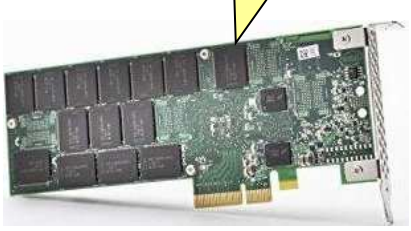
Cost and Performance of M.2 NVMe SSD (Samsung 960 PRO 512GB)

Merit of PCIe SSD for Embedded System 2

- **Various form factor**
  - **HHHL(Half-Height,Half-Length) general PCIe board**
  - **M.2 cost saving module**
  - **SFF-8639 of 2.5” drive compatible size**
  - **BGA package for direct mount on PCB**

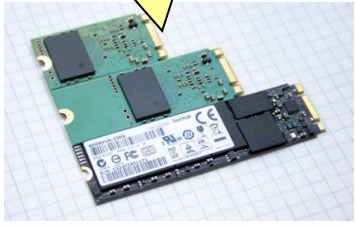
Merit

Big Capacity



HHHL PCIe board

Small, Extractable

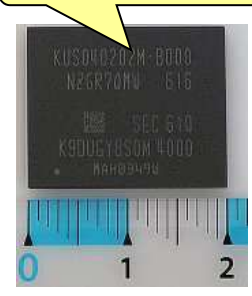


M.2 module (length=42/60/80mm)

Hot Swap

SFF-8639 package

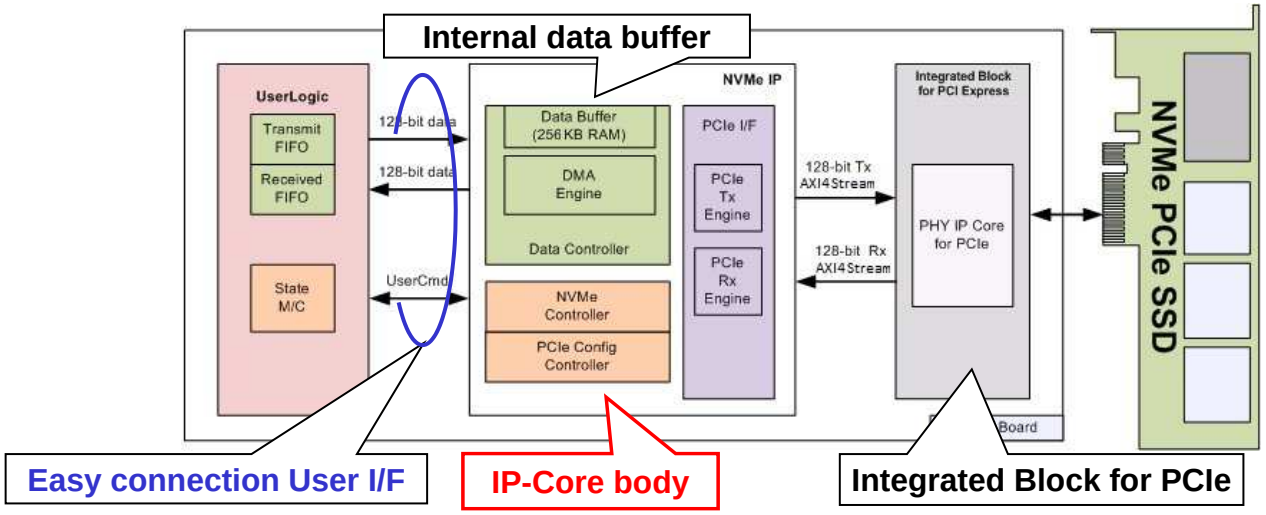
Mount on PCB



BGA pacakge

What's NVMe-IP

- What's NVMe-IP? -> Directly connect NVMe SSD with FPGA
- How to use? -> Just connect with user logic, no need CPU, its F/W, and External DDR Memory
- Application -> Best for ultra high speed data recording system
- User Merit? -> Can develop Storage Application in short period

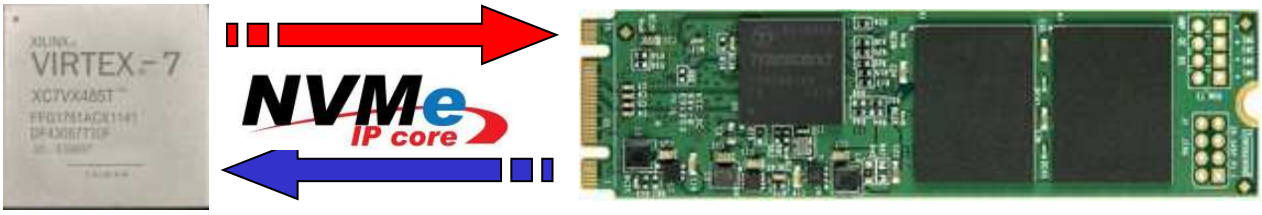


NVMe-IP Merit

1. **Function: Full automatic access to PCIe SSD**
   - No CPU and firmware necessary, just wired logic is enough
2. **Interface: Simple and easy connection**
   - Direct connection to Xilinx Integrated Block for PCIe
   - User I/F control is parameter with pulse, data is simple FIFO
   - Use BRAM for data buffer (external DDR memory not required)
3. **High Performance and Compact size**
   - Write=2148MB/s, Read=3252MB/s (measured by KCU105)
   - Support PCIe GEN3 (Operation confirmed on Kintex-Ultrascale)
   - IP-Core Size=2768SliceRegs, Memory=59BRAMTile
4. **Environment: Full reference design project**
   - Full Vivado project with real board operation in the package

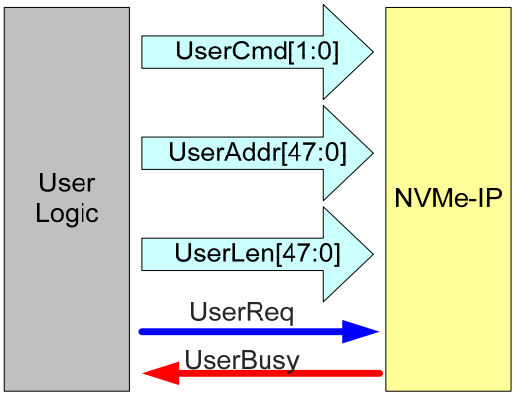
NVMe-IP Merit 1: Function

- **Special PCIe Root port for NVMe SSD control**
  - PCIe Initialization (Integrated Block for PCIe and NVMe register)
  - PCIe and SSD Status Monitor and error detection
- **NVMe Control function**
  - Control NVMe register by user R/W request
  - Process command sequence in NVMe standard
  - Data transfer and flow control between SSD, BRAM, and User FIFO

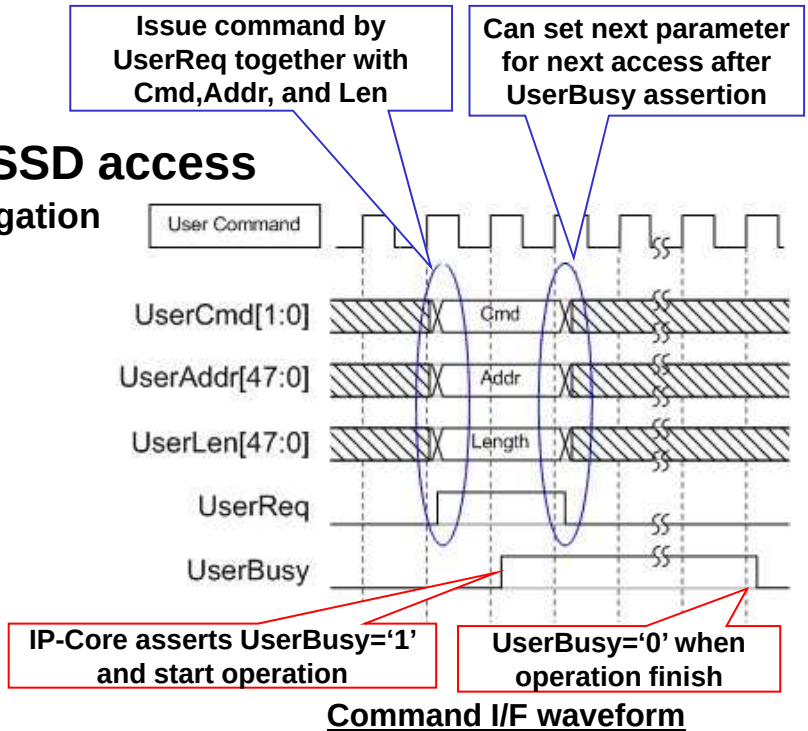


NVMe-IP Merit2: Command I/F

- **Easy Connection User I/F**
  - Set Command/Address/Length
  - Issue UserReq pulse
- **Full Automatic control for SSD access**
  - User only can wait UserBusy negation



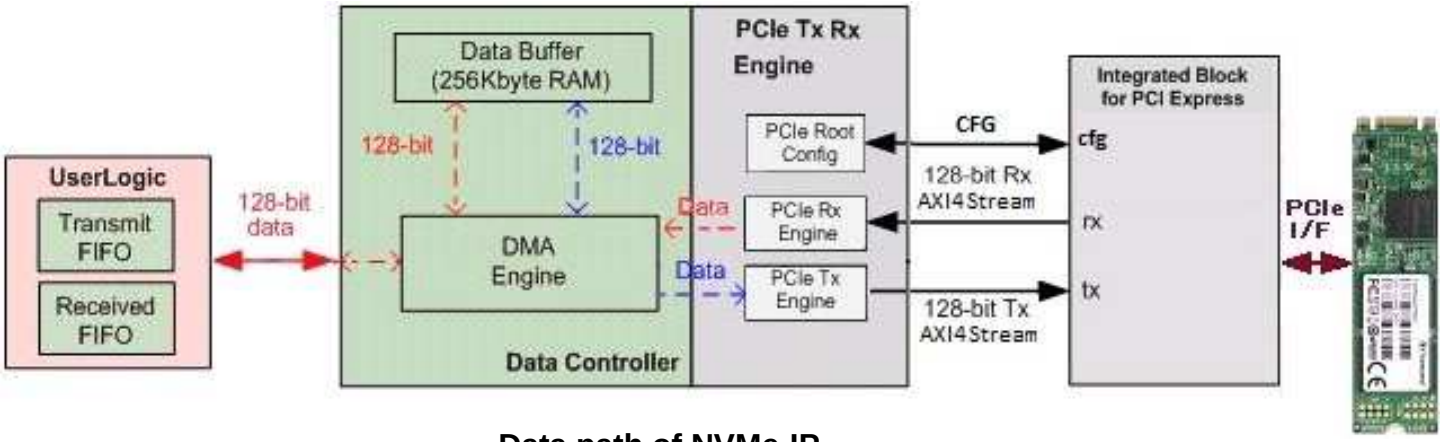
Command I/F Signals



Command I/F waveform

NVMe-IP Merit2: Data I/F

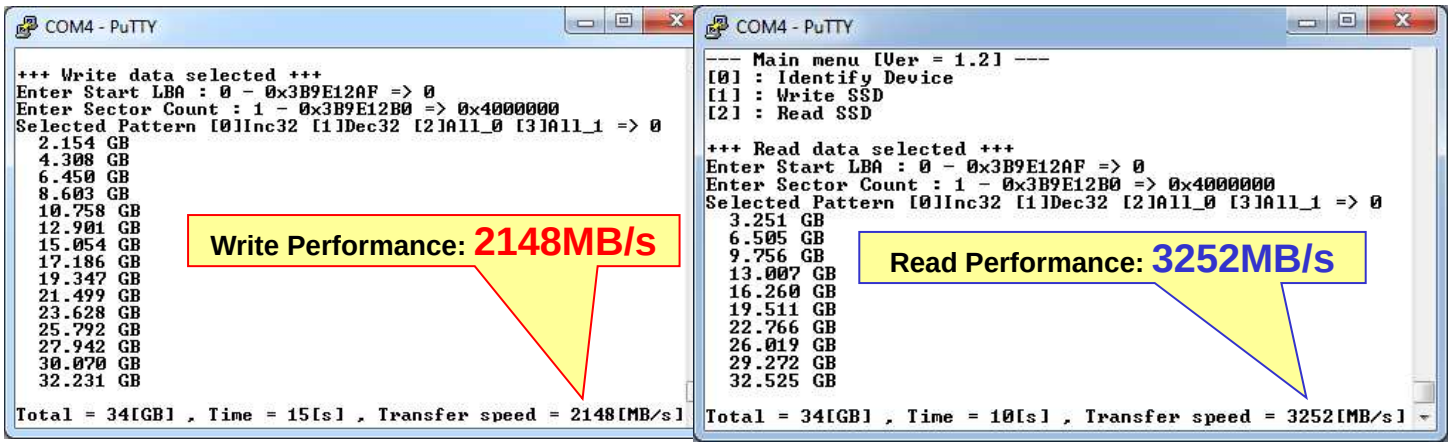
- **Simple 128bit FIFO for each of read and write**
  - **General FIFO of standard Xilinx LogiCORE library**
  - **Data buffer using 256KByte BRAM in NVMe-IP**



Data path of NVMe-IP

NVMe-IP Merit3: Performance

- **Automatic PCIe SSD access by pure hard-wired logic**
  - **Intelligent state machine for complete read/write command execution**
  - **Minimum over head and best performance by synchronized circuit**



Performance Evaluation Result (KCU105) **(SSD: Samsung MZ-V6P512BW)**

NVMe-IP Merit3: Compact Size

- **Optimized size with minimum resource consumption**
  - **Implements dedicated and optimized logic for NVMe SSD control**
- **Block RAM for data buffer**
  - **Internal block memory can minimize access overhead**

Example Implementation Statistics for 7-Series device (PCIe Gen2/Gen3)

Family	Example Device	Fmax (MHz)	Slice Regs	Slice LUTs	Slices	BRAMTile[1]	Design Tools
Virtex-7	XC7VX690TFFG1761-2	300	2768	2438	1146	59	Vivado2015.4
Virtex-7	XC7VX485TFFG1761-2	300	2861	2590	1117	59	Vivado2015.4
Zynq-7000	XC7Z045FFG900-2	300	2861	2589	1125	59	Vivado2015.4
Kintex-7	XC7K325TFFG900-2	300	2861	2593	1170	59	Vivado2015.4

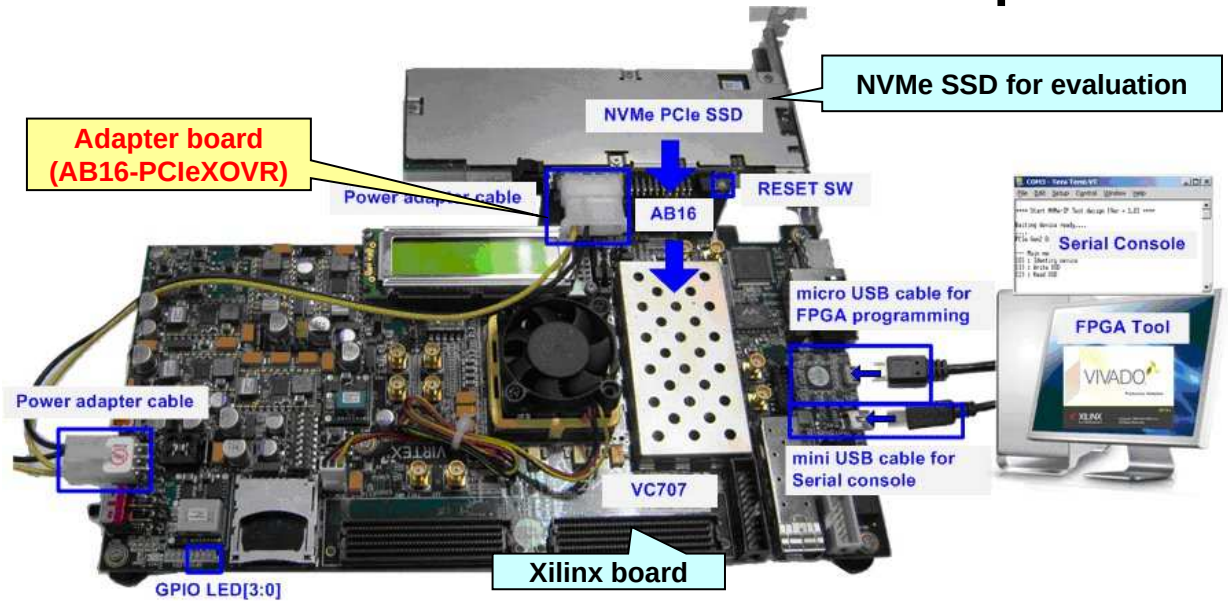
Example Implementation Statistics for Ultrascale device (PCIe Gen3)

Family	Example Device	Fmax (MHz)	CLB Regs	CLB LUTs	CLB	BRAMTile[1]	Design Tools
Kintex-Ultrascale	XCKU040FFVA1156-2E	344	2768	2448	699	59	Vivado2015.4

NVMe-IP Core standalone resource usage

NVMe-IP Merit4: Environment

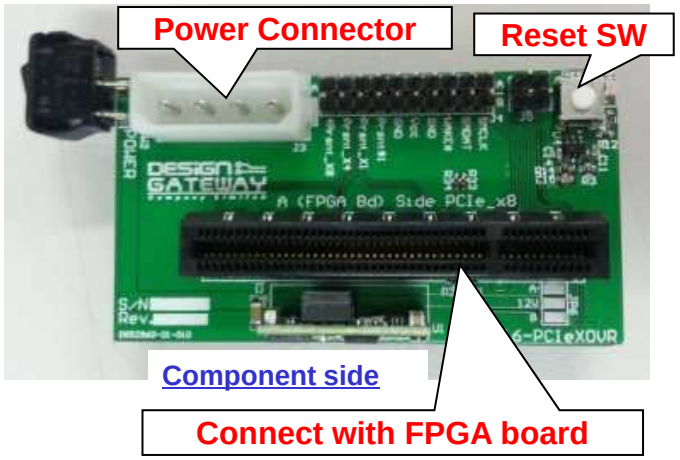
- **Real operation check with Xilinx evaluation board**
- **Free bit-file for evaluation before IP-core purchase**

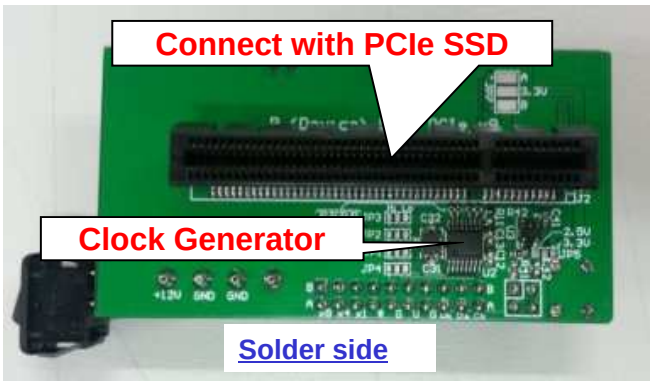


NVMe-IP evaluation environment

NVMe-IP Merit4: Development Tool

- Adapter board for FPGA board evaluation
  (Part#: AB16-PCIeXOVR)
- Connect FPGA board to PCIe socket on component side
- Connect PCIe SSD to PCIe socket on solder side
- SSD R/W access via adapter board from NVMe-IP in FPGA





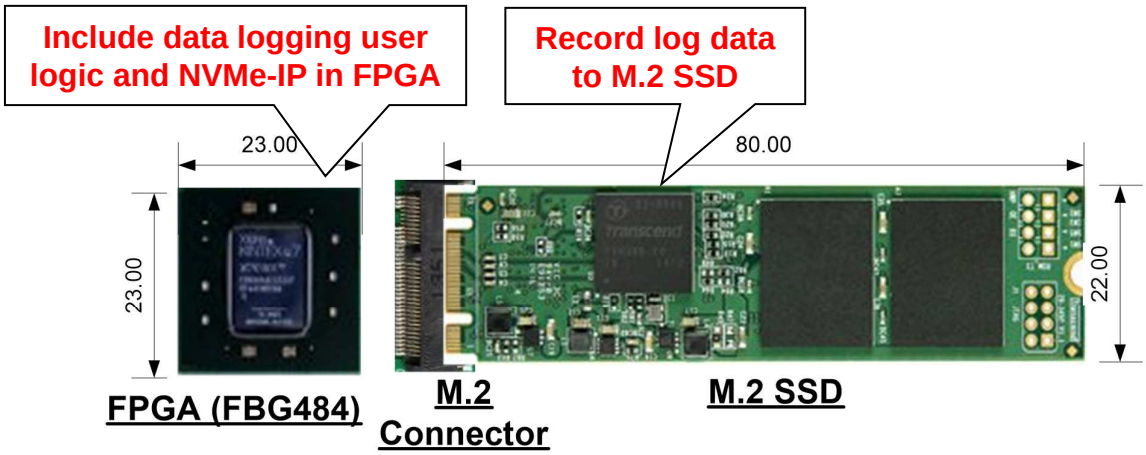
NVMe-IP Merit4: Reference Design

- Vivado project is attached with NVMe-IP deliverables
- Full source code (VHDL) except IP core
- Can save user system development duration
  - Confirm real board operation by original reference design.
  - Then modify a little to approach final user product.
  - Check real operation in each modification step.

Short-term development is possible without big turn back

NVMe-IP Application Example

- **Space-Saving FPGA data logging system**
  - **Latest FPGA+M.2 SSD**



System area image by FBG484 FPGA and M.2 SSD (unit: mm)

For more detail

- **Detailed technical information available on the web site.**
  - http://www.dgway.com/NVMe-IP_X_E.html
- **Contact**
  - **Design Gateway Co,. Ltd.**
  - **sales@design-gateway.com**
  - **FAX: +66-2-261-2290**

Revision History

Rev.	Date	Description
1.0E	10-Jun-16	English Version first release
1.1E	21-Jun-16	Support Kintex-Ultrascale
1.2E	25-Aug-16	Modify page17 because only one x16 DDR4 device can keep NVMe SSD performance
1.3E	12-Sep-16	Support Zynq-7000 and Kintex-7
1.4E	8-Nov-16	Support PCIe GEN3 on Virtex-7
1.5E	21-Dec-16	NVMe-IP core improvement by removing external DDR chip for data buffer
1.6E	6-Jun-17	Performance improved by internal PCIe bridge in NVMe-IP core