SATA3 RAID Demo on StratixV GX Dev Board Instruction

Rev1.0 04-Oct-13

This document describes the instruction to run 4-ch RAID0 of SATA3-IP demo on StratixV GX Development board.

1 Environment Setup

To run RAID demo, HSMCRAID board, provided by Design Gateway, is required to connect StratixV GX Development board with 4 SATA-III HDD/SSD, as shown in Figure 1-1.

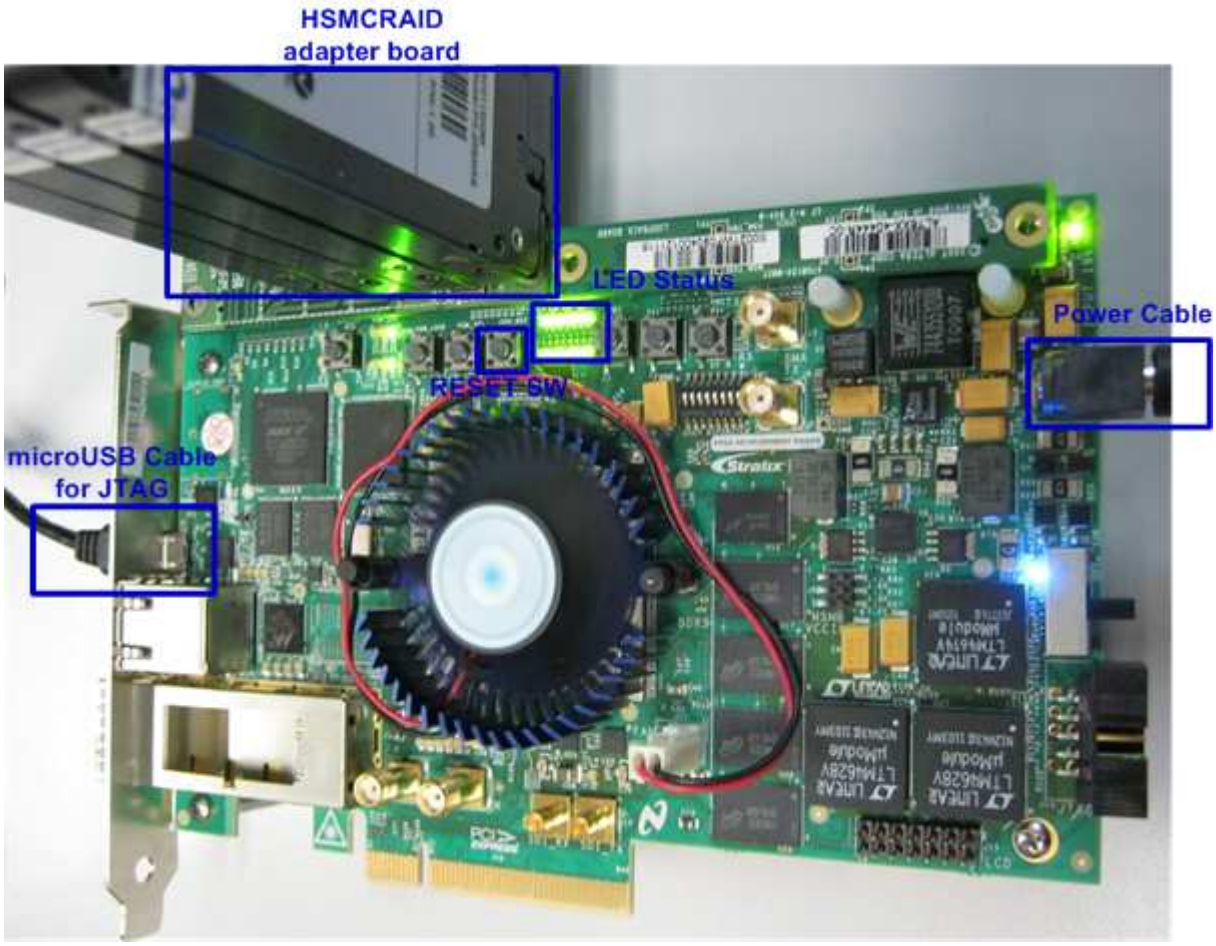

Figure 1-1 RAID Demo Environment Setup

Following step is setup procedure for running demo.

- Connect HSMCRAID board to HSMC#A connector on StratixV GX Development board

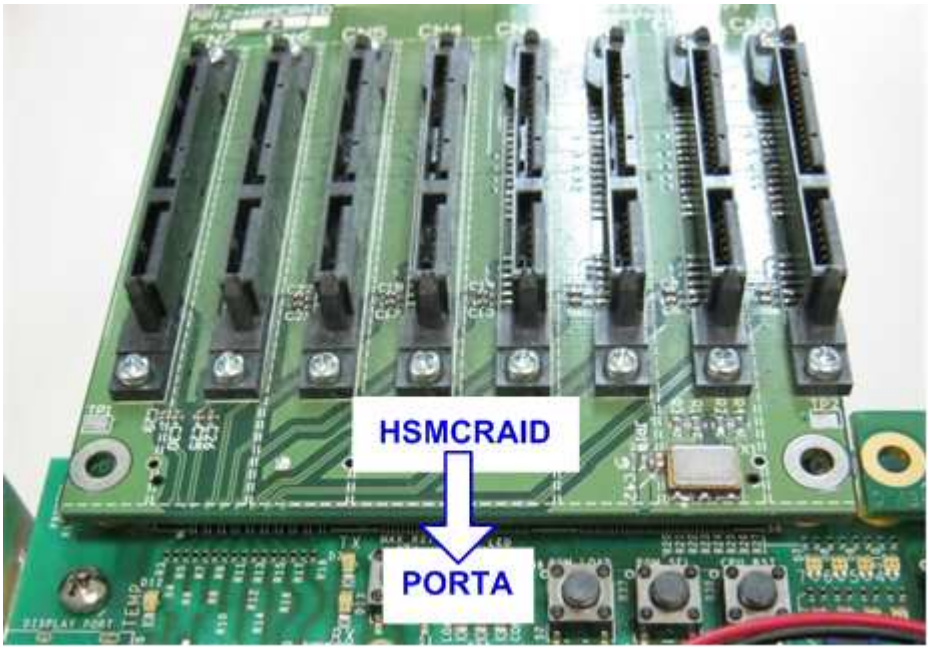

Figure 1-2 HSMCRAID Connection

- Connect 4x2.5” SATA-III HDD/SSD to CN0 – CN3 on HSMCRAID board, as shown in Figure 1-3.
- Connect ATX power cable to HSMCRAID board.

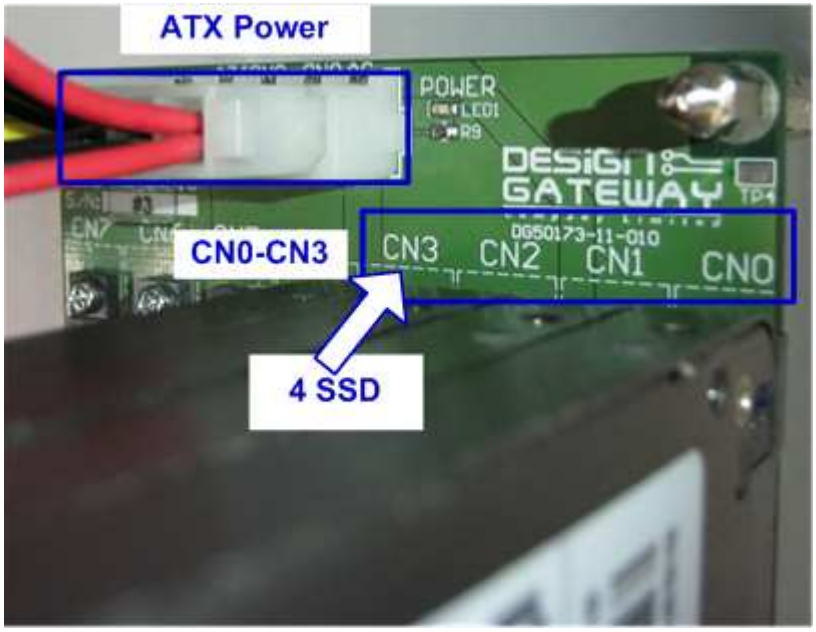

Figure 1-3 SSD and ATX Power Connection

- Connect Power adapter cable to StratixV GX Development board
- Connect microUSB cable from StratixV GX board to PC.
- Power on StratixV GX board and ATX power for SATA-III HDD/SSD

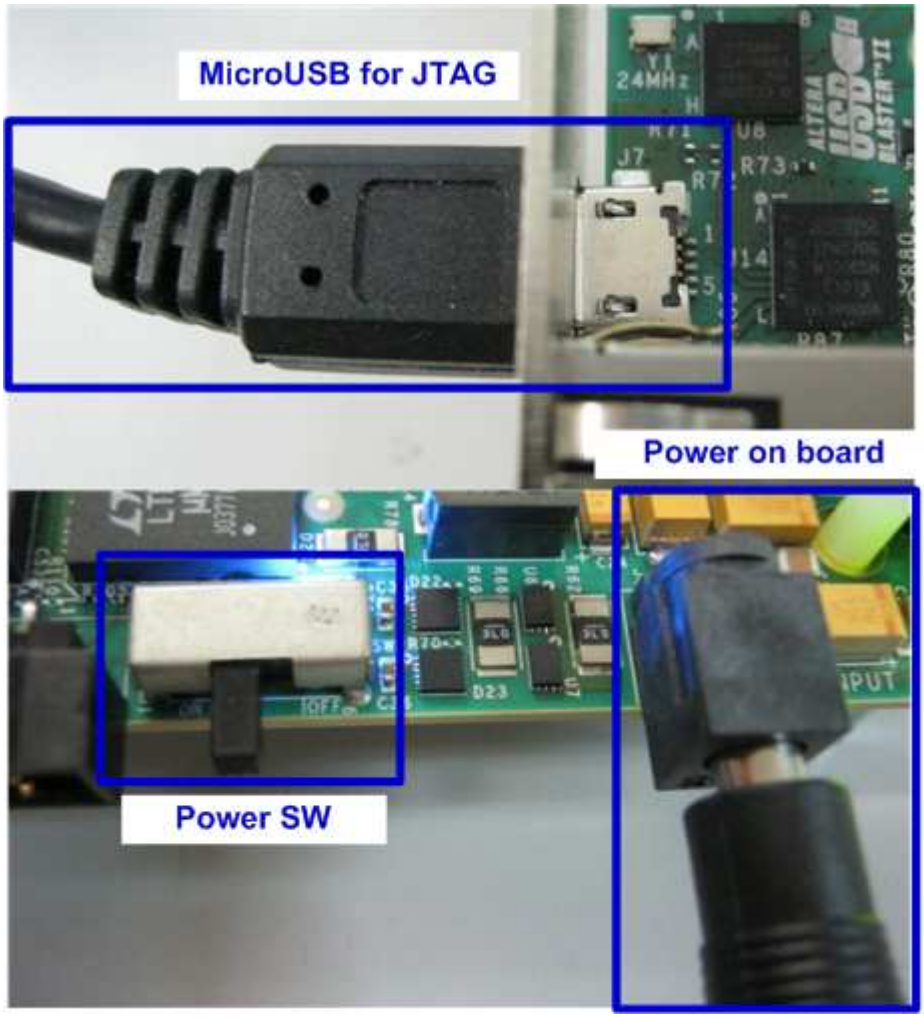

Figure 1-4 MicroUSB and Power Connection

- Open “Clock Control” application which is provided by Altera for StratixV GX Development board, change to U38 tab, change CLK0 value to be 150 MHz, and press “Set New Frequency” button. Then, wait until clock programmable complete. After this step, reference clock will be 150 MHz for SATA interface, as shown in Figure 1-5.

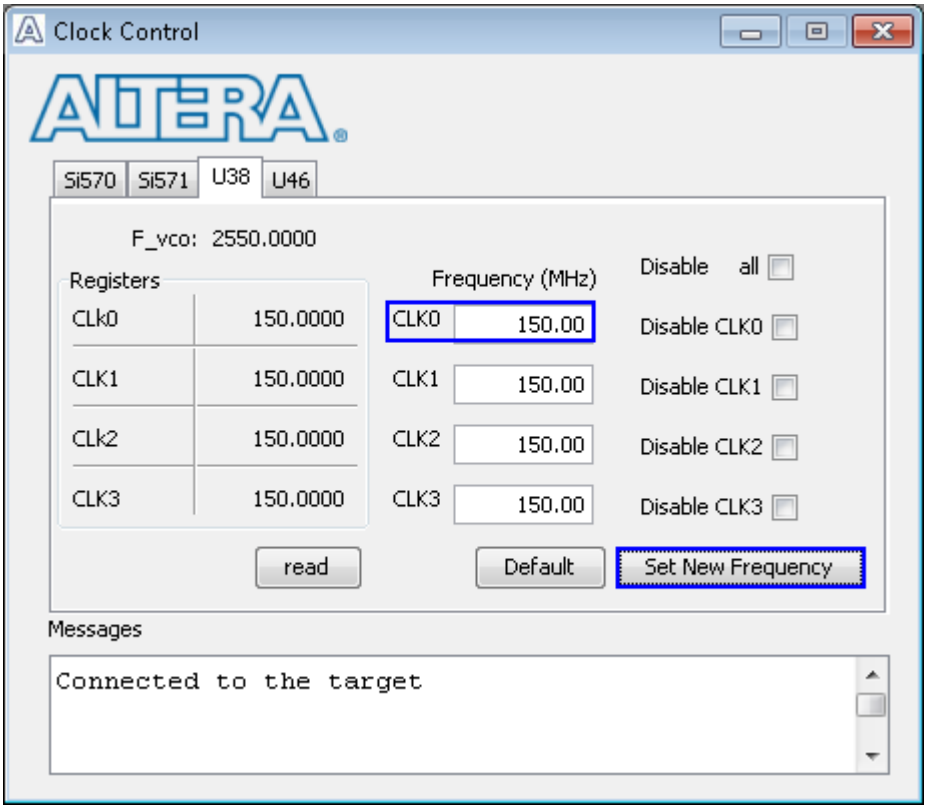

Figure 1-5 Set programmable clock = 150 MHz by Clock Control Application

- Open Quartus Programmer and download “nios_sata3.sof” to StratixV GX Development board, as shown in Figure 1-6.

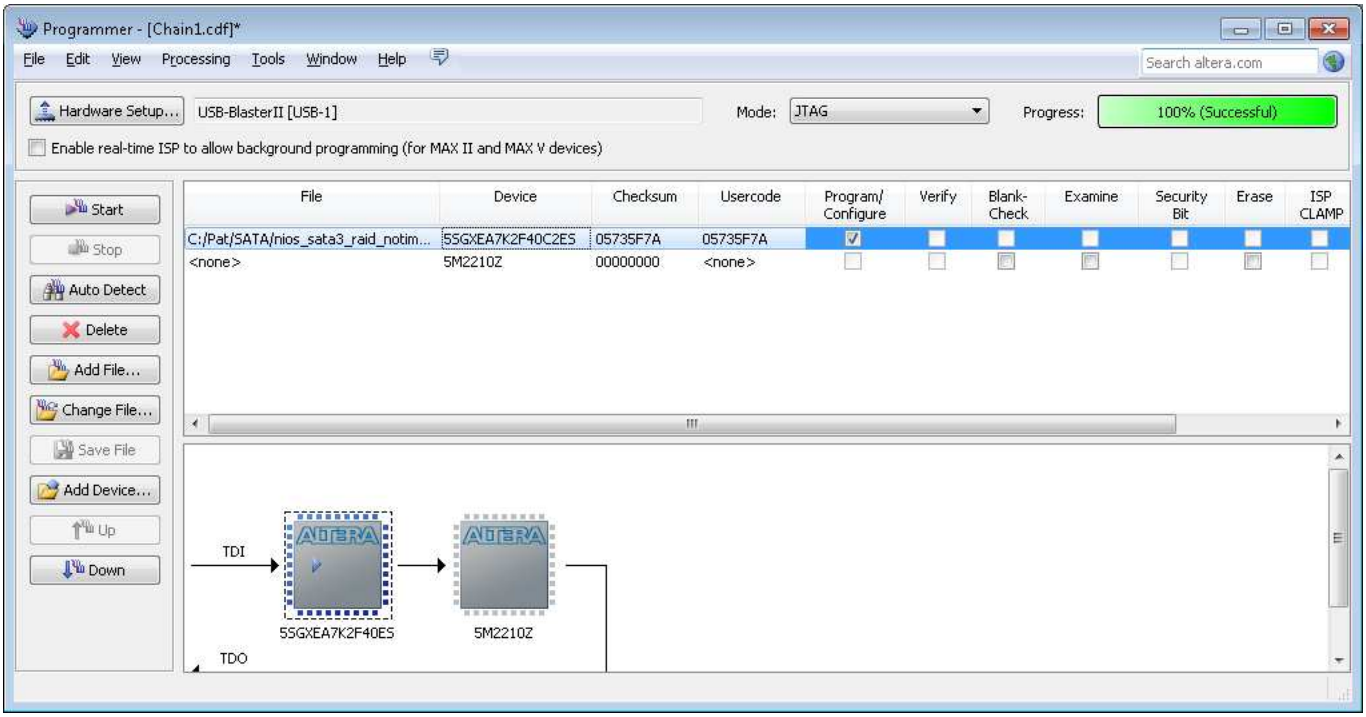

Figure 1-6 Programmer Environment

- Check LED status on StratixV GX board. LED0-7 should be turn-on, and TX and RX of HSMA LED should be OFF as shown in Figure 1-7. The description of each LED is shown in Table 1-1.

Figure 1-7 Normal operation LED Status

LED	SATA	ON	OFF	BLINK
LED0	CN0	OK	SATA-IP cannot detect SATA device. Please check SATA@CN0 connection and confirm that programmable clock is set to 150 MHz.	Transfer error, or 1-hour timeout for evaluation configure file
LED1	CN0	OK	Internal PLL is not LOCK Please confirm that programmable clock is set to 150 MHz.	
LED2	CN1	Same description with LED0, but used for SATA@CN1 status.		
LED3	CN1	Same description with LED1, but used for SATA@CN1 status.		
LED4	CN2	Same description with LED0, but used for SATA@CN2 status.		
LED5	CN2	Same description with LED1, but used for SATA@CN2 status.		
LED6	CN3	Same description with LED0, but used for SATA@CN3 status.		
LED7	CN3	Same description with LED1, but used for SATA@CN3 status.		
D3 (TX)	All	Write SSD in process	Idle Status	-
D13 (RX)	All	Read SSD in process	Idle Status	-

Table 1-1 LED Status of RAID reference design on StratixV GX board

- Open NiosII Command Shell.
- Type “nios2-terminal” and then boot-up screen with Main menu for running SATA RAID demo is displayed, as shown in Figure 1-8. More details about each Menu are described in next topic.

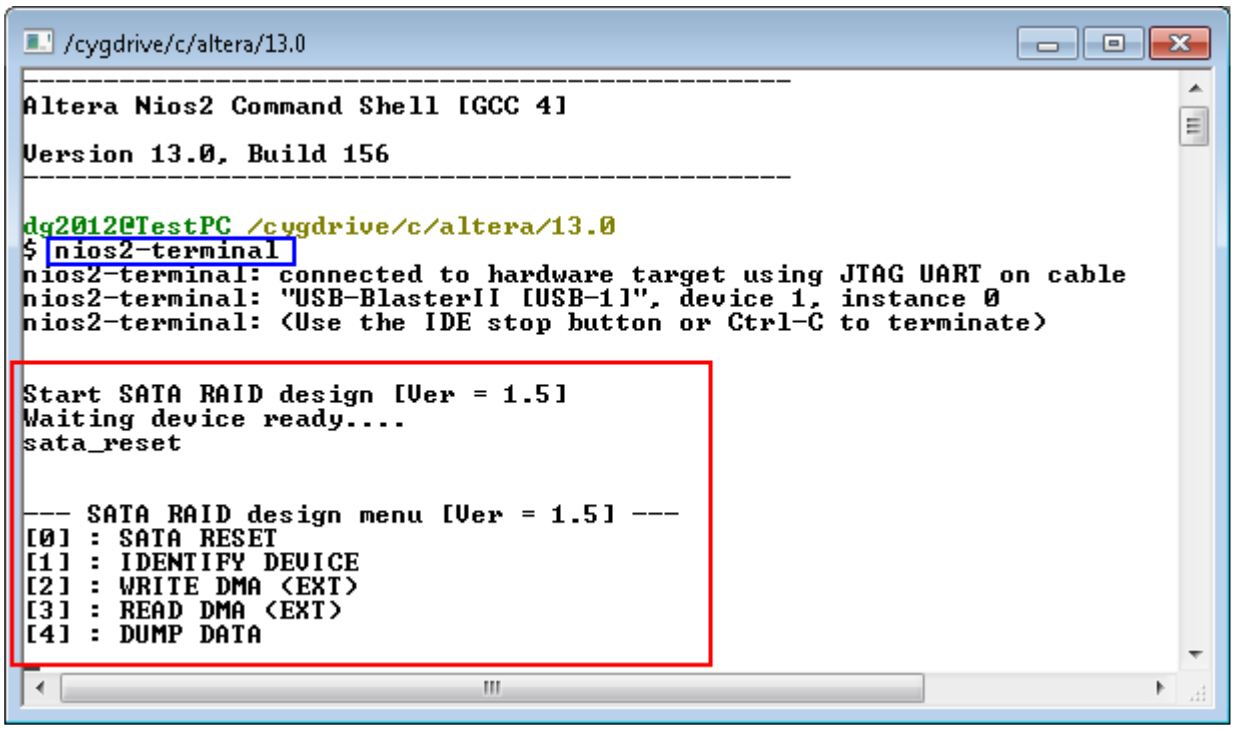

Figure 1-8 Run NIOSII Terminal and boot-up screen

2 Main Menu

2.1 SATA RESET

Select '0' for sending hardware reset signal to SATA-IP. Hardware reset is designed to reset all 4 SATA-IP and SATA-PHY modules. So, SATA initialize process will be restart again and display "SATA RESET selected", as shown in Figure 2-1.

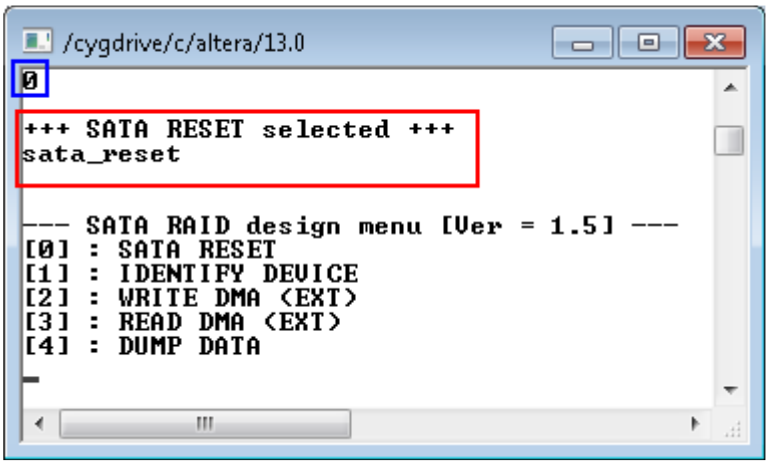

Figure 2-1 SATA RESET Menu

2.2 IDENTIFY DEVICE

Select '1' for sending "IDENTIFY DEVICE" command to 4 HDD/SSD. Disk information (Model name, 48-bit LBA supported, disk capacity) of all four SATA devices will be displayed by using this menu, as shown in Figure 2-2. From this command, maximum LBA size will be calculated from disk which has minimum size x 4.

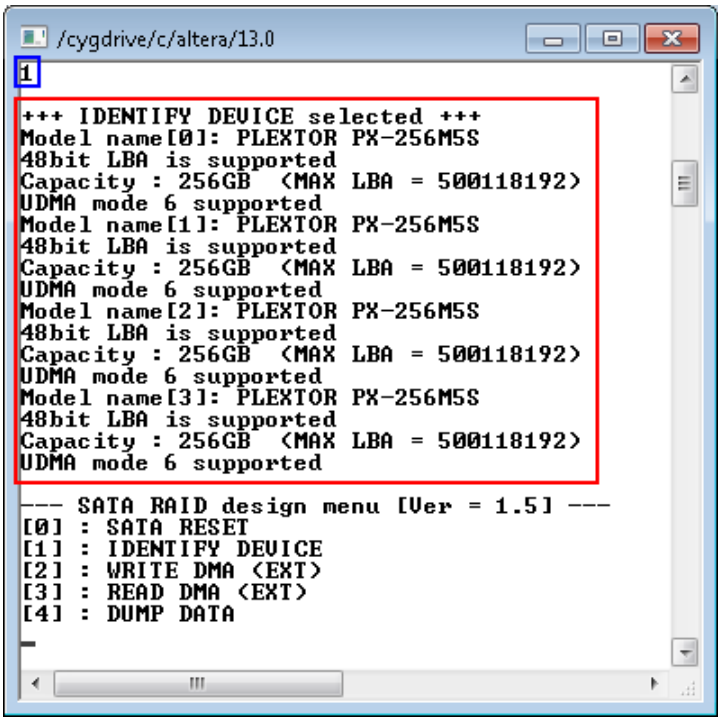

Figure 2-2 IDENTIFY DEVICE Menu

2.3 WRITE COMMAND

Select '2' for sending "WRITE DMA (EXT)" command to HDD/SSD. Input parameter is received as decimal unit by default. 0x is used to be prefix for input as heximal unit. Three inputs are required for this menu, i.e.

- Start LBA: this value, divided by 4, is the start sector number of each HDD/SSD to write data.
- Sector Count: this value, divided by 4, is the total transfer size in sector unit (512 byte) for writing each HDD/SSD. The data size which CPU filled to write buffer is equal to this input. If this value is more than 262144 (4 x maximum size of one SATA command), only 262144 sector data is filled and the later command will use same data area with the first command.
- Write Pattern: this value is used for selecting test pattern to write to buffer and then forward to HDD/SSD. There are 5 test patterns in this demo, i.e. 32-bit increment pattern[0], 32-bit decrement pattern[1], 00000000H[2], FFFFFFFFH[3], and 32-bit LFSR[4].

After Software receives all inputs correctly,
- "Prepare data" will be displayed during CPU writing test pattern data to write buffer.
- "Execute Write" will be displayed during CPU sending WRITE DMA (EXT) command and transferring data from write buffer to HDD/SSD.
- Transfer speed will be displayed after write operation complete.

Figure 2-3 shows two examples of write command with different transfer size. Bigger transfer size can show higher performance speed.

Write operation is cancelled by two cases, i.e. receiving error input or receiving input from keyboard during CPU processing, as shown in Figure 2-4 and Figure 2-5 sequentially.

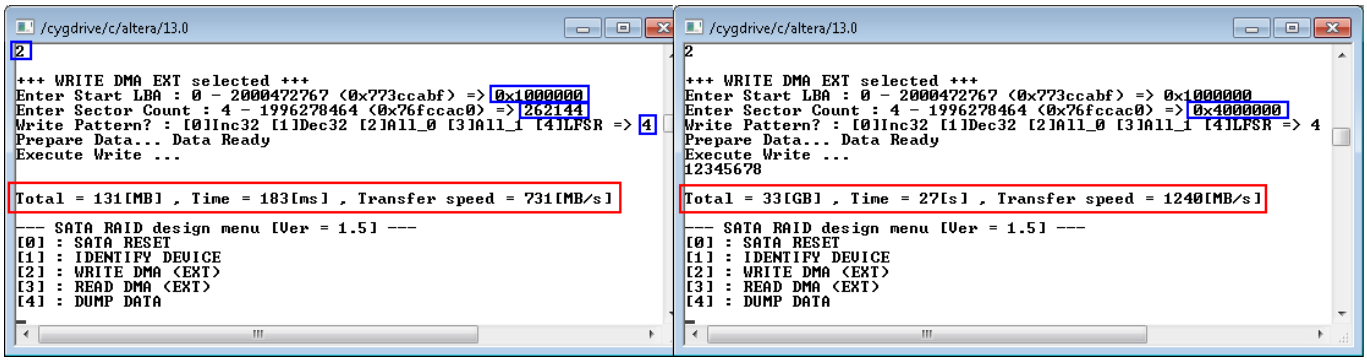

Figure 2-3 WRITE DMA (EXT) command input and output

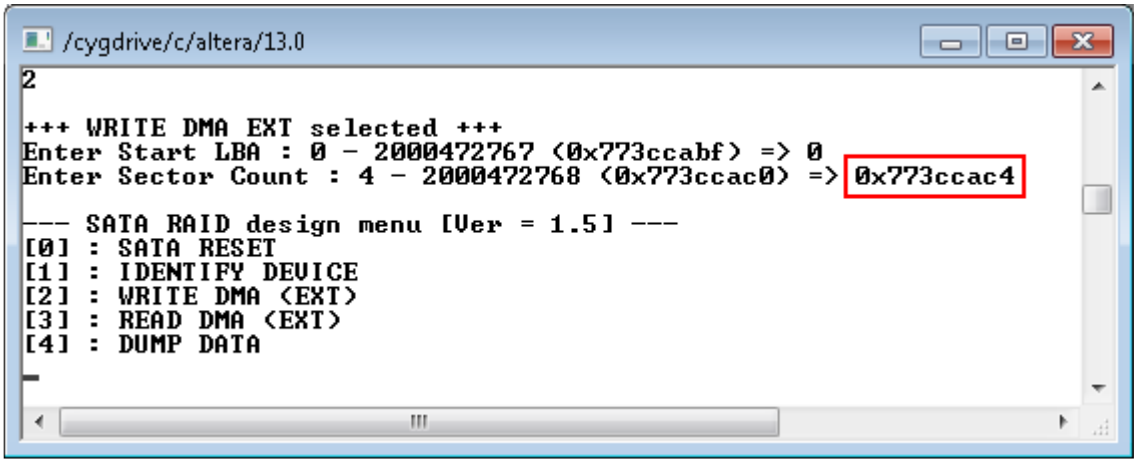

Figure 2-4 Write operation cancelled from error input

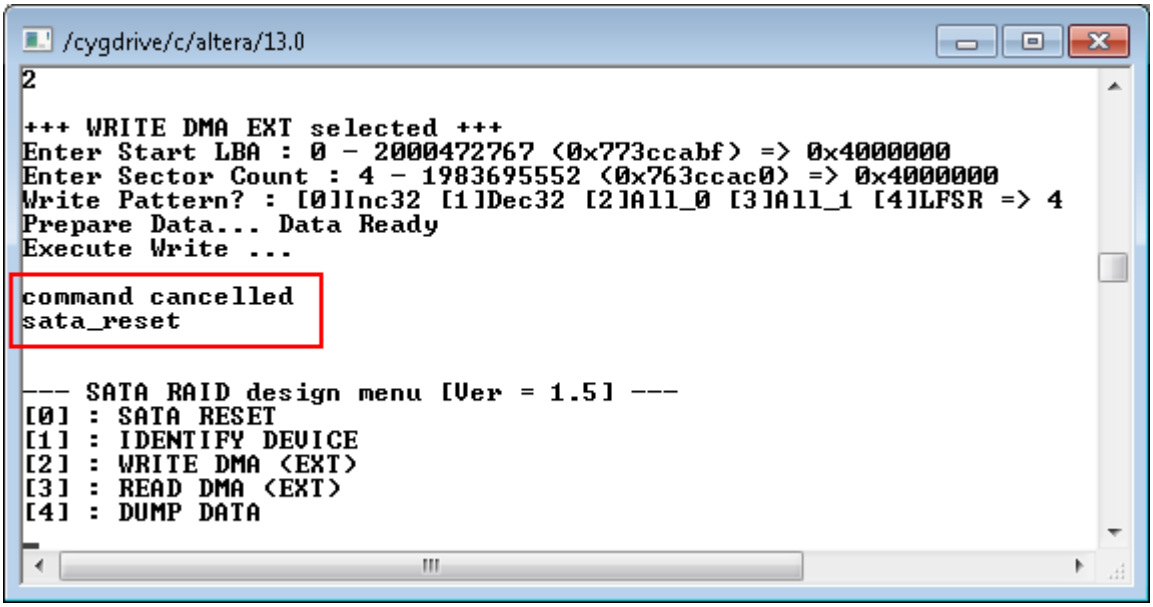

Figure 2-5 Write Operation cancelled from receiving input during operation

2.4 READ COMMAND

Select '3' for sending "READ DMA (EXT)" command to HDD/SSD. Input parameter is received as decimal unit by default. 0x is used to be prefix for input as heximal unit. Two or three inputs are required for this menu, i.e.

- Start LBA: same description with Start LBA in WRITE DMA (EXT) menu, but this is for read operation.
- Sector Count: same description with Sector Count in WRITE DMA (EXT) menu. If this input is not more than 262144, the third input will be displayed for selecting verification pattern. If input is more than 262144, the third input will not be displayed to skip data verification process for checking performance only, as shown in Figure 2-6.
- Verify Pattern: this value is used for selecting verification pattern. This input should be matched with the pattern in WRITE DMA (EXT) menu. Five verification patterns can be selected, similar to write pattern. "Verify Data … Success" is displayed for success case, and "Data Mismatch with failure value" is displayed for failure case, as shown in Figure 2-7

Similar to WRITE COMMAND menu, read operation will be cancelled if receiving error input value or receiving input from keyboard during CPU processing, as shown in Figure 2-8 and Figure 2-9 sequentially.

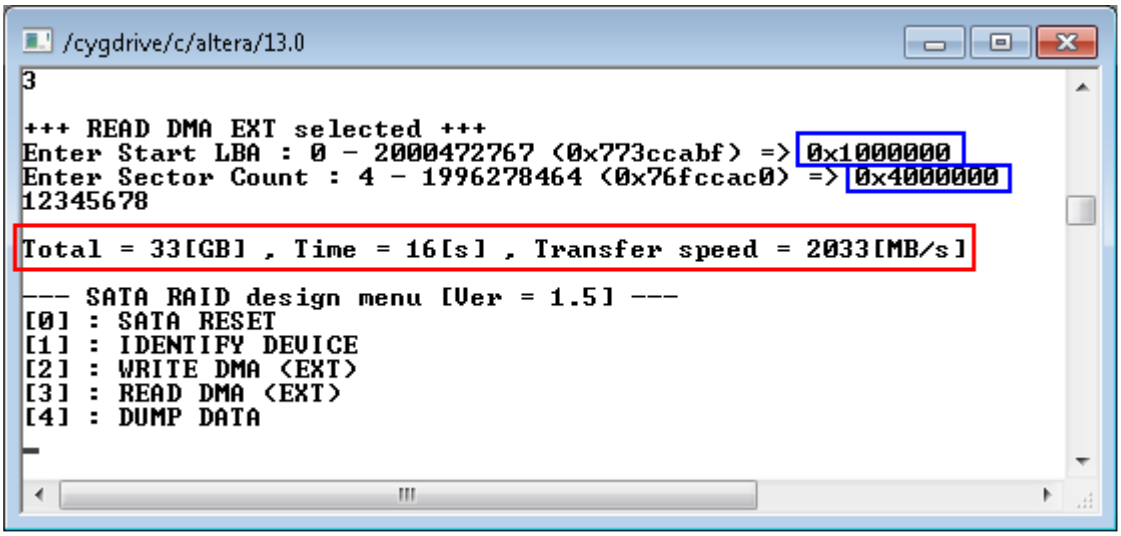

Figure 2-6 READ COMMAND without Verify

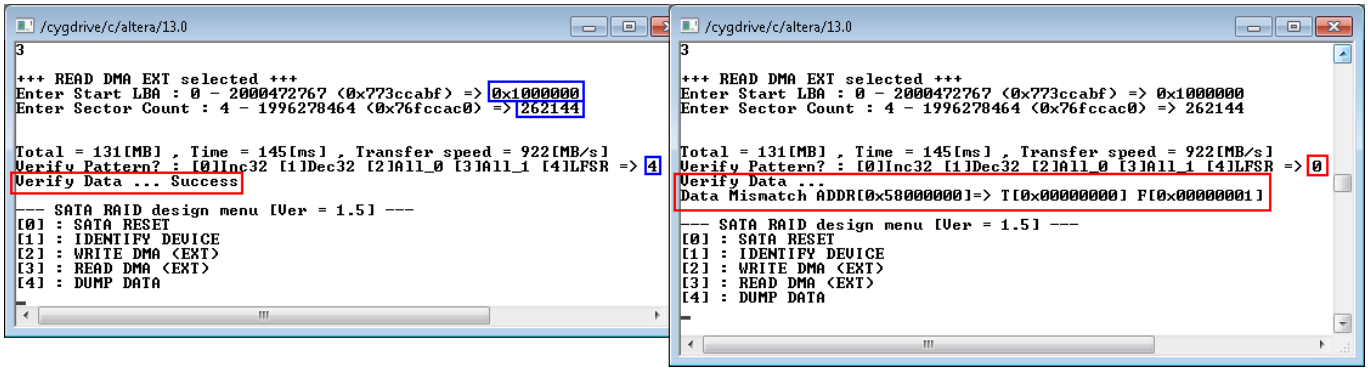

Figure 2-7 READ COMMAND with verify

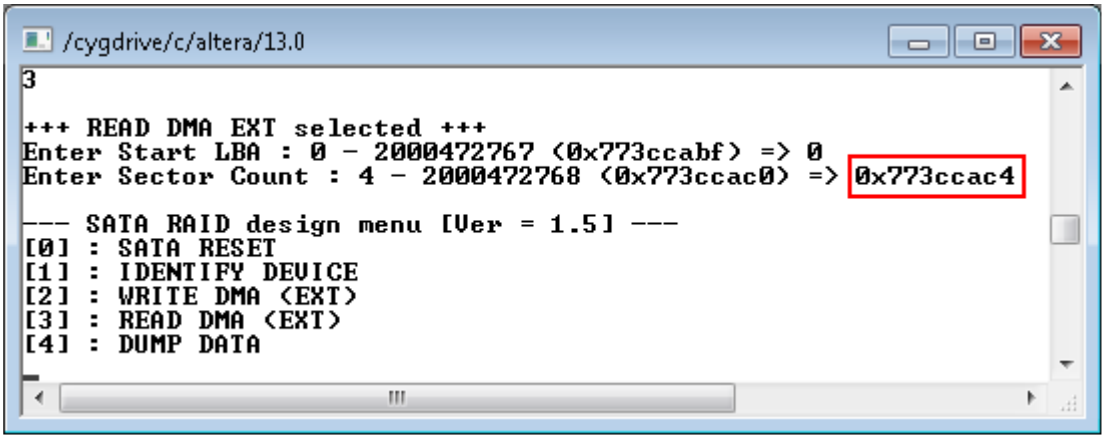

Figure 2-8 Read Operation cancelled from error input

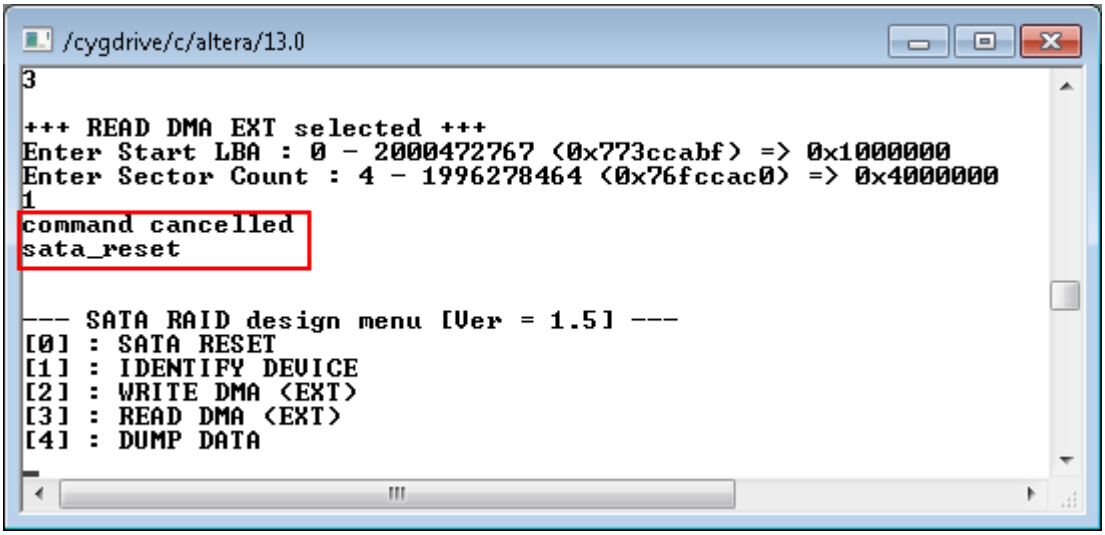

Figure 2-9 Read Operation cancelled from receiving input during operation

2.5 DUMP DATA

Select '4' to read data from DDR3 or read control register inside Avalon2SATA module for debugging. Two inputs are required for this menu, i.e.

- Start address: Heximal value can be input by adding prefix "0x". Memory map of this reference design is displayed in Table 2-1.
- Byte length: Input read length in byte unit.

After setting all inputs, all read values will be displayed on console, as shown in Figure 2-10.

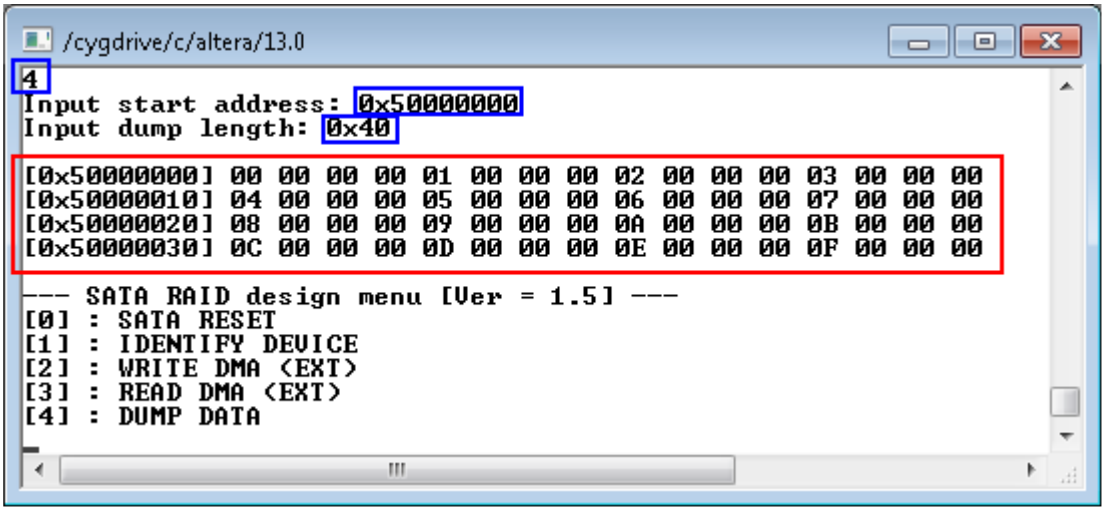

Figure 2-10 DUMP DATA Menu

Address	Memory map
0x01000000-0x0100001F	Avalon2SATA register area for SATA@CN0
0x01000100-0x0100011F	Avalon2SATA register area for SATA@CN1
0x01000200-0x0100021F	Avalon2SATA register area for SATA@CN2
0x01000300-0x0100031F	Avalon2SATA register area for SATA@CN3
0x40000000-0x4FFFFFFF	DDR3 memory area
- 0x40000000-0x40000FFF	TX FIS area
- 0x40001000-0x40001FFF	RX FIS area for SATA@CN0
- 0x40002000-0x40002FFF	RX FIS area for SATA@CN1
- 0x40003000-0x40003FFF	RX FIS area for SATA@CN2
- 0x40004000-0x40004FFF	RX FIS area for SATA@CN3
- 0x50000000-0x51FFFFFF	TX DATA FIS area for SATA@CN0
- 0x52000000-0x53FFFFFF	TX DATA FIS area for SATA@CN1
- 0x54000000-0x55FFFFFF	TX DATA FIS area for SATA@CN2
- 0x56000000-0x57FFFFFF	TX DATA FIS area for SATA@CN3
- 0x58000000-0x59FFFFFF	RX DATA FIS area for SATA@CN0
- 0x5A000000-0x5BFFFFFF	RX DATA FIS area for SATA@CN1
- 0x5C000000-0x5DFFFFFF	RX DATA FIS area for SATA@CN2
- 0x5E000000-0x5FFFFFFF	RX DATA FIS area for SATA@CN3

Table 2-1 Memory map in NIOSII system

3 Revision History

Revision	Date	Description
1.0	04-Sep-13	Initial Release