SATA3 Raid reference design on ArriaV GX manual

Rev1.1 4-Sep-13

1. Introduction

The detail for SATA host application is described in "dg_sata3_host_refdesign_ar5_en.pdf" which shows one channel operation, so user should read it firstly before continuing RAID design. In this document, it will describe only the additional part to modify the design from one channel to 4 channels operating RAID0 system.

2. Hardware description

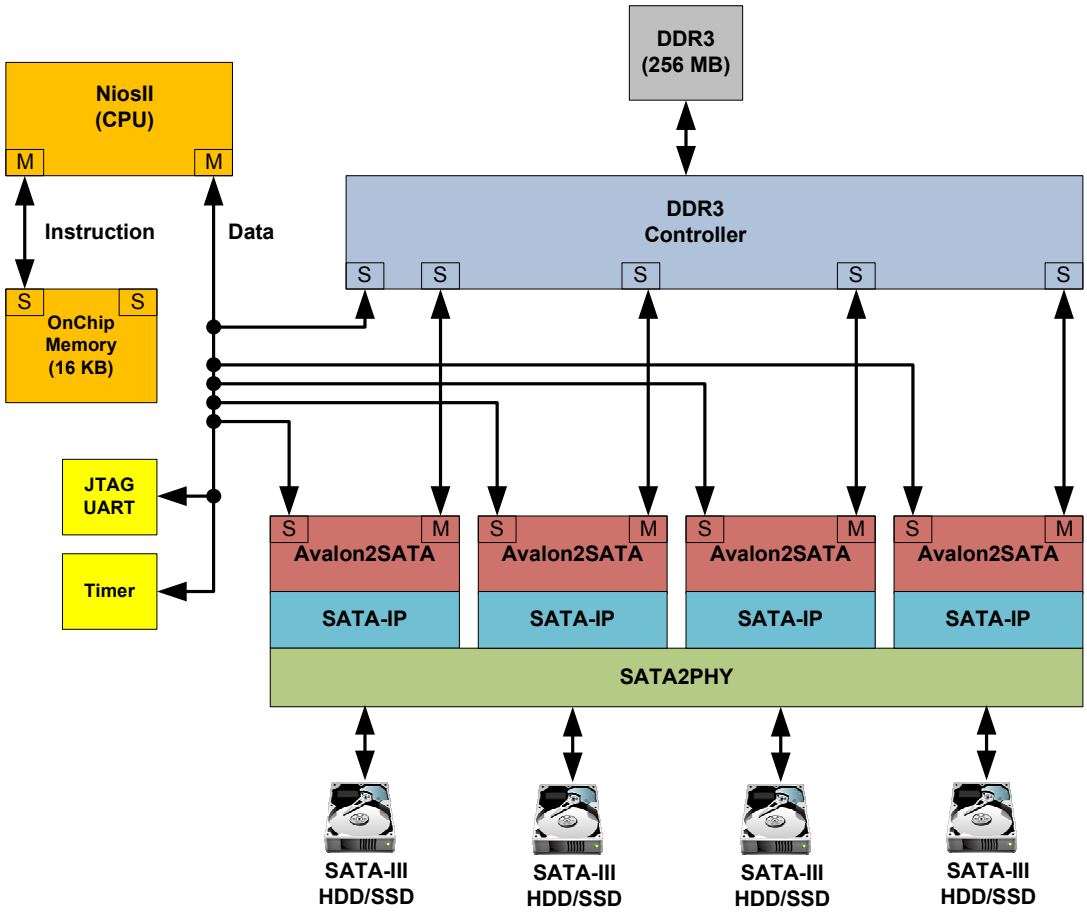

Figure 1 Block diagram of the reference design

- SATA IP RAID design implementation on ArriaV GX Starter board

To modify one host design to be 4 channels RAID0 design, three sets of Avalon2SATA and SATA-IP are required to connect three SATA devices into the system. Control ports are connected to NiosII while data ports are connected to DDR3 controller directly. So, DDR3 and CPU bandwidth will be shared among all four SATA channels.

For SATA physical layer on RAID design, PHY component and the reconfiguration module generated from Megawizard merge all four channels into one file. Since some reset are shared among SATA channels, only "PhyRstCtrl.vhd" is designed to control all channel operations and use four OOB controls to initialize independently, as shown in Figure 2.

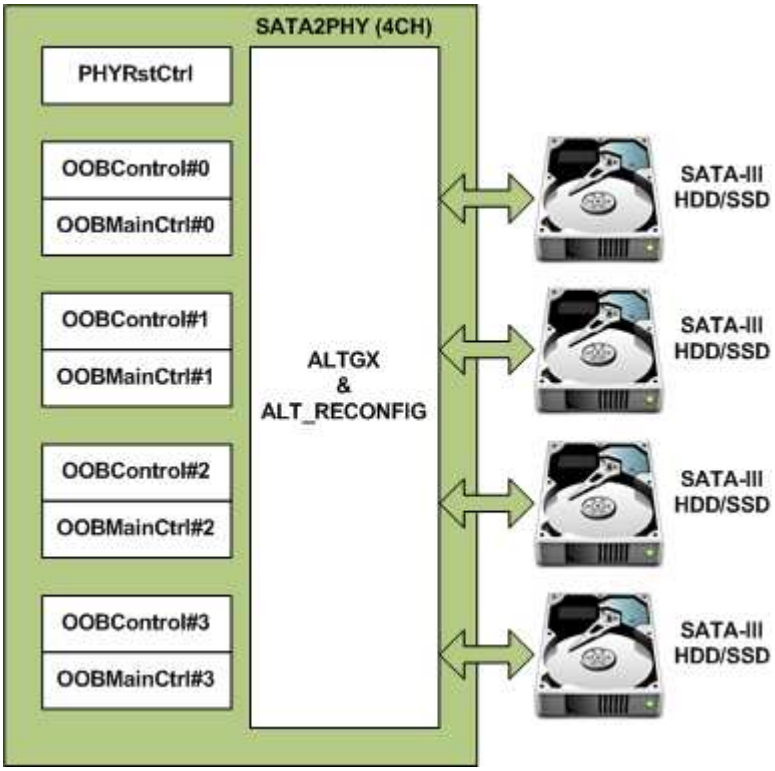

Figure 2 PHY RAID Block Diagram

To control each SATA channel independently, four register areas are defined for NiosII, i.e.

- BA : Base Address = 0x01000000 for SATA device#0
  = 0x01000100 for SATA device#1
  = 0x01000200 for SATA device#2
  = 0x01000300 for SATA device#3

As shown in Figure 3, DDR3 memory area in this demo is split into 4 areas, i.e.

- TX FIS for storing transmit non-DATA FIS from CPU to SATA device. All 4 SATA channels use the same transmit area to create same FIS to SATA device.
- RX FIS#0-3 for storing received non-DATA FIS from each SATA device to CPU, so four different areas are mapped in DDR3.
- TX DATA FIS#0-3 for storing transmit DATA FIS from CPU to SATA device. Data in each SATA device is different, so four areas are mapped.
- RX DATA FIS#0-3 for storing received DATA FIS from each SATA device to CPU, so four different areas are mapped in DDR3.

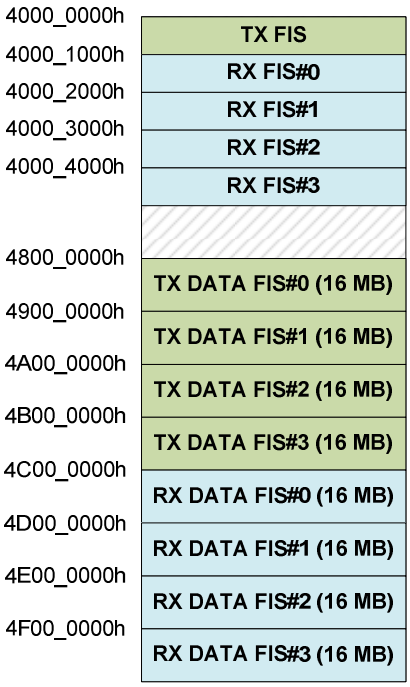

Figure 3 Memory map of Main Memory (DDR3)

- Necessary consideration

Host software source code of this design is stored in “software/Sata_host/Sata_host.c”. Note that this reference design does not include error check or recovery from illegal/unexpected behavior. So user needs to add such consideration that software should check status or error check when Register – Device to Host FIS is received from the Device.

Figure 4 shows reference design operation result on NiosII Terminal screen.

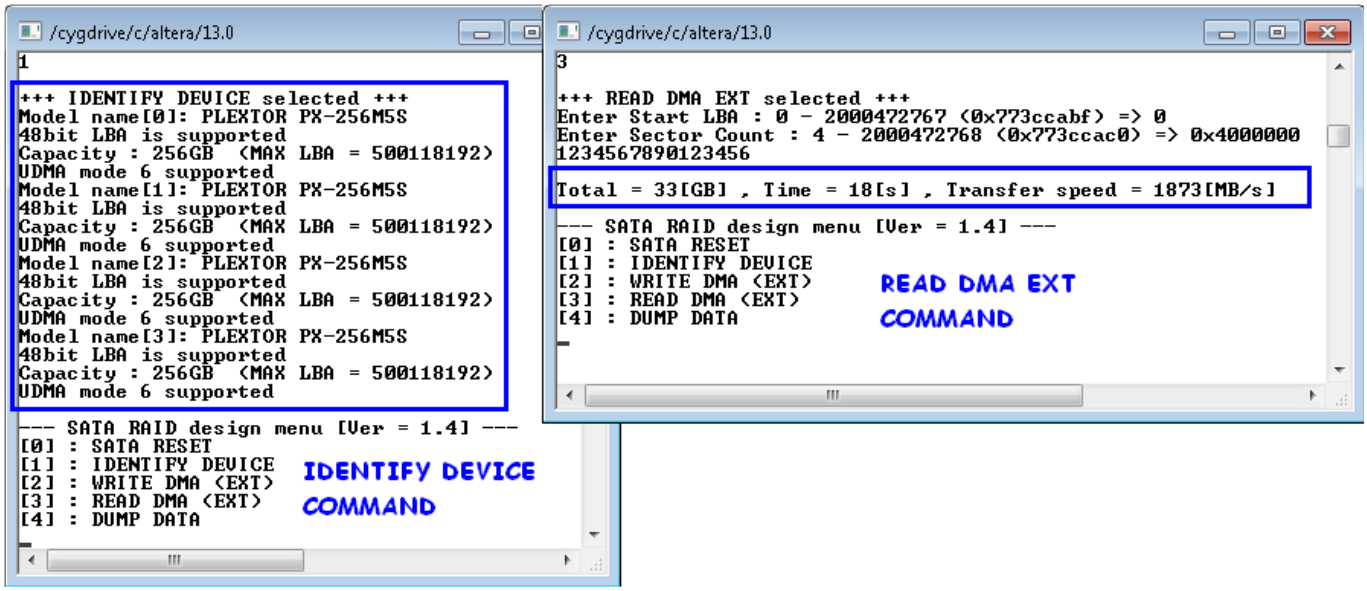

Figure 4 Operation result sample screen

3. Revision History

Revision	Date	Description
1.0	16-Aug-13	Initial Release
1.1	4-Sep-13	Update console