

SATA IP Transport & Link Layer Core

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Product Specification

Rev1.0



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Features

- Compliant with the Serial ATA specification revision 2.6
- Support both of SATA Host and SATA Device (Applicable to SATA Peripheral development)
- Simple transaction interface with Host processor or DMA Engine
- 32-bit internal data path
- 4KB FIFO implemented by BlockRAM in transmit and receive paths
- Support speed auto negotiation for SATA II/I
- Low frequency operation
 - IP Core clock 75.0MHz and PHY clock 150MHz for SATA-II
 - IP Core clock 37.5MHz and PHY clock 75MHz for SATA-I
- CONT primitive support for continue primitive suppression to reduce EMI
- Support 20bit width PHY implemented by Spartan6 GTP
- Reference design available on SP605 (with PCIe2SATA adapter board)

Core Facts	
Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	NGC Netlist
Constraints Files	User constrain file
Verification	Test Bench, Simulation Library
Instantiation Templates	VHDL
Reference Designs & Application Notes	EDK Project, See Reference Design Manual
Additional Items	Demo on SP605
Simulation Tool Used	
Modelsim SE 6.4	
Support	
Support Provided by Design Gateway Co., Ltd.	

Table 1: Example Implementation Statistics

Family	Example Device	Fmax (MHz)	Slices ¹	IOB ²	BUFG/ BUFGMUX	BRAM	MULT/ DSP48	DCM / CMT	MGT	Design Tools
Spartan-6 LXT	XC6SLX45T-3FGG484	227	514	121	3	2	0	1	1	ISE® 11.1.04i

Notes:

- 1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
- 2) Assuming all core I/Os and clocks are routed off-chip
- 3) BUFG/BUFGMUX, DCM/CMT, and MGT resource is not used in SATA IP core, but they are used in SATA PHY design. 2 BUFGMUXs and 1 BUFG are used to support both SATA-I, SATA-II in SATA PHY. 3 BUFGs are used for fixed-speed SATA PHY.

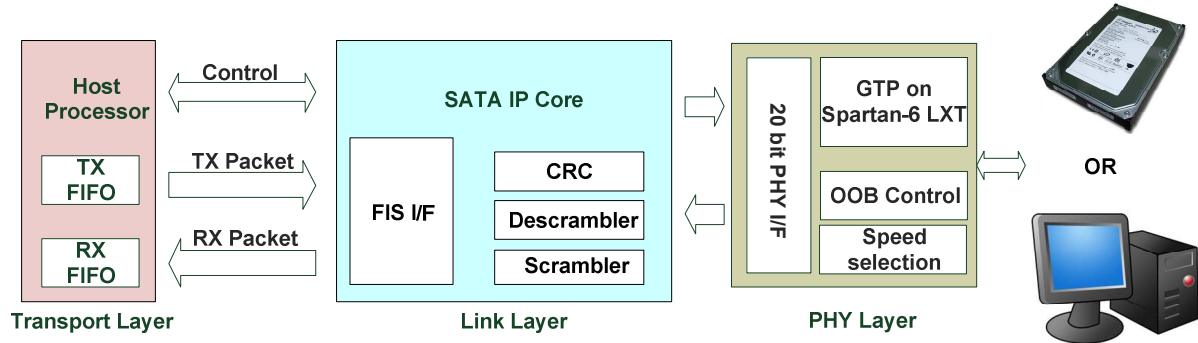


Figure 1: SATA IP Block Diagram

Applications

SATA IP Core is ideal for use in a variety of storage application which require high speed data transfer, cost, scalability and features extensibility such as embedded storage system, RAID controller and High speed and large capacity data acquisition system.

Moreover, the IP also supports SATA Device operation so that SATA Peripherals or SATA Bridge application is also possible.

General Description

The SATA IP Core implements the link layer and some parts of transport layer for communication between upper protocol layer managed by Host processor and PHY layer implemented by Spartan-6 GTP. For Host interface, the IP provides a simple TX and RX transaction interface to transfer data between transport layer and Host processor which are easy to interface with an embedded processor on FPGA (Microblaze). For PHY interface, the IP is designed to support 20-bit PHY interface with 150MHz reference clock for SATA-II 3.0Gbps operation or 75MHz for SATA-I 1.5Gbps operation. (IP Core runs the same operation for both SATA-II and SATA-I. Only clock frequency to synchronous data transferred with SATA PHY is changed)

The SATA IP Core evaluation on SP605 board is possible before IP purchase by using free demonstration bit file. The reference design that describes IP Core communication with transport layer and PHY layer is shipped with IP Core, so that user can easily and immediately start logic design with the SATA IP Core. The reference design that emulates SATA RamDisk as SATA Peripheral Device is also available.

Functional Description

The SATA IP Core is designed to operate under control of a system controller to transfer SATA FIS packet from/to system memory consisted of the following components.

Link Layer

The Link layer transmits and receives frames, transmits primitives based on control signals from the transport layer, and receives primitives from SATA PHY which are converted to control signals to the transport layer.

- **CRC**

The CRC of a frame is a Dword (32-bit) field that shall follow the last Dword of the contents of a FIS and precede EOF primitive.

- **Scramble**

The content of a frame is scrambled before transmission by SATA PHY. Scrambling is performed on Dword quantities by XORing the data to be transmitted with output of a linear feedback shift register (LFSR) by SATA-IP Core.

- **Descramble**

The content of a frame from SATA PHY is descrambled before transmission to transport layer. Descrambling is performed the same ways as scrambling to get FIS.

Transport Layer

The Transport layer constructs frame information structure (FIS) for transmission and decomposes received frame information structures. It also notifies the link layer of the required data flow control, generate status signal for upper layer.

- **FIS Interface**

Provides the interface and data flow control for transmits and receive a transferred transaction with Host.

System Controller

The system controller is typically a host processor that executes application software to communicate with SATA IP Core and handle an upper layer SATA protocol. The system controller may consist of host processor, DMA Engine, TX FIFO and RX FIFO.

SATA PHY

The SATA PHY reference design source code is also provided after purchasing. In this design, it includes "GEN2" port for selecting SATA speed, i.e. '0': SATA-I (1.5Gbps), '1': SATA-II (3.0Gbps). Each Spartan-6 GTP consists of two SATA channels, but this design demonstrates to use only one channel. User needs to implement to use both channels by themselves for RAID application or advance application that requires multiple SATA channels.

Core I/O Signals

Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
Common Interface Signal		
trn_reset	In	Reset SATA IP core. Active high.
trn_link_up	Out	Transaction link up is asserted when the core establish the communication with SATA PHY.
trn_clk	In	Clock which is synchronized with trn_xxx signal for interface with the Host. There is no global clock buffer inside SATA IP core for this signal, so external global clock buffer should be inserted This clock frequency is required to be higher than core_clk frequency.
core_clk	In	IP Core operating frequency output (37.50MHz for SATA-I, 75.00MHz for SATA-II). This clock is generated from SATA PHY.
dev_host_n	In	Device or Host design assignment. '0': ATA Host IP Core, '1': ATA Device IP Core
Transmit Transaction Interface		
trn_tsof_n	In	Transmit Start-Of-Frame (SOF): Indicate start each SATA FIS packet. Active low.
trn_teof_n	In	Transmit End-Of-Frame (EOF): Indicate end each SATA FIS packet. Active low.
trn_td[31:0]	In	Transmit Data: SATA FIS packet data to be transmitted.
trn_tsrc_rdy_n	In	Transmit Source Ready: Indicates that trn_td[31:0] from the Host is valid. Active low.
trn_tdst_rdy_n	Out	Transmit Destination Ready: Indicate that the core is ready to accept data on trn_td[31:0]. Active low. - trn_tsrc_rdy_n must be de-asserted within 4 period of trn_clk after trn_tdst_rdy_n is de-asserted. So the core can accept 4 DWORD of trn_td[31:0] after trn_tdst_rdy_n is de-asserted.
trn_tsrc_dsc_n	In	Transmit Source Abort: Indicates that the Host cancel the current SATA FIS packet. May be asserted any time between SOF and EOF. Active low. - Once asserted, the Core will send out SYNC primitive to abort the current transfer
trn_tdst_dsc_n	Out	Transmit Destination Abort: Indicates that the core is aborting the current SATA FIS packet. Asserted when the physical link is going into reset. Active low.

Signal	Signal Direction	Description
Receive Transaction Interface		
trn_rsof_n	Out	Receive Start-Of-Frame (SOF): Indicate start each SATA FIS packet. Active low.
trn_reof_n	Out	Receive End-Of-Frame (EOF): Indicate end each SATA FIS packet. Active low.
trn_rd[31:0]	Out	Receive Data: SATA FIS packet data to be transmitted.
trn_rsrc_rdy_n	Out	Receive Source Ready: Indicates that trn_rd[31:0] from the core is valid. Active low.
trn_rdst_rdy_n	In	Receive Destination Ready: Indicate that the Host is ready to accept data on trn_rd[31:0]. Active low. - trn_rsrc_rdy_n will be de-asserted within 4 period of trn_clk after trn_rdst_rdy_n is de-asserted. So Host should be supported to accept 4 DWORD of trn_rd[31:0] after trn_rdst_rdy_n is de-asserted.
trn_rsrc_dsc_n	Out	Receive Source Abort: Indicates that the core cancel the current SATA FIS packet. May be asserted any time between SOF and EOF. Active low.
trn_rdst_dsc_n	In	Receive Destination Abort: Indicates that the Host cancel the current SATA FIS packet. Active low. - Once asserted, the core will send out SYNC primitive to abort the current transfer
SATA PHY Interface for Virtex5 GTP		
PHYRESET	In	SATA PHY reset. Active high. This signal is used to reset data buffer interface with SATA PHY when PHY is reset.
PHYCLK	In	Reference Clock for 16-bit SATA PHY (Virtex5 GTP) - 75MHz for SATA-I - 150MHz for SATA-II This clock is generated from DCM inside SATA PHY. It's used for both TX and RX data by elastic buffer in GTP of SATA PHY.
TXDATA[15:0]	Out	16-bit transmit data from the core to the GTP
TXDATAK[1:0]	Out	2-bit Data/Control for the symbols of transmitted data. ("00": data byte, "01": control byte, "1X": undefined).
RXDATA[15:0]	In	16-bit receive data from the GTP to the core.
RXDATAK[1:0]	In	2-bit Data/Control for the symbols of received data. ("00": data byte, "01": control byte, "1X": undefined)
RXDATAVALID	In	Indicates PHY lock and valid data on RXDATA and RXDATAK.
LINKUP	In	Indicates that SATA link communication is established. Active high.
PLLLOCK	In	Indicates that DCM of GTP is locked. Active high.

Timing Diagram

As shown in Figure 2, first data will be transferred by asserting `trn_tsof_n` and `trn_tsrc_rdy_n` after the core is ready by monitoring `trn_tdst_rdy_n` signal. The core can receive up to 4 data from the host after deasserted `trn_tdst_rdy_n`. `trn_td` and `trn_tsrc_rdy_n` are connected to internal FIFO. `trn_teof_n` with `trn_tsrc_rdy_n` are asserted when final data is transferred. After packet is transferred from the Host to the core, the Host will wait to receive error code packet data returned from device to check that all data are received without any error.

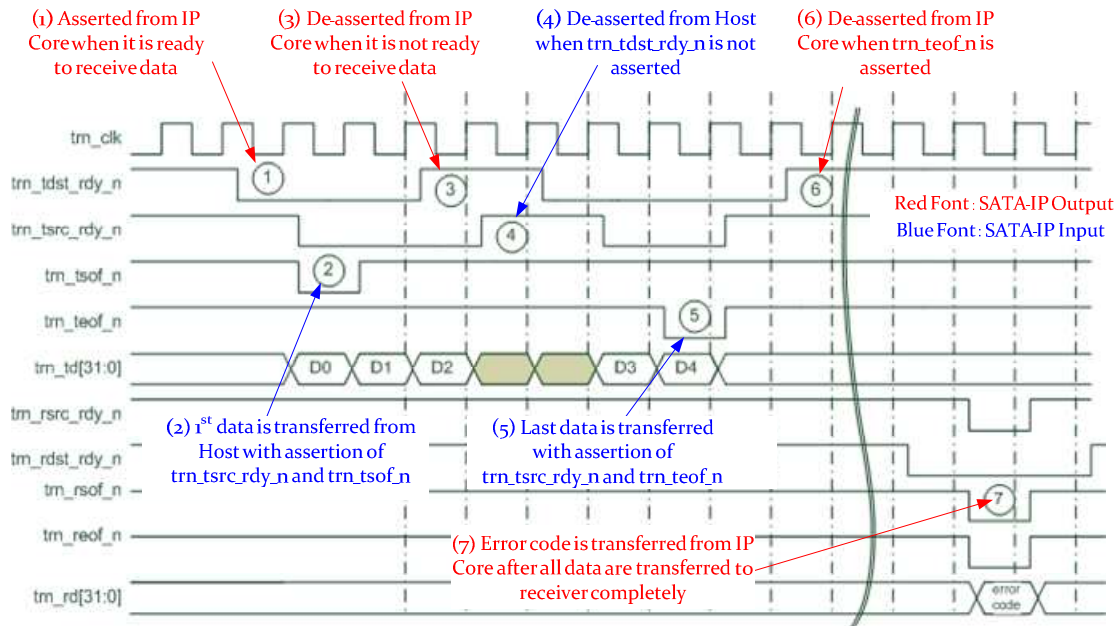


Figure 2: Transmit Transaction Interface Timing

Similar to Figure 2, first data will be transferred from the core after `trn_rdst_rdy_n` signal is asserted. `trn_rdst_rdy_n` signal must be deasserted before data buffer inside the Host is full at least 4 clock period. After packet is transferred from the core to the Host, the Host will wait to receive error code packet data returned from device.

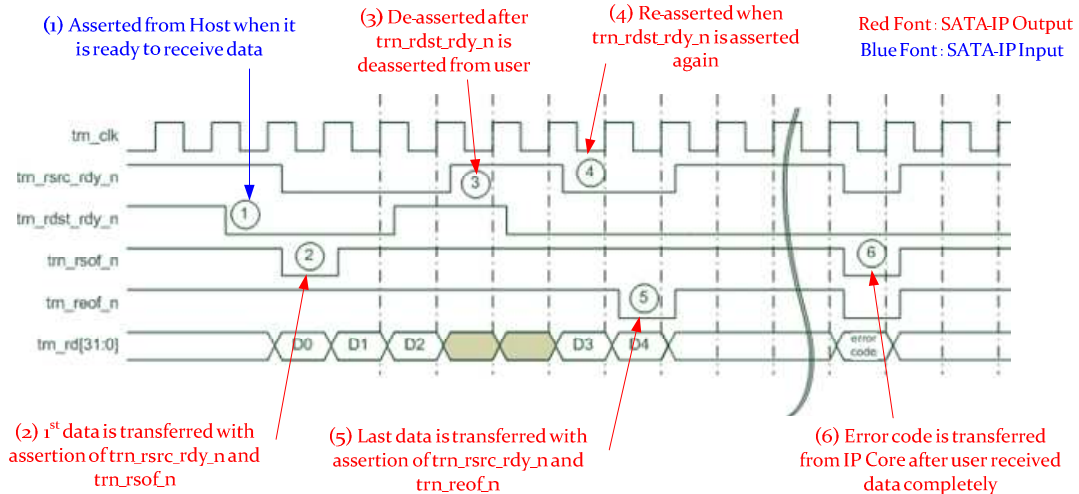


Figure 3: Receive Transaction Interface Timing

Error code which is shown in timing diagram is designed for the Host to check that current data packet can be transferred completely. So, the Host should be checked error code value after end transfer. The detail of error code is shown in Table3.

Table 3: Error code description.

Bit	Signal Name	Description
[31:27]	Reserved	Always zero
[26]	Dir	Current transfer direction flag. '0': From the Host to SATA IP, '1': From SATA IP to the Host
[25:24]	Error	Error code flag. "00": No error, "01": Bad/Unknown SATA FIS packet, "10": CRC error, "11": Reserved. Bad/Unknow SATA FIS packet is found when R_ERR primitive at the end of packet or SYNC primitive during transfer data is received by SATA IP.
[23:8]	Reserved	Always zero
[7:0]	FIS Type	This byte indicates the header of error code packet. "0xEF" is defined to be different from other SATA FIS.

Verification Methods

The SATA IP Core functionality was verified by simulation and also proved on real board design by using SP605 evaluation board.

Recommended Design Experience

Experience design engineers with a knowledge of RocketIO and Xilinx's EDK should easily integrate this IP into their design. For user board development, compliance with design guideline described in UG386 (Spartan-6 FPGA GTP Transceivers User Guide) is strongly recommended.

Ordering Information

This product is available directly from Design Gateway Co., Ltd. Please contact Design Gateway Co., Ltd. for pricing and additional information about this product using the contact information on the front page of this datasheet.

Revision History

Revision	Date	Description
1.0	Jan-19-2010	New release