

SATA-IP Host Demo Instruction on SP605

Rev1.0 21-Jan-10

This document describes SATA-IP Host evaluation procedure using SATA-IP Host reference design bit-file.

1 Environment

For real board evaluation of Host reference design, environment shown in Figure 1 is required.

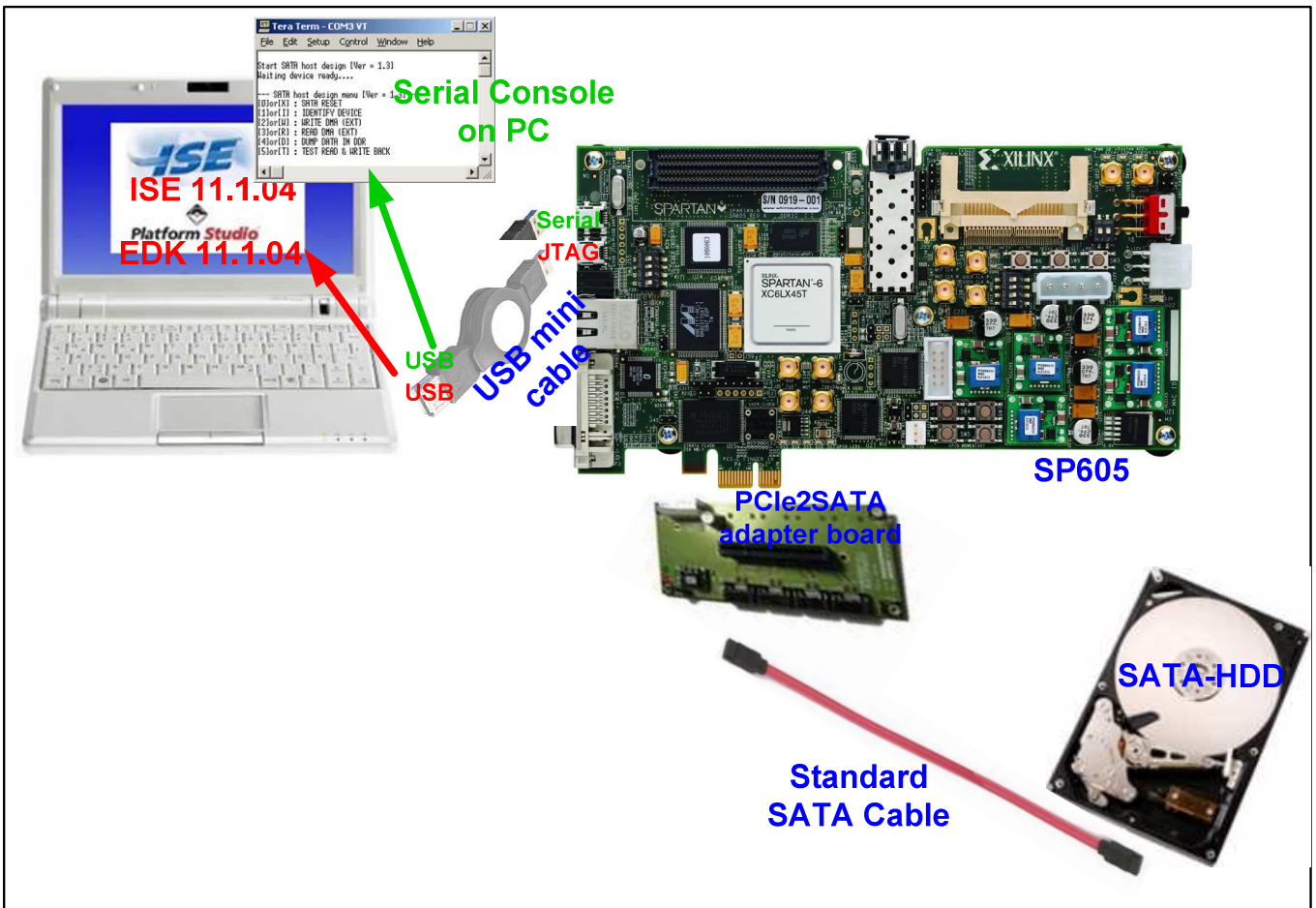


Figure 1 Evaluation environment using reference design bit-file

Note: For evaluation version, IP-Core has 1-hour time limitation to use. After 1-hour use, IP-core will stop any data transfer.

2 Evaluation procedure

- Check all system is power off
- Connect 1st USB mini cable from J4 on SP605 to USB Slot on PC for JTAG programming
- Connect 2nd USB mini cable from J23 on SP605 to USB Slot on PC for Serial Console
- Connect PCIe2SATA adapter board to SP605 board at PCIe connector
- Connect standard SATA cable from SATA Ch#0 on PCIe2SATA adapter board to SATA HDD/SSD
- Set SW[1] at S2 to ON : for connecting SATA-II HDD/SSD, OFF : for connecting SATA-I HDD/SSD, as shown in Figure 2.



Figure 2 The example to set SW for SATA-II speed

- Power up SP605 board and open serial monitoring software such as HyperTerminal. Terminal settings should be (Baud Rate=115,200 Data=8 bit Non-Parity Stop=1).
- Download bit-file to SP605 by using iMPACT Software.
- After FPGA start operation, check GPIO LEDs status on SP605 board at DS3-DS6, next to PCIe connector. All LEDs must be ON for SATA-II and three LEDs are ON for SATA-I, as shown in Figure 3. Each LED description is described as follows.



Figure 3 LED status after system set up complete at SATA-II and SATA-I speed

LED	ON	OFF
DS3	OK	SATA clock cannot lock. Please check OSC 200 MHz at U6 on SP605 board.
DS4	OK	SATA-IP cannot detect SATA device. Please check SATA-cable connection or SATA-cable type that is standard, not cross-cable from Xilinx evaluation board.
DS5	SATA-II	SATA-I
DS6	OK	DDR3 cannot initialize. Please check DDR3 on SP605 board.

Table 1 LED Status of host reference design on SP605 board

Note: All LEDs will be OFF after 1-hour timeout.

- At serial console on PC, main menu will be displayed as shown in Figure 4. Then, user can execute each command operation. Please check serial-cable connection if this menu is not displayed on console.

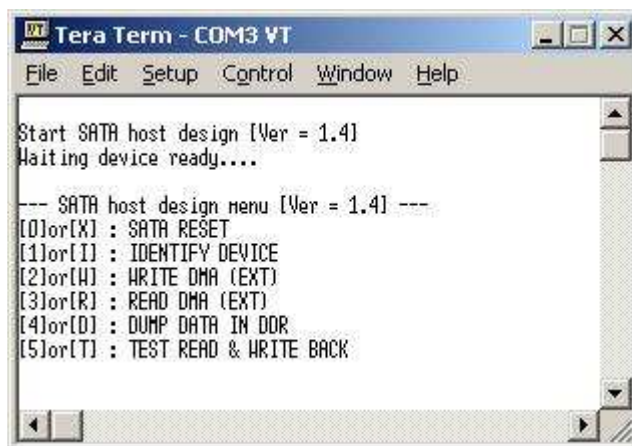


Figure 4 Main Menu of host demo

3 Main Menu

3.1 SATA RESET

Select '0' or 'X' for sending hardware reset signal to SATA-IP. Hardware reset is designed for both SATA-IP and SATA-PHY module. So, SATA initialize process will be started again after sending this reset and "SATA RESET selected" will be displayed, as shown in Figure 5.

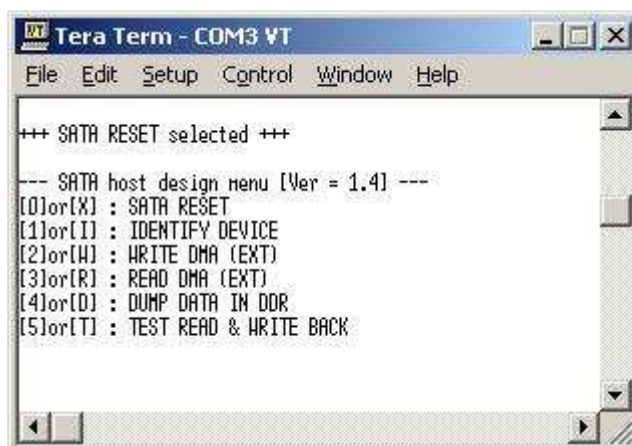


Figure 5 SATA Reset Output

3.2 IDENTIFY DEVICE

Select '1' or 'I' for sending "IDENTIFY DEVICE" command to HDD/SSD. Disk information (Model name, 48-bit LBA supported, disk capacity) will be displayed by using this menu, as shown in Figure 6.

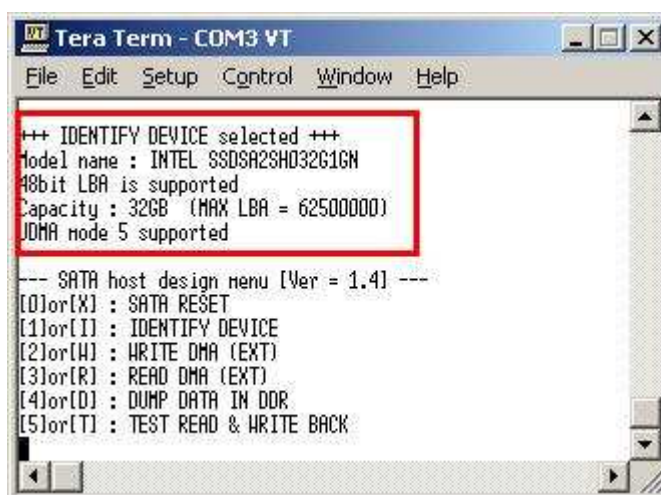


Figure 6 Disk Information from IDENTIFY DEVICE command

3.3 WRITE DMA (EXT)

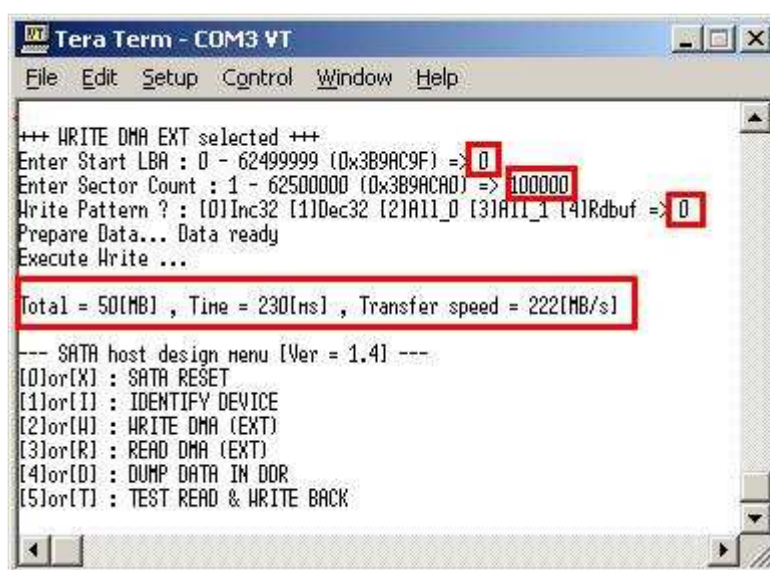
Select '2' or 'W' for sending "WRITE DMA (EXT)" command to HDD/SSD. Three inputs are required for this menu, i.e.

- Start LBA: this value is used to be the sector number of HDD/SSD to start write data to it.
- Sector Count: this value is used to be total transfer size in sector unit (512 byte) to write HDD/SSD. If this value is more than 65536, data written to HDD/SSD will be duplicated every 65536 sectors from write buffer limitation (32 MB).
- Write Pattern: this value is used to select test pattern to write to buffer and HDD/SSD. There are five test patterns in this demo, i.e. 32-bit increment pattern[0], 32-bit decrement pattern[1], 00000000H[2], FFFFFFFFH[3], and current data in read buffer[4].

After Software receives all inputs correctly,

- "Prepare data" will be displayed during CPU writing test pattern data to write buffer.
- "Execute Write" will be displayed during CPU sending WRITE DMA (EXT) command and transferring data from write buffer to HDD/SSD.
- Transfer speed will be displayed after write operation complete.

Figure 7 shows the example of test result when operation complete. Write operation will be canceled from two cases, i.e. receiving error input or receiving any input from user during CPU processing this operation, as shown in Figure 8 and Figure 9.



```

Tera Term - COM3 VT
File Edit Setup Control Window Help
+++ WRITE DMA EXT selected +++
Enter Start LBA : 0 - 62499999 (0x3B9AC9F) => 0
Enter Sector Count : 1 - 62500000 (0x3B9ACAD) => 100000
Write Pattern ? : [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]Rdbuf => 0
Prepare Data... Data ready
Execute Write ...

Total = 50[MB] , Time = 230[ms] , Transfer speed = 222[MB/s]

--- SATA host design menu [Ver = 1.4] ---
[0]or[X] : SATA RESET
[1]or[I] : IDENTIFY DEVICE
[2]or[W] : WRITE DMA (EXT)
[3]or[R] : READ DMA (EXT)
[4]or[D] : DUMP DATA IN DDR
[5]or[T] : TEST READ & WRITE BACK
  
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Figure 7 WRITE DMA (EXT) command input and output

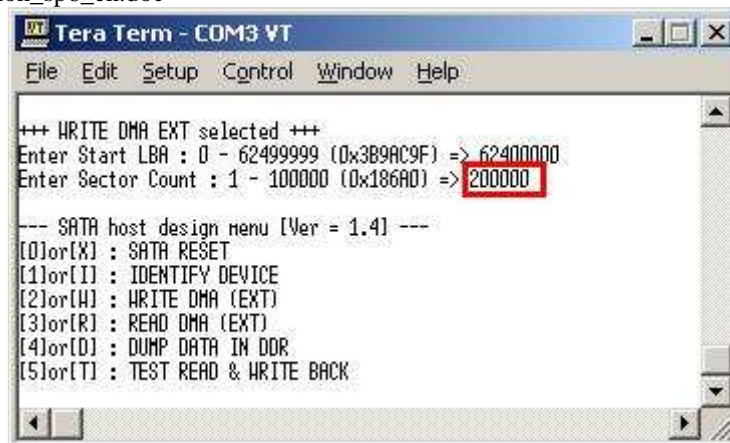


Figure 8 Write Operation canceled from error input

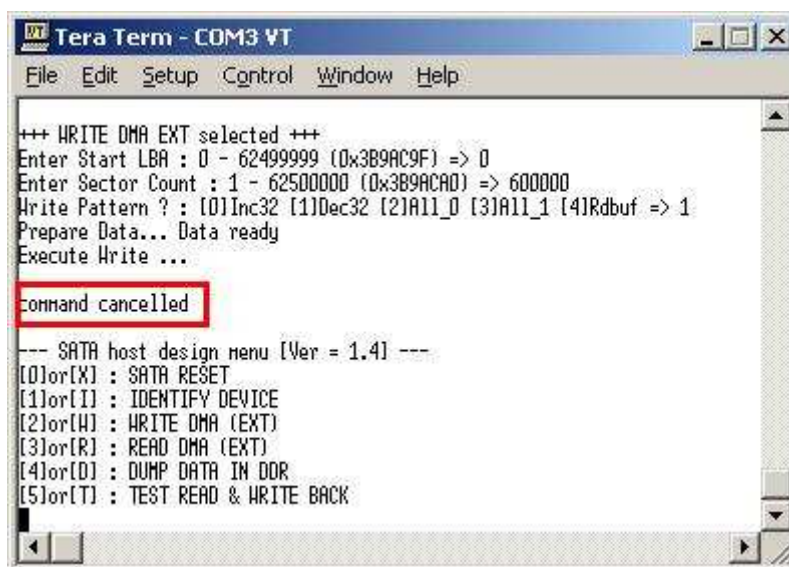


Figure 9 Write Operation canceled from receiving input during operation

3.4 READ DMA (EXT)

Select '3' or 'R' for sending "READ DMA (EXT)" command to HDD/SSD. Two or three inputs are required for this menu, i.e.

- Start LBA: this value is used to be the sector number of HDD/SSD to start read data from it.
- Sector Count: this value is used to be total transfer size in sector unit (512 byte) to read HDD/SSD. If this value is more than 65536 which is read buffer size (32 MB) value, transfer speed will be displayed as output without verify, as shown in Figure 10.
- Verify Pattern: this menu will be displayed if Sector Count is less than 65537. Five verify pattern can be selected, like in WRITE DMA (EXT) menu. "Verify Data ... Success" will be displayed if all data in read buffer is equal to check pattern, but "Data Mismatch with failure value" will be displayed instead if data is not equal, as shown in Figure 11.

Similar to WRITE DMA (EXT) menu, Read operation will be canceled if receiving error input or receiving any input from user during CPU processing, as shown in Figure 12 and Figure 13.

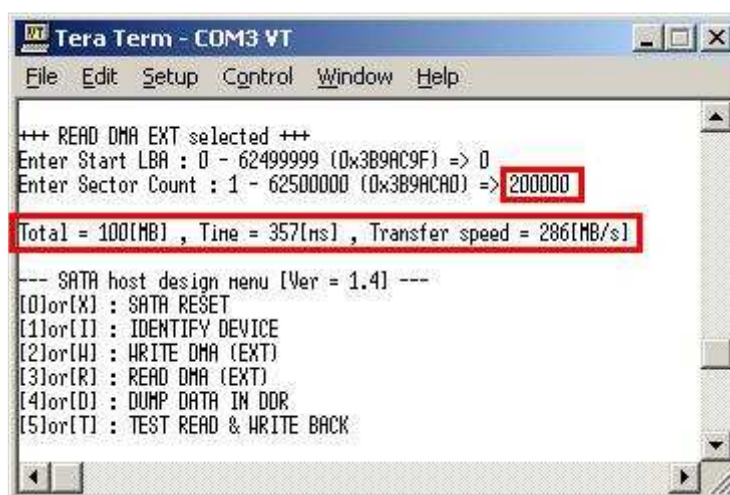


Figure 10 READ DMA (EXT) command without verify

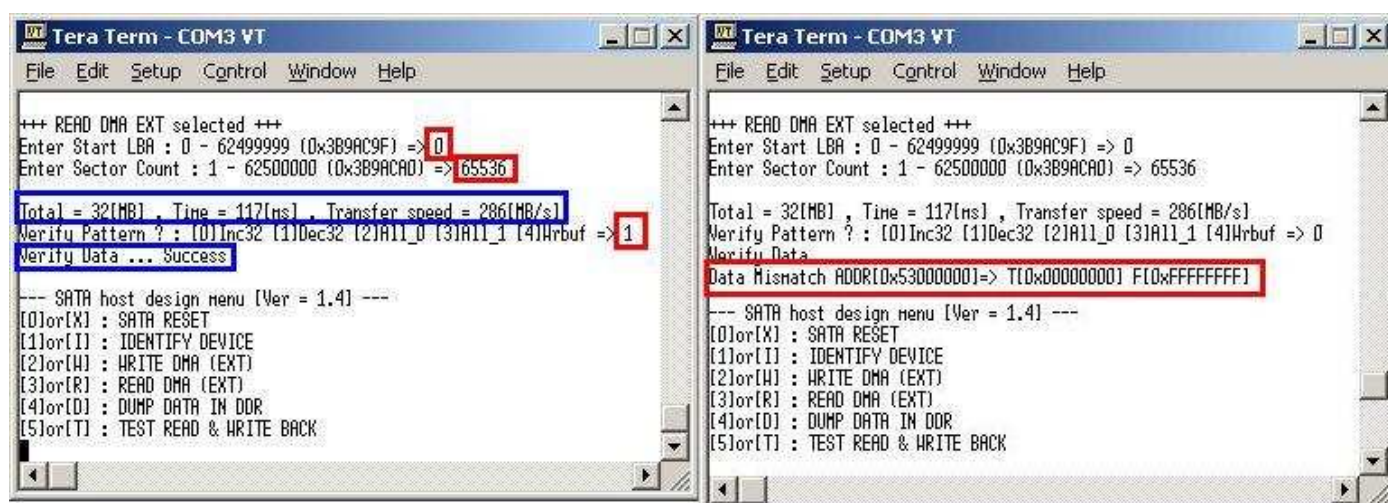


Figure 11 READ DMA (EXT) with verify process

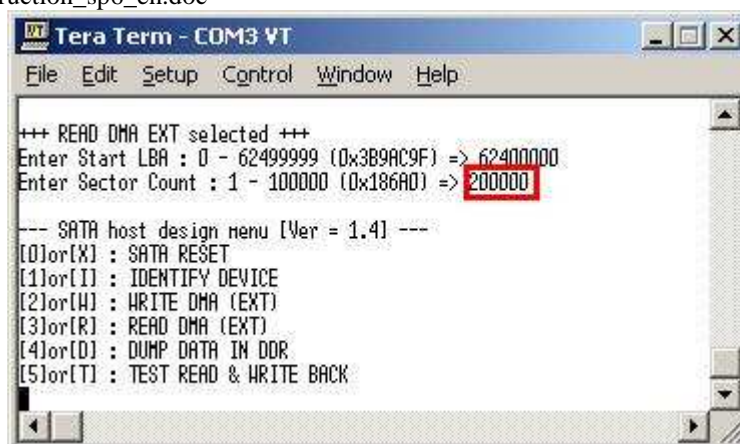


Figure 12 Read Operation canceled from error input

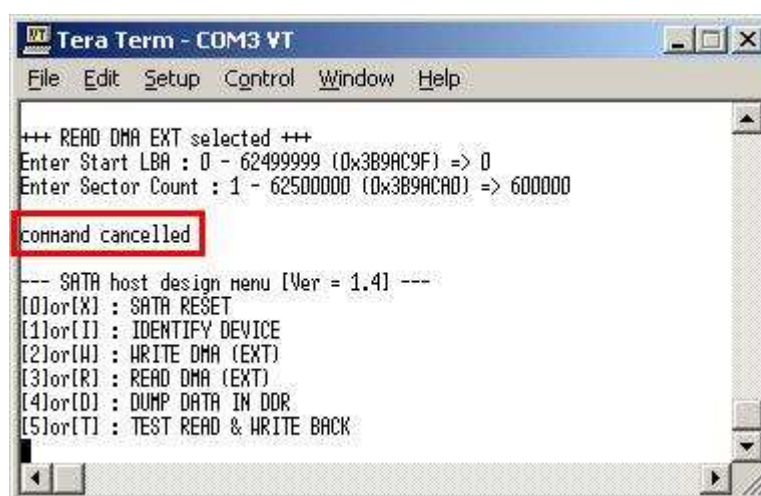


Figure 13 Read Operation canceled from receiving input during operation

3.5 DUMP DATA IN DDR

Select '4' or 'D' to dump data from buffer to display on Serial Console. In this demo, DDR3 is mapped to address = 50000000H-57FFFFFFH. Six submenus can be selected, i.e.

- 'G': this submenu is used to select the address to read, as shown in Figure 14. The address can be input to be hex value by adding prefix "0x", so normally input will be received in decimal value.

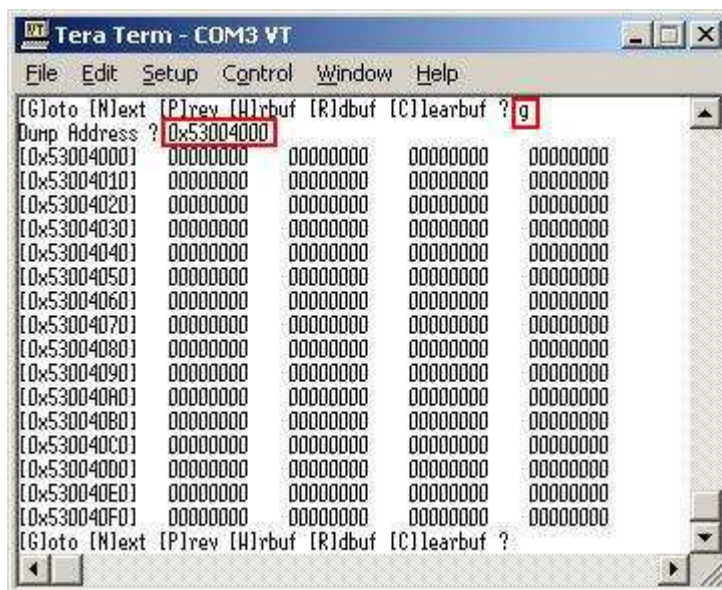


Figure 14 Goto submenu example

- 'N': this submenu is used to read next 256 byte data in buffer, as shown in Figure 15.
- 'P': this submenu is used to read previous 256 byte data in buffer, as shown in Figure 15.

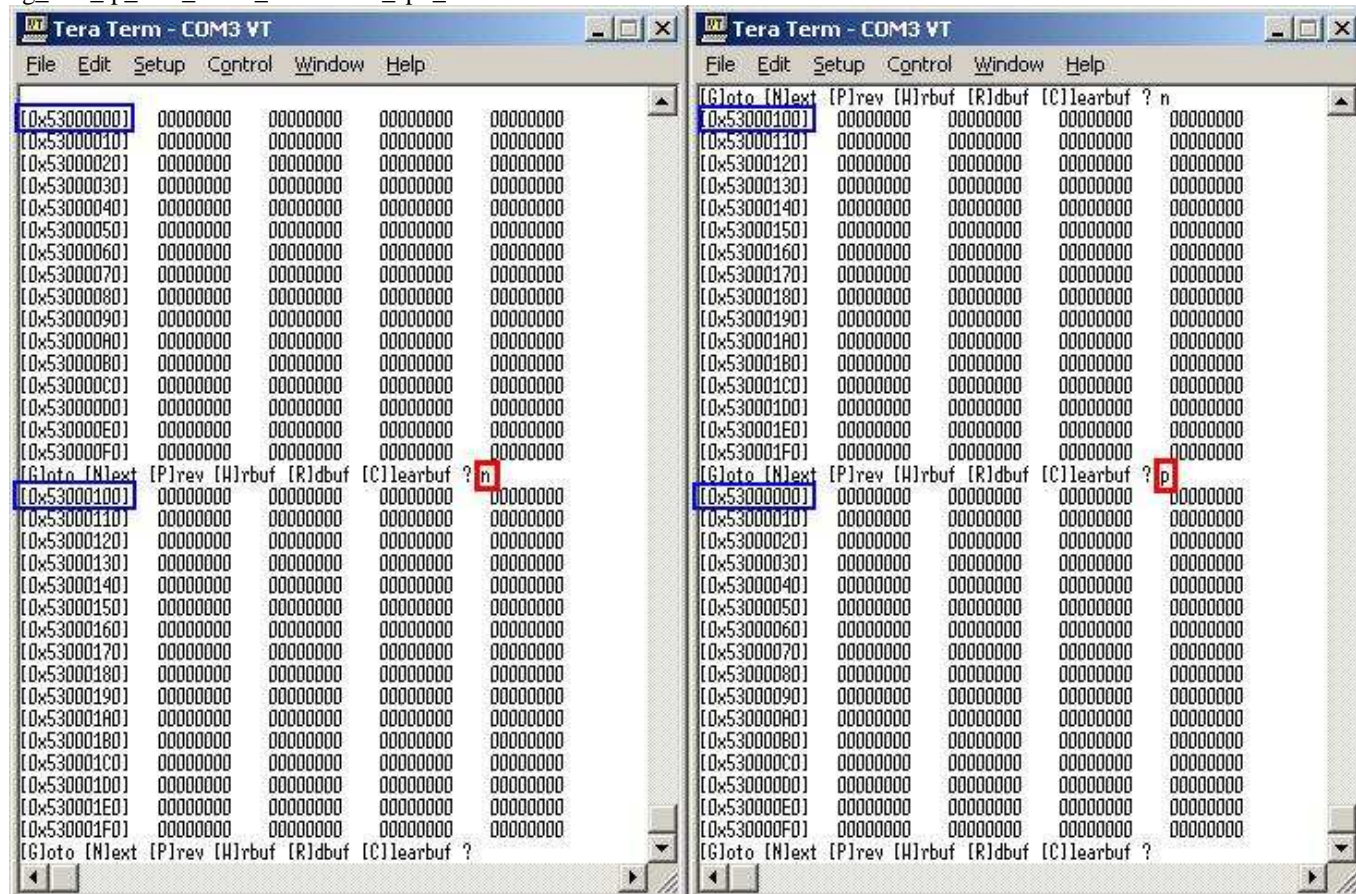


Figure 15 Read Next/Previous 256 byte data in buffer

- 'W': this submenu is used to read 256 byte data at top of write buffer, as shown in Figure 16.
- 'R': this submenu is used to read 256 byte data at top of read buffer, as shown in Figure 16.

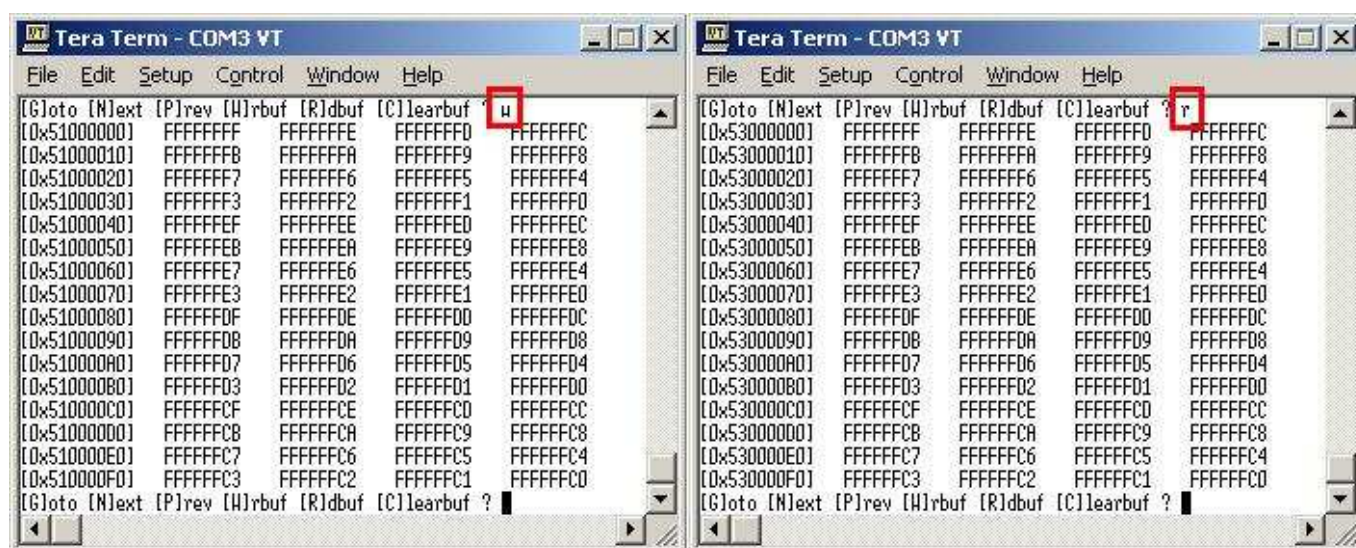


Figure 16 Read 256 byte data at top of write/read buffer

- 'C': this submenu is used to clear data in write/read buffer to be zero value. Select 'Y' to confirm for clear write/read buffer, but user can select 'N' to not clear the current buffer.

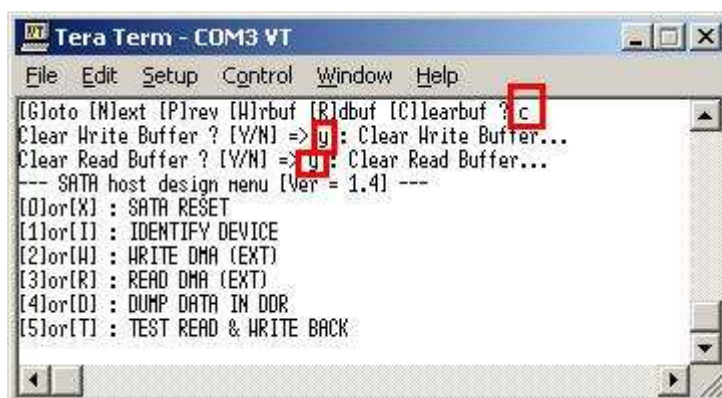


Figure 17 Clear buffer to be zero

User can exit this menu by input other key, such as 'x'.

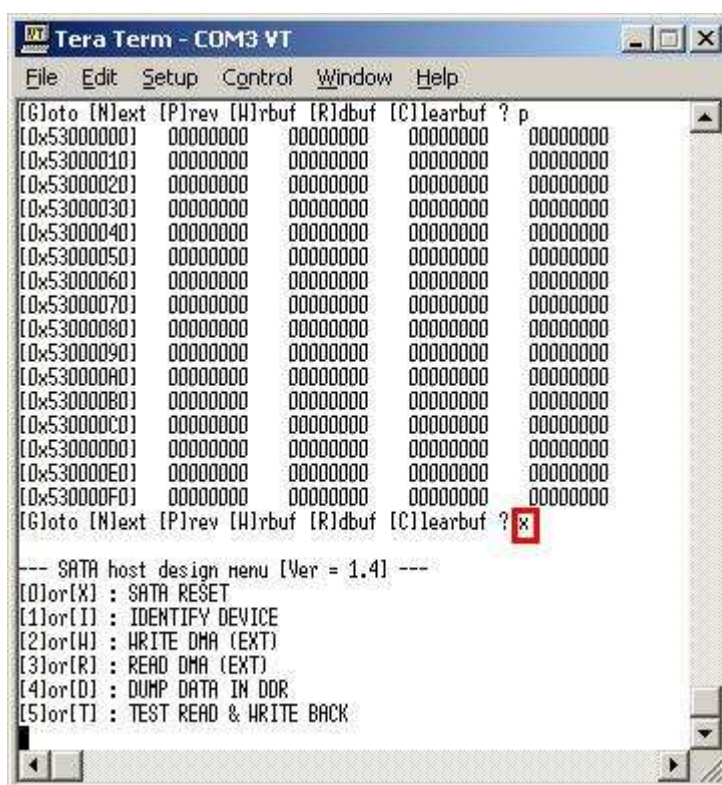


Figure 18 Exit dump menu

3.6 TEST READ & WRITE BACK

Select '5' or 'T' for test sending "WRITE DMA (EXT)" and "READ DMA (EXT)" without fill or verify test pattern. Write and Read speed will be displayed as output for this menu, as shown in Figure 19. Two inputs are required to use this menu, similar to "READ DMA (EXT)".

The test operation will be canceled if CPU receives any input from user during operation.

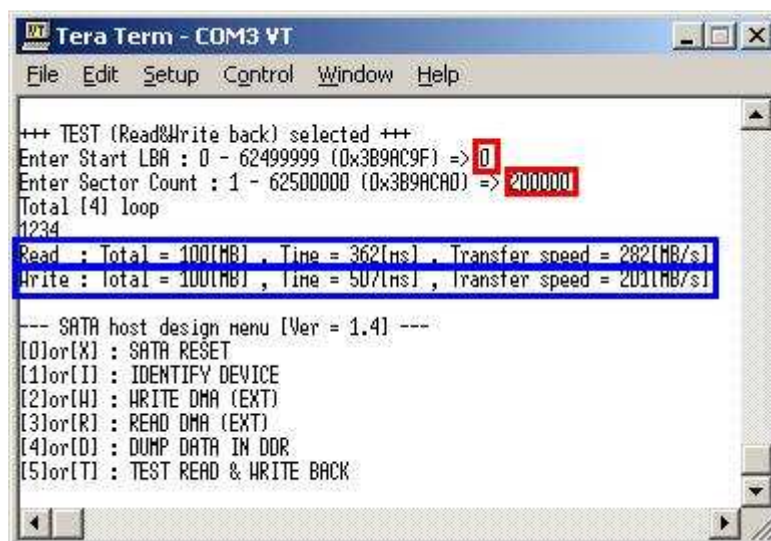


Figure 19 Test Menu Operation

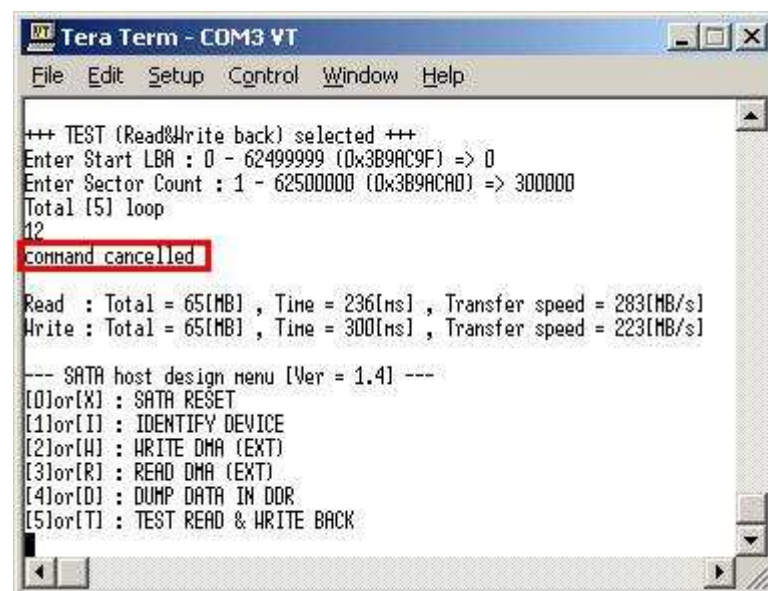


Figure 20 Test Operation canceled

4 Revision History

Revision	Date	Description
1.0	21-Jan-10	Initial version release