SDXC-IP core Introduction

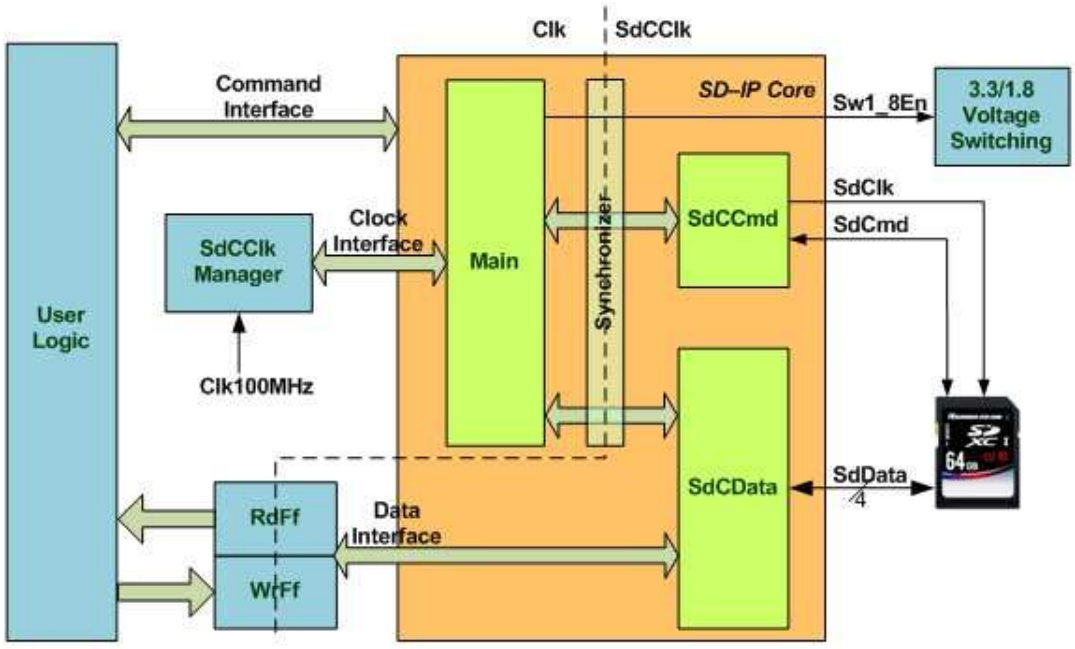
Introduction

SDXC-IP core is compliant with SD Specification Version 3.01 and support SDSC Card, SDHC card, and SDXC card. For speed transfer mode, this core can support SDR12, SDR25, and SDR50 mode (SDR104 soon). DesignGateway provides demo bit file for Xilinx ML505/506 evaluation boards, so you can easily evaluation SDXC-IP core on this board before purchasing. There are three reference designs on both boards, i.e. raw data format for simple interface, FAT32 file system, and exFAT file system. Bit file includes 1-hour time limitation..

Features

- Compliant with SD specification Part 1 (Physical Layer) version 3.01
- Support SDSC/SDHC/SDXC card with auto-detect type
- Support bus speed mode: SDR12 (12.5 MB/s), SDR25 (25 MB/s), and SDR50 (50 MB/s). SDR104 will be supported soon.
- Auto SD clock suspension for power saving
- Auto error checking function
  - Cyclic Redundancy Check (CRC16) for data read transfer
  - CRC status check for data write transfer
  - Timeout when no command response returned from SD card
  - Timeout when SD card is not ready in time during initialization process
- High performance for data transfer by 4-bit SD data transfer mode
- Simple connection for command signal and FIFO interface for data signal
- No global clock and clock management inside it to reduce clock resource for RAID system
- Reference design available on ML505/ML506
  - High performance write/read transfer by raw data formant (no file system)
  - Write/Read transfer in exFAT and FAT32 file system format

Block Diagram



Resources

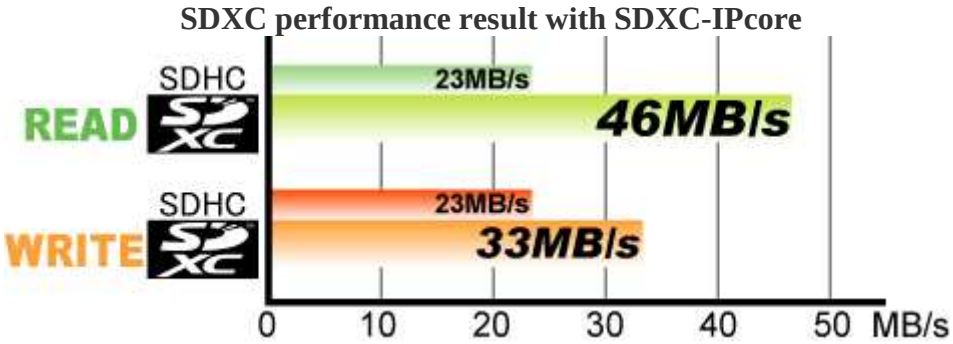
Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family	Example Device	Fmax (MHz)	Slice LUT-FF	Slice LUTS	Slices[1]	IOB[2]	BUFG	BRAM	MULT/ DSP48/E	DCM / CMT	Design Tools
Spartan-6	XC6SLX45-3FGG484	256	733	706	260	134	-	-	-	-	ISE11.5
Virtex-5	XC5VLX50T-1FF1136	344	734	646	249	134	-	-	-	-	ISE11.5
Virtex-6	XC6VLX240T-1FF1136	370	713	699	242	134	-	-	-	-	ISE11.5

Notes:
1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details
2) Assuming all core I/Os and clocks are routed off-chip

Performance

SDXC-IP core supports SDR50 mode (SDR104 released soon) for fully use SDXC card performance



*with Hagiwara HPC-SDX64G10C

Support exFAT & FAT32 files system

SDXC-IP core supports exFAT and FAT32 file system. Data from system using SDXC-IP core will compatible with other system which also support file system. It is effective for system crossing check and easy for data usage to apply with any applications. User can evaluate SDXC-IP core with file system on ML505/506.

*support command: fm, dir, cd, mk, rm, nw, rd, dl, help