

SHA256IP Demo Instruction

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This document describes the instruction to demonstrate the operation of SHA256IP on Arria10SoC development board. This demonstration uses SHA256IP demo software to communicate with development board via 1-Gb Ethernet for set length of data, send input text data, and read hash result. User is also able to use SignalTap to see the operation of provided signals in FPGA.

1 Environment Setup

To operate SHA256IP demo, please prepare following test environment.

- 1) FPGA development boards (Arria10SoC development board)
- 2) Test PC with 1-Gb Ethernet connection.
- 3) Micro USB cable for JTAG connection connecting between FPGA development board and PC
- 4) Ethernet cable (Cat5e or Cat6) for network connection between FPGA development board and PC
- 5) Quartus Prime for programming FPGA, installed on Test PC
- 6) File "SHA256IPDemoPack.zip" that included Test Application named "SHA256IP Demo", configuration file named "SHA256IPTest_time_limited.sof" and SignalTap file named "stp1.stp".

(To download this file, please visit our web site at www.design-gateway.com)



Figure 1-1 SHA256IP demo (FPGA<->PC) on Arria10SoC board



2 PC Setup

Before running demo, please check the network setting on PC. Ethernet setting is shown as follows.

Network and Sharing Center		\bigcirc								
🗧 🔶 👻 🛧 🕎 > Control Pane	el > Network and Internet > Network and	Sharing Center ・ つ Search C								
Control Panel Home	View your basic network informa	ation and set up connections								
Change adapter settings	View your active networks									
Change advanced sharing settings	NetworkAccess type:InternetPublic networkConnections:Image: Ethernet									
	Change your networking settings									
	Figure 2-1 IPv4 setting									

- 1) Open Ethernet setting option from Control Panel -> Network and Internet -> Network and Sharing Center.
- 2) Click Ethernet icon which is used to connect with FPGA board.

Ethernet Status	× Ethernet Properties	×
General	Networking	
Connection No Internet access IPv6 Connectivity: No network access Media State: Enabled Duration: 01:56:55 Speed: 1.0 Gbps Details Activity Sent Sent Received	Connect using: 1-Gb LAN connection Image: Intel(R) Ethemet Connection (7) I219-V Configure This connection uses the following items: Image: Client for Microsoft Networks Image: Client for Microsoft Network Adapter Multiplexor Protocol Image: Client for Microsoft LLDP Protocol Driver Image: Internet Protocol Version 6 (TCP/IPv6) Image: Client for Microsoft Network Adapter Multiplexor Protocol Image: Microsoft LLDP Protocol Driver Image: Internet Protocol Version 6 (TCP/IPv6) Image:	`````
Bytes: 39,299,554 503,073,087	Description Transmission Control Protocol/Internet Protocol. The default wide area network protocol that provides communication across diverse interconnected networks.	
Close	OK Cance	el

Figure 2-2 Select IP address setting menu

- 3) Click Properties button in Ethernet Status window.
- 4) Select "TCP/IPv4".
- 5) Click Properties button in Ethernet Properties window.





 \times

Internet Protocol Version 4 (TCP/IPv4) Properties

General	
You can get IP settings assigned autom this capability. Otherwise, you need to for the appropriate IP settings.	natically if your network supports ask your network administrator
Obtain an IP address automatical	у
• Use the following IP address:	6a
IP address:	192 . 168 . 11 . 81
Subnet mask:	255 . 255 . 255 . 0
Default gateway:	
Obtain DNS server address autom	natically
• Use the following DNS server add	resses:
Preferred DNS server:	
Alternate DNS server:	
Validate settings upon exit	Advanced
	OK Cancel

Figure 2-3 Set IP address

6) Set IP address = 192.168.11.81 and Subnet mask = 255.255.255.0. After that, click OK button to confirm IP address setting.



3 FPGA board setup

- 1) Make sure power switch is off and connect power supply to FPGA development board.
- 2) Connect USB cable between FPGA board and PC via micro USB
- Connect CAT5e/CAT6 cable between PC and Ethernet connection of FPGA board. User must use the right port when FPGA board has two 1Gb Ethernet ports.



Figure 3-1 Power, Ethernet, and micro USB cable connection

- 4) Power on system.
- 5) Open QuartusII Programmer to program FPGA through USB-1 by following step.
 - a) Click "Hardware Setup..." to select USB-BlasterII.
 - b) Click "Auto Detect" and select FPGA device. (10AS066N3).
 - c) Select FPGA device icon.
 - d) Click "Change File" button, select SOF file in pop-up window, and click "open" button
 - e) Check "program"
 - f) Click "Start" button to program FPGA.
 - g) And wait until Progress status is equal to 100%

Programmer - D:/66.Projects/32.SH	_		\times											
(a dit View Processing Tools W	a tit View Processing Tools Window Help													
Ardware Setup USB-Blasteril [USB	Mode:	Mode: JTAG Progress:												
Enable real-time ISP to allow background programming when available														
File	Device	Checksum	Usercode	Program/	Verify	Blank-	Examine	Security	Erase		IPS File			
output_files/SHA256 e>	10AS066N3F40 SOCVHPS	1D3CD247 00000000	FFFFFFFF <none></none>											
Auto Detect	5M2210Z	00000000	<none></none>											
X Delete	510122102	0000000	Shonez											
Add File														
Change File.														
Save File		\rightarrow	-	→	-									
Add Device														
10AS066N3H 1 TDO	40 SOCVH	142	5M22102	5M22	2102									

Figure 3-2 FPGA Programmer



6) When configuration is completed, Quartus will show popup message of OpenCore Plus as shown in Figure 3-3 OpenCore Plus Status. Please do not press cancel button, because NiosII in tCAMIP will stop running.

OpenCore Plus Status	×
Click Cancel to stop using OpenCore Plu	s IP.
Time remaining: unlimite	d
Cancel	

Figure 3-3 OpenCore Plus Status

- 7) When configuration is completed, user can check status LEDs on board as Figure 3-4 • LED#1 is always blink to show clock is working.

 - LED#2 is rstB signal. This LED#2 is related to hardware reset switch "S10".
 - LED#3 is "Connection on" status of TOE1G-IP. This LED is on when software open connection to board.
 - LED#4 is "Ready" status of TOE1G-IP. This LED is on when ethernet connection between PC and board is ready.



Figure 3-4 LEDs status on board



4 SignalTap setup

This designed block diagram of this demo is shown as in Figure 4-1. SignalTap is prepared to see all control signals between SHA256IP and user logics design.



Figure 4-1 Demo environment block diagram

4.1 SignalTap operations

Step to use SignalTap II Logic Analyzer is as follows.

- a) Click File -> Open ..., then select file type to SignalTap II Logic Analyzer Files (*.stp)
- b) Select "stp1.stp", then click Open button as shown in Figure 4-2
- c) As in Figure 4-3, connect FPGA board by select Hardware to USB-BlasterII.
- d) Setup trigger condition to specify signals behavior. Sample of trigger condition and result is shown as in topic 4.2
- e) Click "Run Analysis" button, wait to capture signals from SHA256IP.
- f) The result will be shown, when do SignalTap detect signals same as trigger condition.



Figure 4-2 Open file "stp1.stp"



🥠 Sigi	nalTap II Logic Ar	nalyzer - D:/66.Proj	ects/32.SH	A256/construct	ion/intel/SHA2	56IPTest - SHA2	56IPTest - [stp1	.stp]*						_		×
Elle E	ait <u>v</u> iew <u>P</u> roject	Processing Tool	is <u>vv</u> indow	Пеір						1	\frown			Search alter	a.com	
	<u>्र</u> 🥂 🕷 🛍									_(c					
Instar	r 🖻 🗧	🕽 🔳 🛄 Ready	y to acquire							_ ×	Cha	ain Configur	ration: JTAG	ready		×
Instanc	マノー	Status	Enabled	LEs: 4349	Memory: 87552	Small: 0/18520(Medium: 9/2131	Large: 0/0			Hardware	USB-Bla	eterll [USB_1]		Satu	10
🕄 at	ito_signaltap_0	Not running	\checkmark	4349 cells	87552 bits	0 blocks	9 blocks	0 blocks			riardware.	000-014	atem [000-1]		Oetu	ip
	_										Device:	@1: 10A	S066H1(. ES)/10AS066 -	Scan (Chain
	\frown										>> SOF	- Manager:	1			_
	(f)											managon				
					1											
log: 1	rig @ 2020/11/19 1	2:39:08 (0:0:5.1 elap:	sed)		20 40	0 40	20 40	<u></u>	click to insert tin	me bar	400		400 47	c 400	- 000	004
lype A	lias	Name		•	-32 - 16	<u>y</u> 16	32 48	64	80 96	11Z	148	144	160 17	6 <u>19</u> 2	248	. 224
*	testReg.u_tes	tRegISHA256IP:u_SF	HA256IP[Isto	thEn	1											
	± testReg:u	testRealSHA256IP:u	SHA256IPII	enath[600]					000000000000000000000000000000000000000	0008h						
*	testReg:u tes	tReg SHA256IP:u SH	A256IP bus	v												
*	testReg:u_tes	tReg SHA256IP:u_SH	A256IP has	hValid												
1		testReg SHA256IP:u	SHA256IP	nash[2550]					X							
*	testReg:u_tes	tReg SHA256IP:u_SH	HA256IP ffEn	npty												
a		testReg SHA256IP:u	_SHA256IP f	fWrData[70]	00h					00	h					
-	testReg:u_tes	tReg SHA256IP:u_SH	HA256IP ffWr	En			w									
	⊞⊡testReg:u_	testReg SHA256IP:u	_SHA256IP t	fDataCnt[100]	000h	1 1 1 1 00	Ch 🛄				000h					
Fierarc → ↓	ata Setup hy Display: SHA256IPTest + testReg:u_te SHA256I	× C] Data Log: 🔝 auto_sig	gnaltap_0												×
🕄 aut	to_signaltap_0													0%	6 00 :	:00:00

Figure 4-3 SignalTap II Logic Analyzer



4.2 SignalTap trigger condition

On demo running, user is able to use SignalTap to setup trigger condition and check the signal waveform after trigger is detected. The prepared SignalTap signals are separated to 3 parts as (1) Set length, (2) Data transfer and (3) Hash result, respectively.

4.2.1 <u>To see set length signals timing</u>

Figure 4-4 show trigger condition and Figure 4-5 show sample result from SignalTap when user press hash button in topic 5.2 or 5.3.

trigg	ger: 20	20/11/19 12:34:59 #0	Lock mode:	C Allow all changes	•
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	342	342	1 Basic AND ▼
*		testReg:u_testReg SHA256IP:u_SHA256IP rstB	\checkmark	\checkmark	
*		testReg:u_testReg SHA256IP:u_SHA256IP lengthEn	\checkmark	\checkmark	1
5		testReg:u_testReg SHA256IP:u_SHA256IP length[600]	\checkmark	\checkmark	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
*		testReg:u_testReg SHA256IP:u_SHA256IP busy	\checkmark	\checkmark	
*		testReg:u_testReg SHA256IP:u_SHA256IP hashValid	\checkmark	\checkmark	
5		testReg:u_testReg SHA256IP:u_SHA256IP hash[2550]	\checkmark	\checkmark	xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
*		testReg:u_testReg SHA256IP:u_SHA256IP ffEmpty	\checkmark	\checkmark	
5		testReg:u_testReg SHA256IP:u_SHA256IP ffWrData[70]	\checkmark	\checkmark	XXh
*		testReg:u_testReg SHA256IP:u_SHA256IP ffWrEn	\checkmark	\checkmark	
5		testReg:u_testReg SHA256IP:u_SHA256IP ffDataCnt[100]	\checkmark	\checkmark	XXXh

Figure 4-4 Trigger setup for set length signals

🥠 SignalTap II Logic Anal	lyzer - D:/66.Pro	jects/32.SH	A256/construc	tion/intel/SHA2	56IPTest -	SHA256I	PTest - [stp	1.stp]*								-		×
File Edit View Project	Processing Too	ols Window	Help												Se	arch alter:	a.com	- 5
層 📒 🤈 C 👫 🐽	Þ 😫 😮																	
Instance Manager: 🍡 👂	🔳 🚺 Read	ly to acquire									×	JTAG Cha	ain Configu	uration:	JTAG read	у		×
Instance	Status	Enabled	LEs: 4349	Memory: 87552	Small: 0/	18520(M	edium: 9/213	1 Large: 0/0				Hardwara	USB BI	actorii []	SB-11	-	Sotu	
🕄 auto_signaltap_0	Not running	\checkmark	4349 cells	87552 bits	0 blocks	9 t	locks	0 blocks				Tiardware. USD-Diasterii [USD-1			30-1 <u>]</u>	.j • Setup		
												Device:	@1: 10/	AS066H1	I(. ES)/10A	S066 -	Scan	Chain
												>> SO	F Manage	r. 🚢	0			
log: Trig @ 2020/11/19 12:	30:06 (0:0:29.2 ela	apsed) #1							click to	o insert tim	e bar							
Type Alias	Name	e		-6 -4	-2 ,	9 2	!, 4	, 6,	<mark>8</mark> ,	10 .	12	. 14	16	18	, 2 ₁ 0 ,	22 .	24	26
testReg:u_testR	eg SHA256IP:u_S	HA256IP rstB	3			<u> </u>												
testReg:u_testR	eg SHA256IP:u_Si	HA256IP(leng	then	0000000000	000000000000000000000000000000000000000												_	
testReg.u_test	adSHA256ID:u SI		engin[600]	000000000	0000011	^ <u> </u>				00	00000	1000000000	1					_
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EntestRegru ter	stRegISHA256IP:u	SHA256IPI	nash[255_0]			6A09	E667BB67A	E853C6EE37	2A54EE	53A510E5	27F9B	05688C1E8	3D9AB5B	E0CD19	h			_
testReg:u testR	ealSHA256IP:u SI	HA256IPIffEm	nptv												_			
E testReg:u tes	stRegISHA256IP:u	SHA256IPIf	fWrData[70]			1				00h								_
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E testReg:u_test	stReg SHA256IP:u	_SHA256IPlf	fDataCnt[100]							000h								
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🥦 Data 🛛 🚟 Setup																		
Hierarchy Display:	×	Data Log:	F															×
SHA256IPToct		Duta Log.	analtan 0															
V V = testRegu test	Reg	Tel auto_si	griaitap_0															
SHA256IP:u	u SHA256IP																	
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🕄 auto_signaltap_0																		
																0%	00:	00:00
			Figure	4-5 Sar	nple	resu	ilt for	set le	engt	th sig	gna	als						



4.2.2 To see data transfer signals timing

Figure 4-6 show trigger condition and Figure 4-7 show sample result from SignalTap user press hash button in topic 5.2 or 5.3.

trig	ger: 20	20/11/19 12:34:59 #0	Lock mode:	🌈 Allow all changes	▼
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	342	342	1 → Basic AND →
*		testReg:u_testReg SHA256IP:u_SHA256IP rstB	\checkmark	\checkmark	
*		testReg:u_testReg SHA256IP:u_SHA256IP lengthEn	\checkmark	\checkmark	
- 🛜		testReg:u_testReg SHA256IP:u_SHA256IP length[600]	\checkmark	\checkmark	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
*		testReg:u_testReg SHA256IP:u_SHA256IP busy	\checkmark	\checkmark	
*		testReg:u_testReg SHA256IP:u_SHA256IP hashValid	\checkmark	\checkmark	
- 🛜		testReg:u_testReg SHA256IP:u_SHA256IP hash[2550]	\checkmark	\checkmark	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>
*		testReg:u_testReg SHA256IP:u_SHA256IP ffEmpty	\checkmark	\checkmark	
- 🛜		testReg:u_testReg SHA256IP:u_SHA256IP ffWrData[70]	\checkmark	\checkmark	XXh
*		testReg:u_testReg SHA256IP:u_SHA256IP ffWrEn	\checkmark	\checkmark	1
-		testReg:u_testReg SHA256IP:u_SHA256IP ffDataCnt[100]	\checkmark	\checkmark	XXXh

Figure 4-6 Trigger setup for data transfer

A SignalTap II Logic Analyzer - D:/66.Projects/32.SHA256/construction/intel/SHA256IPTest - SHA256IPTest - [stp1.stp]*														- Gearch alt	era.con	×					
- E2 📮	って ※ 品	K																			
Instance Ma	anager: 🍡 🔊	Read	dy to acquire										×	JTAG C	Chain (Configura	ation:	JTAG rea	ady		×
Instance		Status	Enabled	LEs: 4349	Memo	rv: 87552	Small: 0/	18520	Medium: 9/21	131 Large	0/0										
🔝 auto	signaltap 0	Not running		4349 cells	87552	bits	0 blocks	9	blocks	0 bloc	ks			Hardwa	ire: U	ISB-Blas	sterll [U	JSB-1]			Setup
														Device:	0	01: 10AS	S066H	1(. ES)/10)AS066 -	Sc	an Chain
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log: Trig	@ 2020/11/19 12:3	32:03 (0:0:5.1 elap	psed)		-					- 40	cli	ick to inse	rt time ba	40	00	00			00	00	20
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*	testRegu_testRe	9311A2301F.U_3	HA256IPIlone	, nthEn																	
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-	testReg:u_testRe	g SHA256IP:u_S	HA256IP has	hValid																	
a		tReg SHA256IP:u	J_SHA256IP I	hash[2550]		6A09E667BB67AE853C6EF372A54FF53A510E527F9B05688C1F83D9AB5BE0CD19h										h					
	testReg:u_testRe	eg SHA256IP:u_S	HA256IP ffEn	npty																	
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🔝 auto_	signaltap_0																		C	1%	00:00:00

Figure 4-7 Sample result for data transfer signals



4.2.3 To see hash result signals timing

Figure 4-8 show trigger condition and Figure 4-9 show sample result from SignalTap when user press hash button in topic 5.2 or 5.3.

trig	ger: 20)20/11/19 12:34:59 #0	Lock mode:	Allow all changes	•
		Node	Data Enable	Trigger Enable	Trigger Conditions
Туре	Alias	Name	342	342	1 Basic AND ▼
*		testReg:u_testReg SHA256IP:u_SHA256IP rstB	\checkmark	\checkmark	
*		testReg:u_testReg SHA256IP:u_SHA256IP lengthEn	\checkmark	\checkmark	
5		testReg:u_testReg SHA256IP:u_SHA256IP length[600]	\checkmark	\checkmark	XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
*		testReg:u_testReg SHA256IP:u_SHA256IP busy	\checkmark	\checkmark	
×.		testReg:u_testReg SHA256IP:u_SHA256IP hashValid	\checkmark	\checkmark	1
5			\checkmark	\checkmark	>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>
*		testReg:u_testReg SHA256IP:u_SHA256IP ffEmpty	\checkmark	\checkmark	
5		testReg:u_testReg SHA256IP:u_SHA256IP ffWrData[70]	\checkmark	\checkmark	XXh
×.		testReg:u_testReg SHA256IP:u_SHA256IP ffWrEn	~	\checkmark	
5			~	~	XXXh

Figure 4-8 Trigger setup for input key and searching result

🥍 Signal T	lap II Logic Analy	zer - D:/66.Pro	jects/32.SH	A256/construc	tion/intel/SHA	256IPTest - SH	A256IPTest -	[stp1.stp]*					_		×
File Edit	View Project F	Processing Too	ols Window	Help									Search alter	a.com	- 6
🔤 📮 ') (* 1 🕷 🚵 🕨	12 12													
Instance Ma	nager: 🍡 🔊	Read	ly to acquire								×	JTAG Chain Configuration: J	AG ready		×
Instance		Status	Enabled	LEs: 4349	Memory: 875	52 Small: 0/1852	20 Medium: 9	9/2131 Large: 0/0							
🕄 auto :	signaltap 0	Not running		4349 cells	87552 bits	0 blocks	9 blocks	0 blocks				Hardware: USB-Blasterll [US	B-1] •	Setu	Ip
	De												ES)/10AS066 -	Scan	Chain
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												>> SOF Manager:			
-															
log: Trig (@ 2020/11/19 12:35	5:11 (0:0:11.7 ela	apsed)						click to insert ti	ime bar					
Type Alias	5	Nam	e	-	-1		(1			2			3
-	testReg:u_testReg	g SHA256IP:u_S	HA256IP rstE	3											
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		RealSHA256IP:u	SHA256IPI	hash[2550])	E9CEE71AB932FDE863	38D08BE4DE9DFE39	EA049BDAFB342CE	E659E	C5450B69AEh X			_
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auto_s	ignatap_u														
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Figure 4-9 Sample result for input key and searching result



5 SHA256IP demo software

SHA256IP demo software is used for show hash function that compute by SHA256IP in A10SoC board via 1-Gb Ethernet connection.

5.1 Demo software interface description

	🖳 SHA256IP Demo	—	\times
a	SHA256IP (timeout): 1.00 Connect		
	Hash function by input text		
\frown	hash		
(b	input text abcd1234		
	length : hash		
	Speed test with 64-bit counter pattern data		
\bigcap	Speed Test with 64-bit Counter data size (bytes): 3200000 3200000	0	
Ċ	counter pattern		
	length : hash		

Figure 5-1 Software interface

Figure 5-1 shows SHA256IP demo software and the description is shown as below.

- a) Connect button is used for open connection to A10SoC board via 1Gb-Ethernet.
- b) This section is hash functional test by input text.
- c) This section is speed test function with fixed data pattern by 64-bit counter pattern.



5.2 Hash function by input text

User can input text data and press hash button, then software will transfer input text to SHA256IP and get the hash result back to show in "length : hash" text box. Figure 5-2 shows example of hash function by input text.

🖳 Sha256ip D	- □ >						\times
SHA256IP (timeou	SHA256IP (timeout): 1.00						
Disconnect	Disconnect						
Hash function by	Hash function by input text						
hash	hash						
input text	abcd1234						
length : hash	length : hash 8 bytes : E9CEE71AB932FDE863338D08BE4DE9DFE39EA049BDAFB342CE659EC5450B69AE						
Speed test with 64-bit counter pattern data							
Speed Test wit	h 64-bit Counter	data size (bytes):	32000000	32000000			
counter pattern							
length : hash							



5.3 Speed test with 64-bit counter pattern data

User can input data size (bytes unit), and press "Speed test with 64-bit Counter" button. Then software will show pattern of data in counter pattern text box and send command to A10SoC board to start generate test pattern data send to SHA256IP. After hash function is finished, software will get the result hash value and show in "length : hash" text box. Then software will popup message to show time of hash function operation. Figure 5-3 shows example of speed test with 64-bit counter pattern data.

💀 SHA256IP D	emo			,	- 🗆	X	
SHA256IP (timeo	ut): 1.00		[
Connect						^	
Hash function b	y input text			data size (bytes time (seconds):): 32000000 0.164		
input text	xt abcd1234 h 8 bytes : E9CEE71AB932FDE863338D08BE4DE9DFE39EA049BI			ві ок			
length : hash							
Speed test with	64-bit counter patte	m data	1				
Speed Test wit	th 64-bit Counter	data size (bytes):	32000000	32000000			
counter pattern	hex : 000000000	00000 01000000000000 020000000000000 increment until			FF083D0000	0000000	
length : hash	32000000 bytes : 1CA554E6F0817062B6B4765BFF7F52A425811534A636D112157934704156FE15						

Figure 5-3 Example of speed test with 64-bit counter pattern data



6 Revision History

Revision	Date	Description
1.00	26-Jan-2021	Initial version release