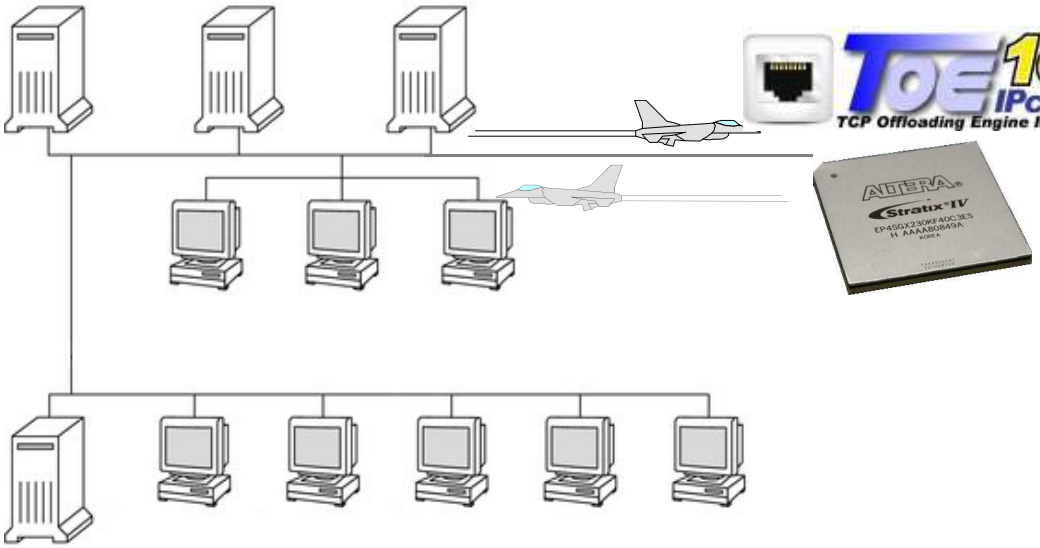
TOE1G-IP Introduction (Altera)

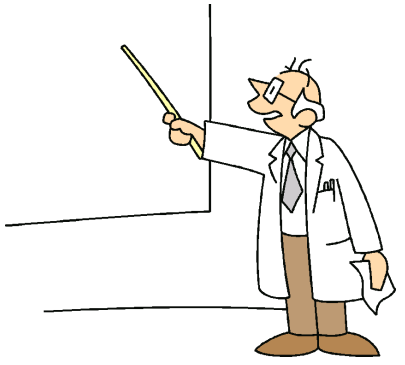
Ver1.4E



Extreme TCP Speed on GbE

Agenda

- Advantage and Disadvantage of TCP on GbE
- TOE1G-IP core overview
- TOE1G-IP core description
  - Initialization
  - High-speed transmit
  - High-speed reception
- User I/F, Buffer size parameterization
- Reference design
- Resource usage and real performance

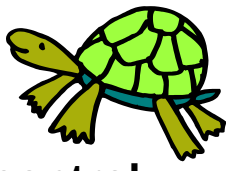


Advantage of TCP/IP on GbE

- **Advantage of GbE (Giga-bit Ethernet)**
  - **1Gbps speed in theoretical maximum**
  - **Any PC furnishes GbE port**
  - **Popular in the market, very low cost**
- **Advantage of TCP/IP**
  - **Standard Ethernet protocol**
  - **Guaranteed data reliability**
  - **Major OS provides protocol stack**

Disadvantage of TCP/IP on GbE

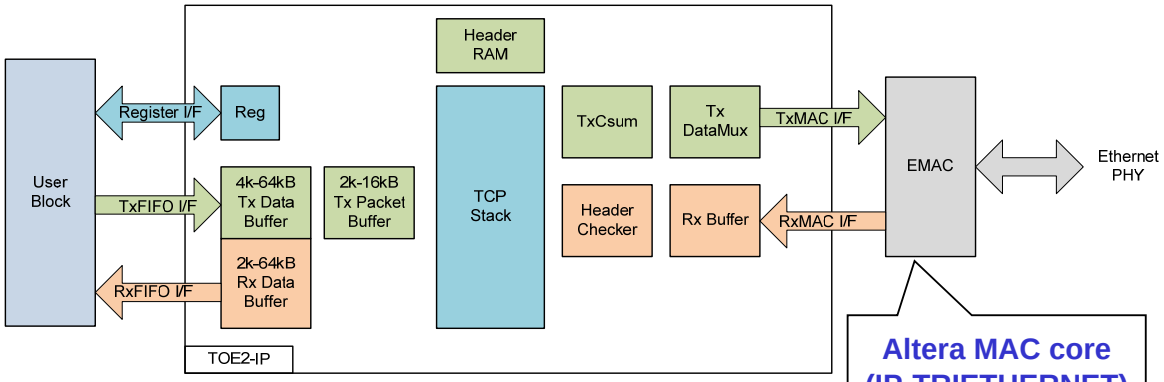
- **Poor Performance**
  - **Complicated protocol management**
  - **Necessary high-performance CPU for TCP control**
  - **Practical speed is around 300Mbps at maximum**
- **Requires expensive High performance CPU**
  - **FPGA internal CPU (NiosII) is not enough**
  - **Needs external high-performance but expensive CPU**
  - **If use SoC, TCP consumes most CPU resource**



TOE1G-IP core can provide ideal solution!

TOE1G-IP core Overview

- 2nd generation TCP/IP off-loading engine core
- Inserts between user logic and Altera EMAC module
- Fully hard-wired TCP control for both Tx and Rx
- Supports Full Duplex communication



TOE1G-IP core block diagram

TOE1G-IP core Advantage 1

- Fully hard-wired TCP/IP protocol control
  - Possible to build CPU-less network system
  - Zero load for CPU

- Support all of Tx only, Rx only, and full-duplex
  - 110MByte/sec speed for half-duplex mode
  - 100MByte/sec speed for full-duplex mode

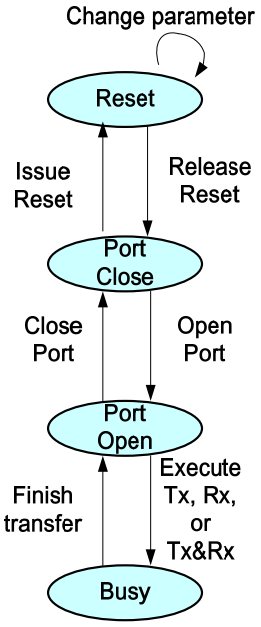
- Guarantee transfer data reliability
  - Tx: Automatic retry when No-ACK, Duplicate-ACK, timeout
  - Rx: Automatic ACK control by Sequence number calculation

TOE1G-IP core Advantage 2

- **Selectable data buffer size**
  - Selectable buffer size of memory usage vs. performance
- **Compatible with Altera MAC core (IP-TRIETHERNET)**
  - Direct connection between TOE1G-IP and EMAC
- **Many reference design on Altera evaluation board**
  - Full QuartusII project for standard Altera board
  - Free bit-file for evaluation before purchase
  - All source code (except IP-core) in design project
  - 2 port of TOE1G-IP (fast) + CPU (slow) design
  - FTP server sample design using TOE1G-IP core and CPU

TOE1G-IP core Operation

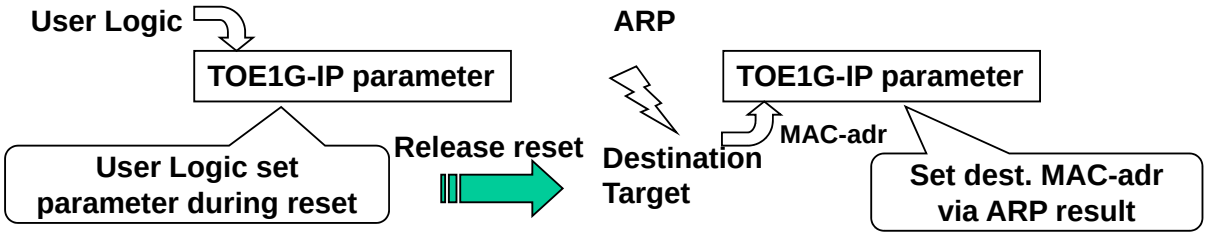
- **Set parameter (IP-adr&MAC-adr, etc) during Reset**
- **Release Reset then initialize including ARP**
- **Idle state after initialization finish, wait command**
- **Port open by either of Active (Client) or Passive (Server) mode**
- **Tx and Rx operates individually (full-duplex)**
- **If want change parameter, move to Reset state (transfer/packet length can change except Busy)**



State Diagram

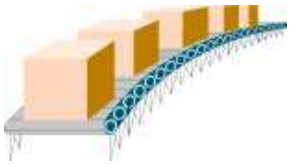
TOE1G-IP Initialization

- Set parameter to TOE1G-IP
  - User logic can set parameter during TOE1G-IP reset
  - Set IP address, MAC address, and Port number
  - Release reset after parameter setting finish
- TOE1G-IP executes ARP after reset release
  - Issue ARP to destination target
  - Get MAC-adr of the target via ARP result



High-Speed Tx

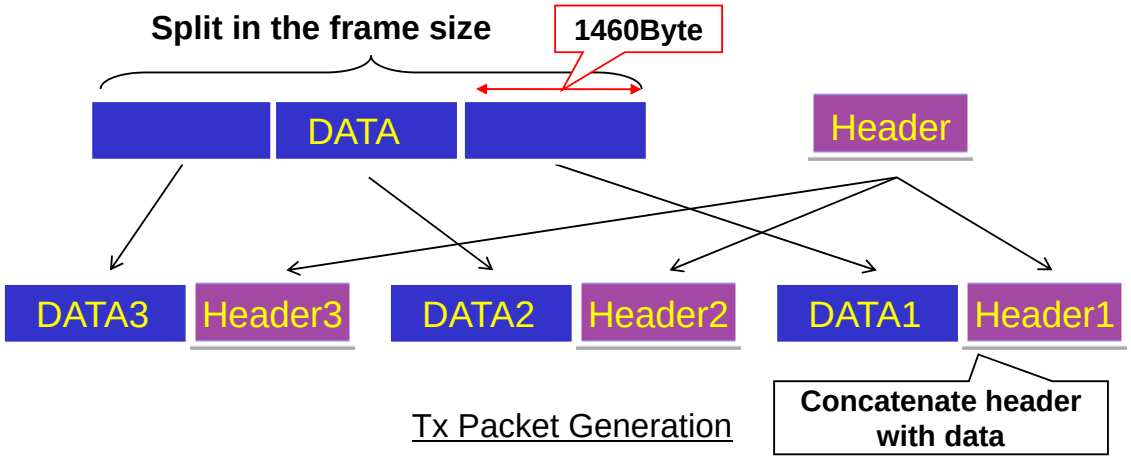
- Tx packet generation
  - User Logic writes Tx data to TxFIFO
  - Split Tx data in the frame size
  - Concatenate header with Tx data



- Automatic retransmit function
  - Check ACK reply from destination
  - Detect No-ACK, Duplicate-ACK, and Timeout
  - Resend same packet by such ACK error detection

Tx Packet Generation

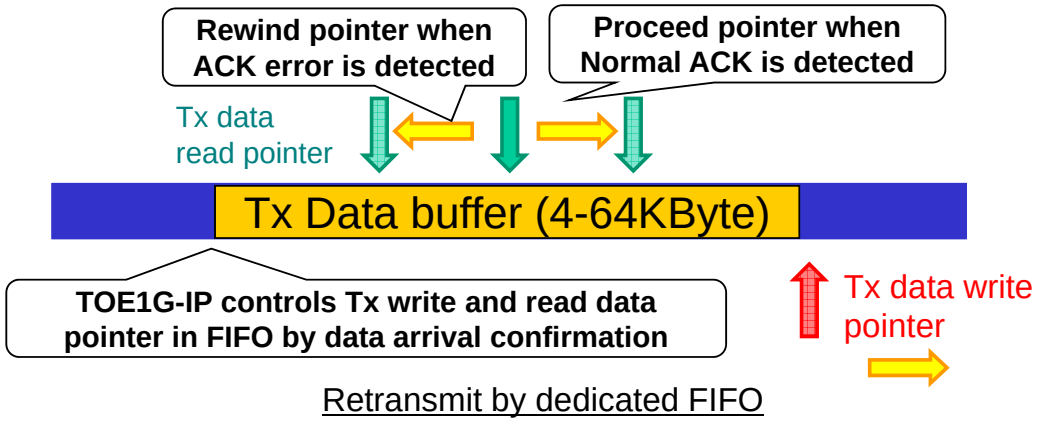
- **Generate header and concatenate it with Tx data**
  - **TOE1G-IP splits Tx data in the frame size**
  - **Generate checksum and sequence number in TOE1G-IP**



Tx Packet Generation

Automatic retransmit

- **Retransmit function by dedicated FIFO**
  - **Proceed pointer by normal ACK reception**
  - **Rewind pointer by illegal ACK reception**
  - **TOE1G-IP controls pointer and retransmit operation**



Retransmit by dedicated FIFO

High-Speed Rx

- **Rx packet header check**
  - Ignore packet if destination is not TOE1G-IP or if checksum is wrong
- **Data reordering**
  - Reorder when sequence number skip is detected
  - Avoid retransmit request for transfer efficiency
  - If reordering is not possible, then send duplicate ACK

- **Duplicate data management**
  - Check duplicate data in Rx packet
  - Retrieve original data by trimming duplicate data part

- **Flow control**
  - Automatic Window Update packet sending

Rx Packet Header Check

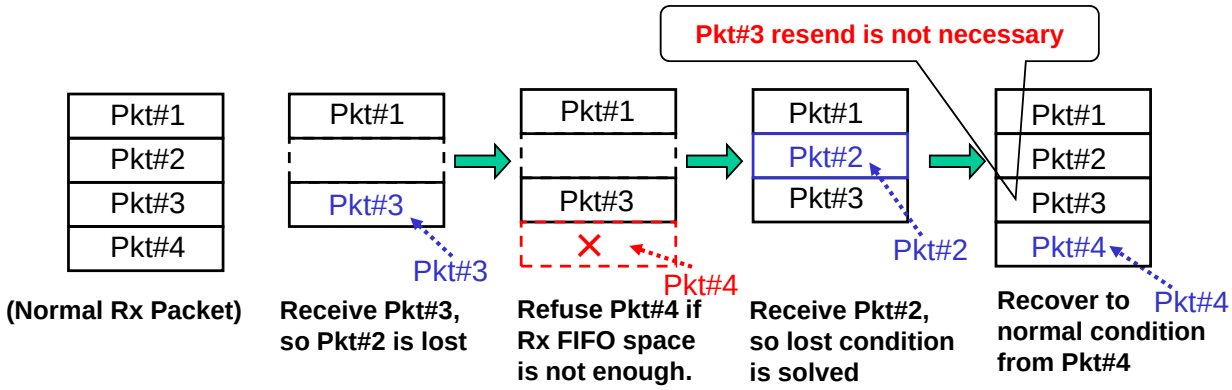
- **Verify header check sum in Rx packet**
  - Also check following condition in TOE1G-IP

Byte Offset	Protocol	Description	Check condition
0-5	ICMP	Destination MAC adr	Match with MAC adr set by SML/SMH register
6-11	ICMP	Source MAC adr	Match with target MAC adr set by ARP
12-13	ICMP	Type	= 0x0800 (IP packet)
14	IP	Version/Header	= 0x45 (IPv4, IP header len=20)
20	IP	Flag/Fragment OFS	= b"000000" (no fragment)
23	IP	Protocol Number	= 0x06(TCP packet)
26-29	IP	Source IP adr	Match with IP adr set by DIP register
30-33	IP	Destination IP adr	Match with IP adr set by SIP register
34-35	TCP	Source port number	Match with DPN register or extracted target port number in Passive Open
36-37	TCP	Destination port number	Match with port number set by SPN register
38-41	TCP	Sequence number	Possible value within TOE2-IP core can process this packet

Header check condition in Rx packet

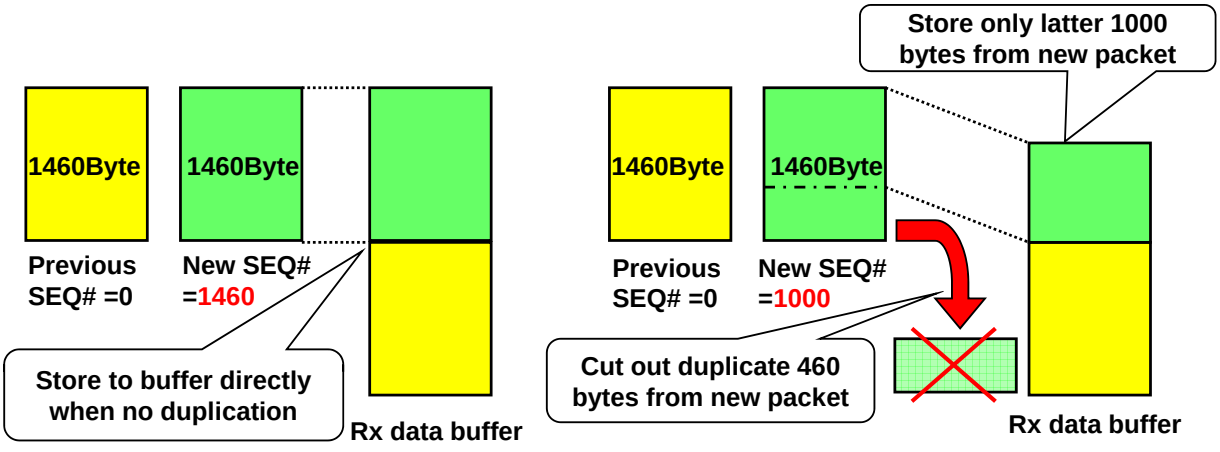
Data Reordering

- **Function when SEQ number skip is detected**
  - **Not accept any packet other than that can solve lost condition**
- **Data reordering function**
  - **Recover data contiguous from lost-solved packet**
  - **Keep performance by suppress resend request**



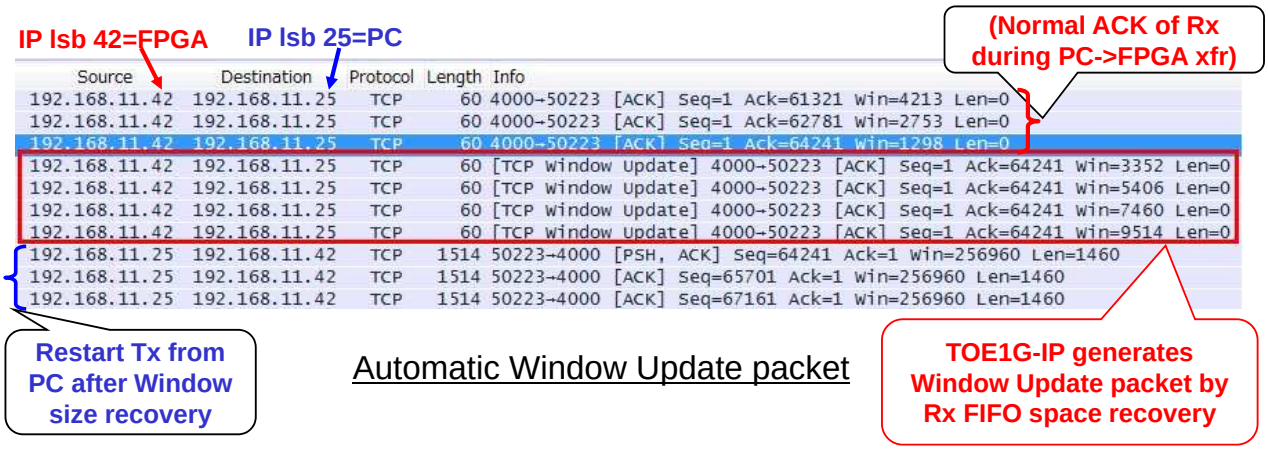
Duplicate data trimming

- **Detect data duplication and correct automatically**
  - **Detect Rx data duplication by checking sequence number**
  - **Trim duplicate block and retrieve contiguous data**



Flow Control (Automatic Window Update transmit)

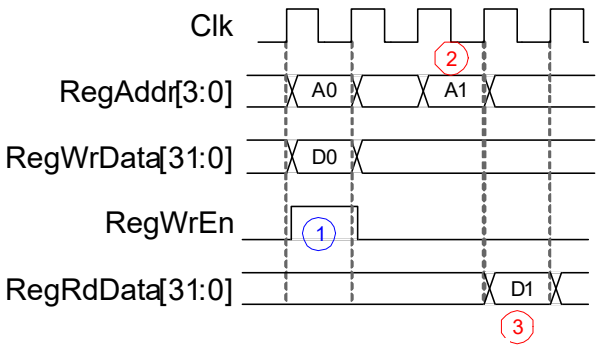
- **Generates TCP Window Update (ACK) packet**
  - Detect available space recovery in Rx data buffer
  - Send Window Update packet when space exceeds threshold
  - PC side can restart Tx operation by Window Size recovery



Automatic Window Update packet

User Interface (Control)

- **3 types of Register I/F, Tx FIFO I/F, and Rx FIFO I/F**
  - Register I/F for initial parameter setting and Tx/Rx command
  - Tx FIFO I/F and Rx FIFO I/F is standard FIFO interface

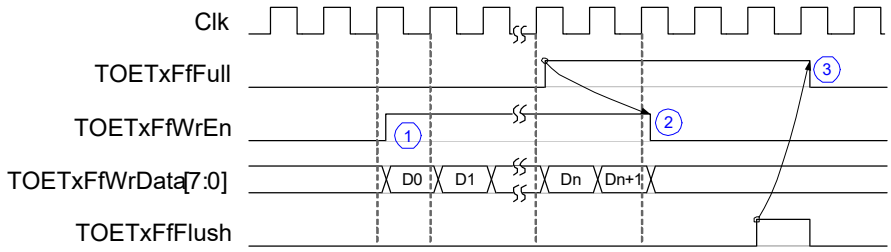


Register I/F timing

[Register Write]
(1) Assert RegWrEn with RegAddr and RegWrData

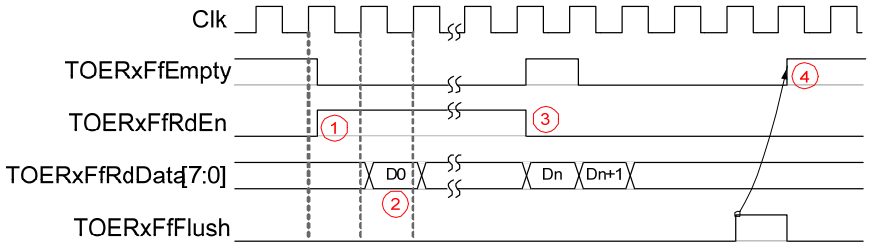
[Register Read]
(2) Set RegAddr
(3) Valid RegRdData output in the next clock

User Interface (Data)



[Tx data write]
(1) Write data with WrEn
(2) Suspend write within 4 Clk after Full assertion
(3) FIFO clear by Flush

Tx FIFO I/F timing



[Rx data read]
(1) Read by RdEn assertion when not Empty
(2) Read data after 1 Clk
(3) Read is inhibited when Empty
(4) FIFO clear by Flush

Rx FIFO I/F timing

Buffer Capacity

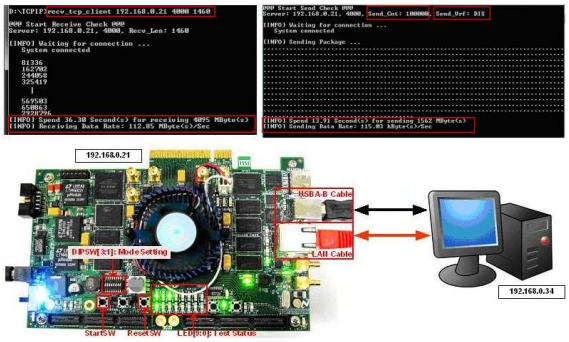
- **Parameterized 3 types of data buffer**
  - **(1) Tx Data Buffer: 4KByte - 64KByte**
  - **(2) Tx Packet Buffer: 2KByte - 16KByte**
  - **(3) Rx Data Buffer: 2KByte - 64KByte**
- **User can optimize resource usage and performance**

Generic Name	Range	Description
TxBufBitWidth	12-16	Set Tx data buffer size in address bit width When set to 12, size is 4KByte, when 16, 64KByte for example.
TxPacBitWidth	11-14	Set Tx packet buffer size in address bit width When set to 11, size is 2KByte, when 14, 16KByte for example
RxBufBitWidth	11-16	Set Rx data buffer size in address bit width When set to 11, size is 2KByte, when 16, 64KByte for example.

Buffer size is selectable by parameterization

Free SOF File for Evaluation

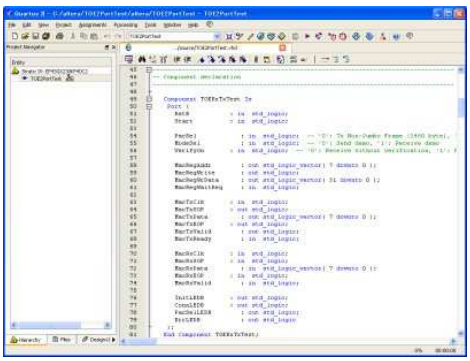
- **SOF file for evaluation with Altera standard board**
  - **Ready for ArriaV GX/StratixIV GX/Arria10SoC/CycloneV E Development kit**
  - **Support both Half-Duplex and Full-Duplex operation**
  - **Measure transfer speed performance and data reliability**
  - **2 port (Fast+Slow) operation, FTP sample application**



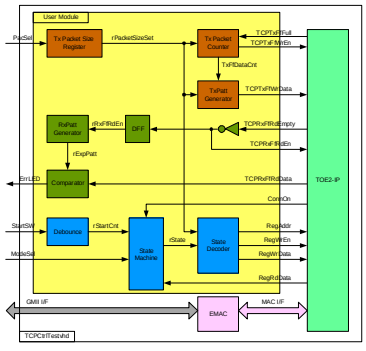
Evaluation environment for Altera board

Reference Design Overview

- **QuartusII design project for real operation**
  - **All source code (except IP-core) included in full project**
  - **Both half-duplex and full-duplex design in IP-core package**
  - **2 port design and FTP design available for IP-core customer**



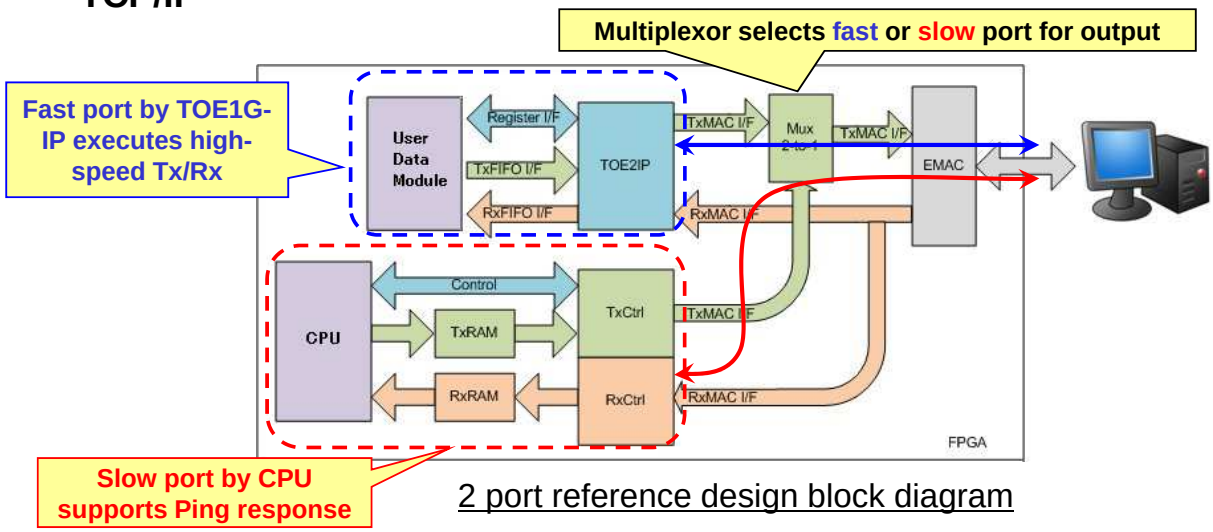
QuartusII project in package



Reference design block diagram

Reference Design（2 Port Design)

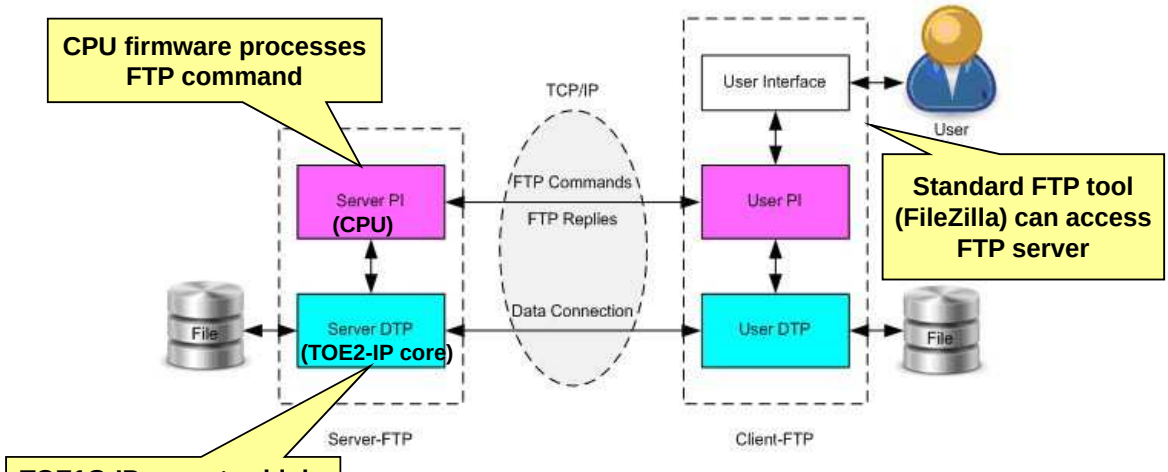
- Implements 2 port of fast port by TOE1G-IP and slow port by CPU
- Data Tx and Rx for fast port and 'Ping' command for slow port
- Emulates real product that requires more protocol other than TCP/IP



2 port reference design block diagram

Reference Design（FTP sample)

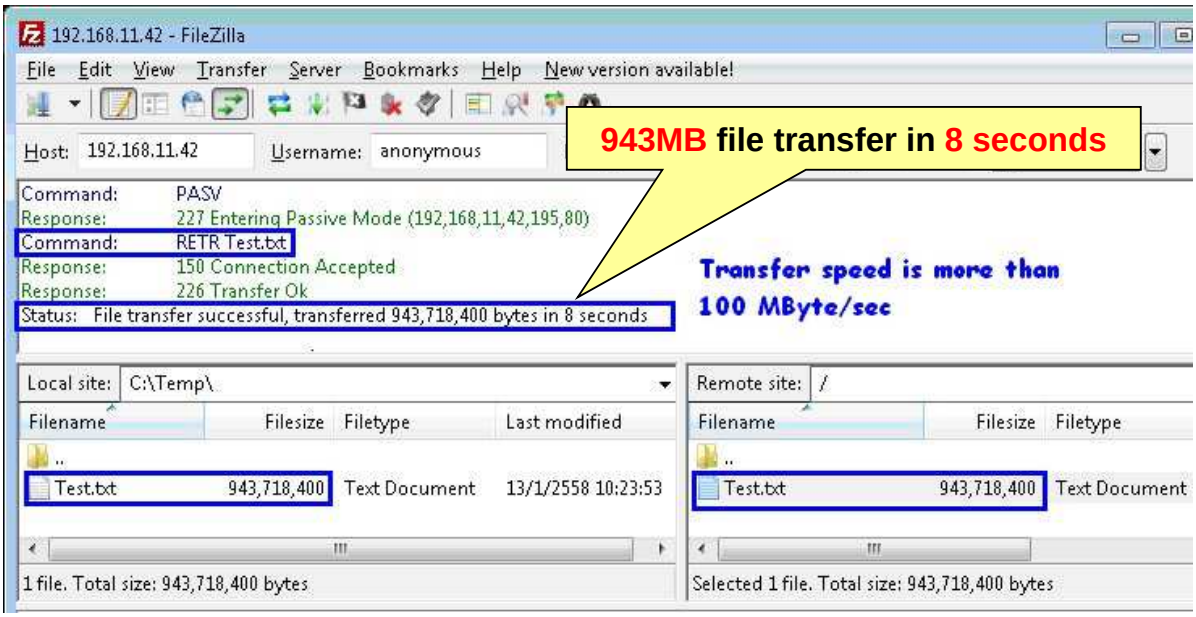
- FPGA board operates as high-speed FTP server
- TOE1G-IP core executes ultra high-speed file data transfer
- CPU (NiosII) handles FTP command process by its firmware



FTP sample system

Reference Design (FTP sample: cont'd)

- **Extreme transfer speed over 100MB/s**



Real performance result of 943MByte file download by FileZilla

Effective Development on Ref. Design

- **QuartusII project file in TOE1G-IP package**
- **Full source code (VHDL) except IP core**
- **Can save user system development duration**
  - **Confirm real board operation by original reference design.**
  - **Then modify a little to approach final user product.**
  - **Check real operation in each modification step.**

Short-term development is possible without big turn back

Resource Usage

- **TOE1G-IP core standalone resource usage**
  - **Condition = Maximum buffer setting**
    (TxDataBuf=RxDataBuf=64KB, TxPacketBuf=16KB)

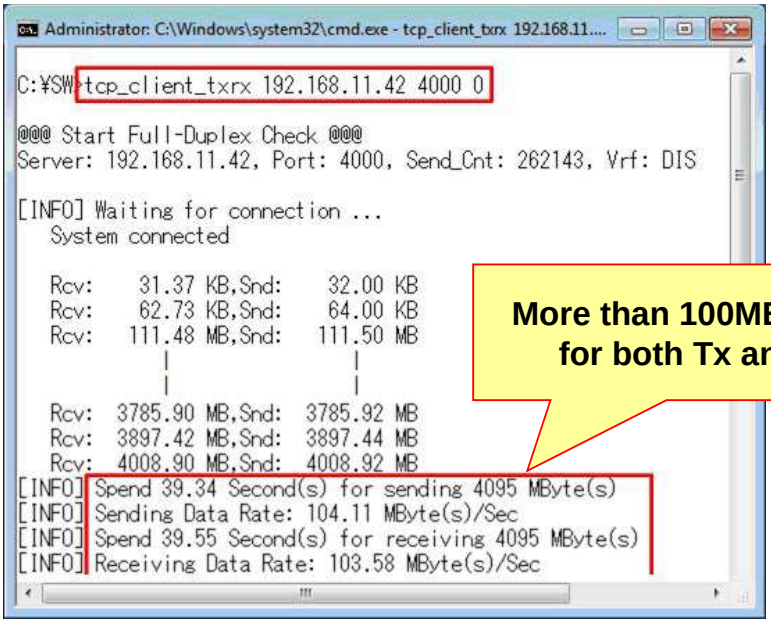
Family	Example Device	Combinatorial ALUTs	Registers	Pin	Block Memory bit	Design Tools
Stratix IV GX	EP4SGX230KF40C2	2,226	2,778	137	1,181,696	QuartusII 14.0
CycloneV E	5CEFA7F31I7	2,052	3,084	137	1,181,696	QuartusII 15.1
ArriaV GX	5AGXFB3H4F35C5	2,064	3,002	137	1,181,696	QuartusII 14.0
Arria10 SX	10AS066N3F40E2SGE2	2,028	3,050	137	1,181,696	QuartusII 16.0

TOE1G-IP core standalone compilation result

This result is based on maximum buffer size setting.
User can save memory resource by smaller buffer size setting

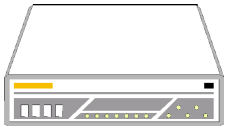
Transfer Performance

- **Real performance in full-duplex test**



TOE1G-IP Application Market

- **Data transfer in FA market**
  - **Medical video processing system**
  - **Sensor data logger measurement instrument**
- **Storage system using TCP such as NAS, iSCSI**
  - **TOE1G-IP replaces CPU for hard TCP processing**
- **Network product**
  - **Network printer for high speed print data download**
  - **Network camera for high speed video data upload**


For more detail

- **Detailed documents available on the web site.**
- **http://www.dgway.com/TOE1G-IP_A_E.html**
- **Contact**
  - **Design Gateway Co,. Ltd.**
  - **E-mail :**
    ip-sales@design-gateway.com
  - **FAX : +66-2-261-2290**


Revision History

Rev.	Date	Description
1.0E	April 5, 2016	English version initial release
1.1E	August 30,2016	Added Arria10SoC support
1.4E	October 20,2016	Addes CycloneV support