# USB3DevIP Data Recorder by FAT32 Demo Instruction

Rev1.0 13-Mar-15

This instruction document describes how to run FAT32 data recorder by using USB3-DevIP in step by step. Data stream input is sent from hardware system at 256 MB/s through USB3 interface, so Test PC should be high-performance and not run other application during the test.

## 1 Environment Setup

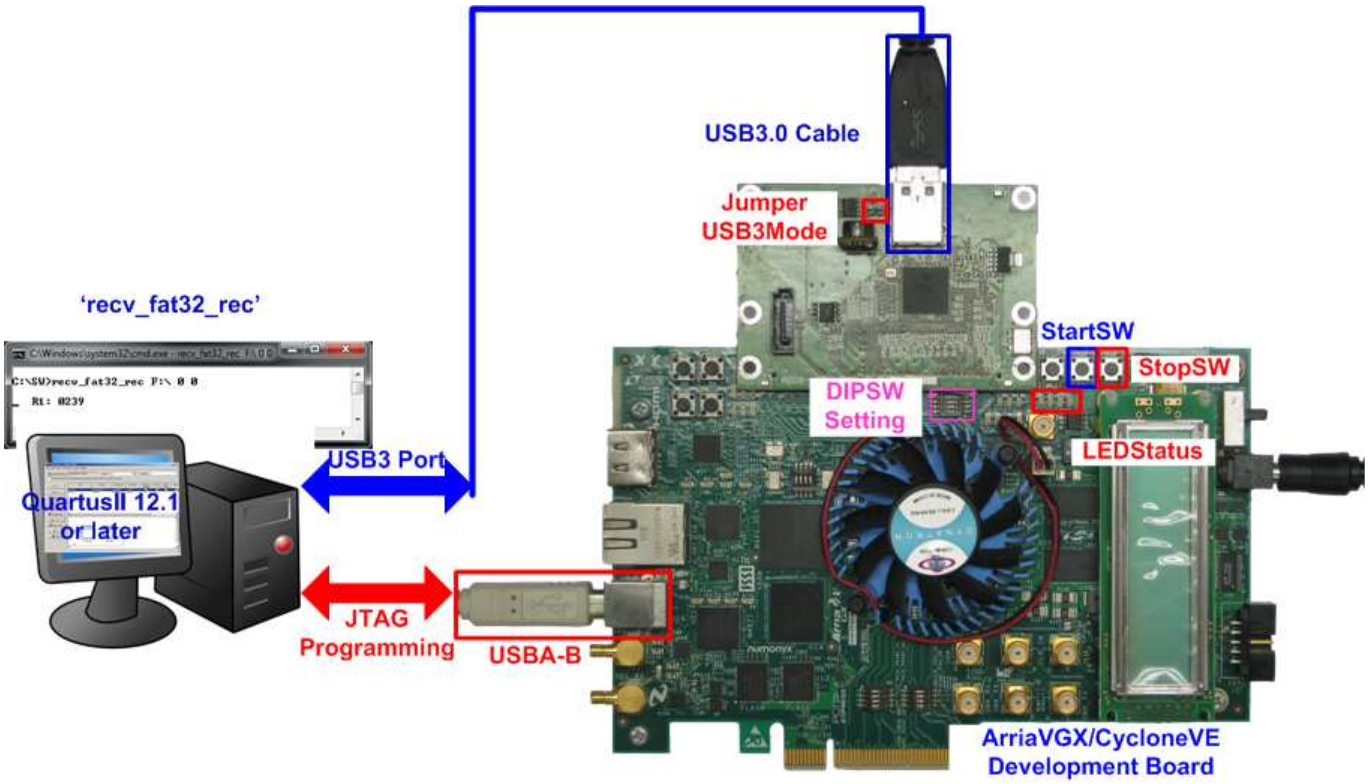


Figure 1 FAT32 Data Recorder Hardware Setup on ArriaVGX board

To run the demo, please prepare test environment as follows.

1) FPGA development board (ArriaVGX/CycloneVE development board)
2) Quartus Programmer ver 12.1 or later to program FPGA board
3) NiosII command shell ver 12.1 or later to monitor board status through JTAG-UART
4) PC with built-in USB3 which has performance more than 256 MB/s
   *Note: Please run USB3-IP device demo with the benchmark to check read performance firstly. More than 256 MB/sec must be achieved.*
5) AB08-USB3HSMC adapter board, provided by Design Gateway
6) USB3 A-A cable to connect between USB3 adapter board and PC
7) USB A-B cable to connect between FPGA board and PC for programming and UART
8) "recv_fat32_rec.exe" test application on PC, provided by Design Gateway
9) 64-bit Windows7 OS installation on PC to run test application

## 2 How to run the demo

- Check that FPGA board is powered off.
- Connect USB A-B cable from USB connector on FPGA board (J10 on CycloneV board/J14 on ArriaV GX board) to USB on PC for JTAG programming and JTAG-UART operation.
- Connect adapter board to HSMC connector on FPGA board.
- Confirm that JP1 on the adapter board is not jumped (OFF).
- Connect USB3.0 A-A cable between USB on adapter board and USB3 port on PC.
- Power on FPGA board.
- Open QuartusII programmer and download SOF file to FPGA board.

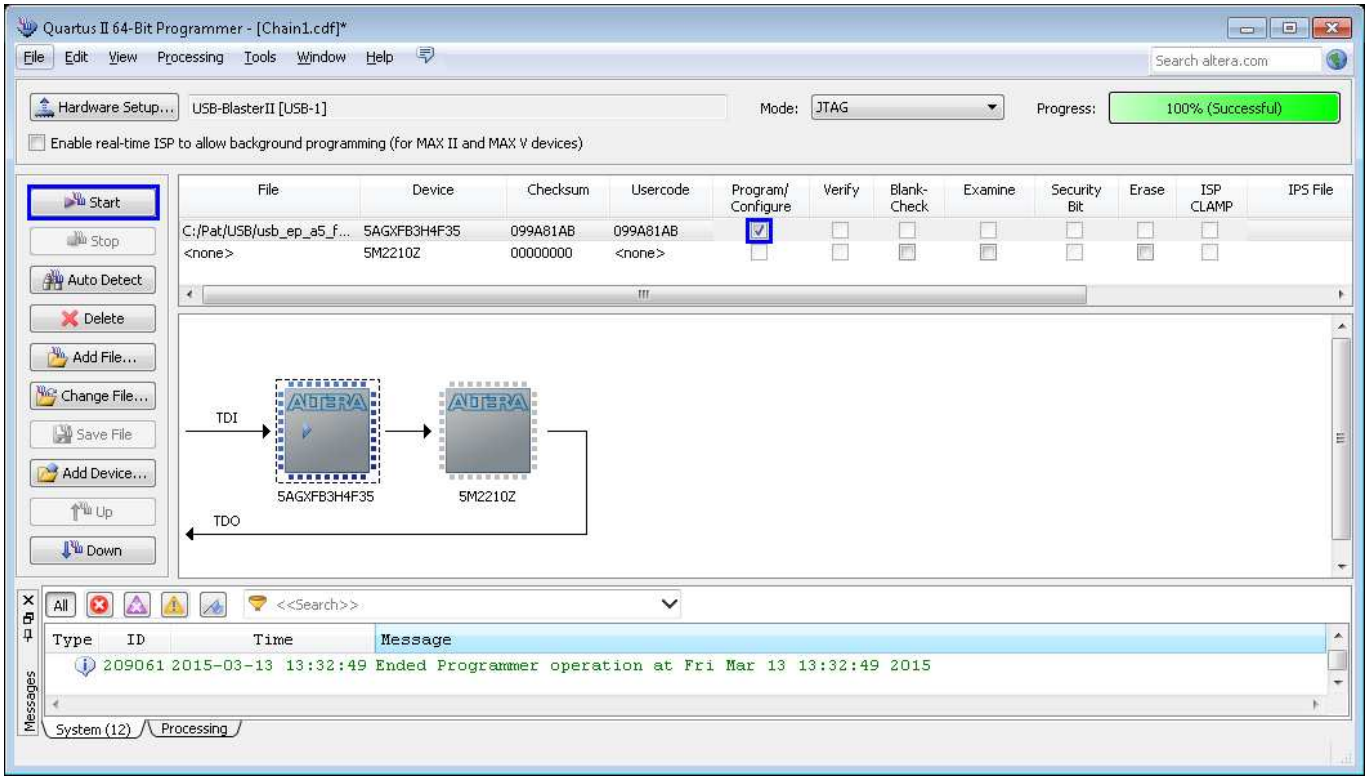


Figure 2 Download SOF File by QuartusII Programmer

- Open NiosII command shell, and type “nios2-terminal”. Then, USB3-IP debug message will be displayed on the console, as shown in Figure 3. New drive named “DGDrive” will be appeared on TestPC, as shown in Figure 4.
  *Note: If SCSI command message is not appeared or drive is not detected on PC, please check USB3 connection between the adapter board and PC.*

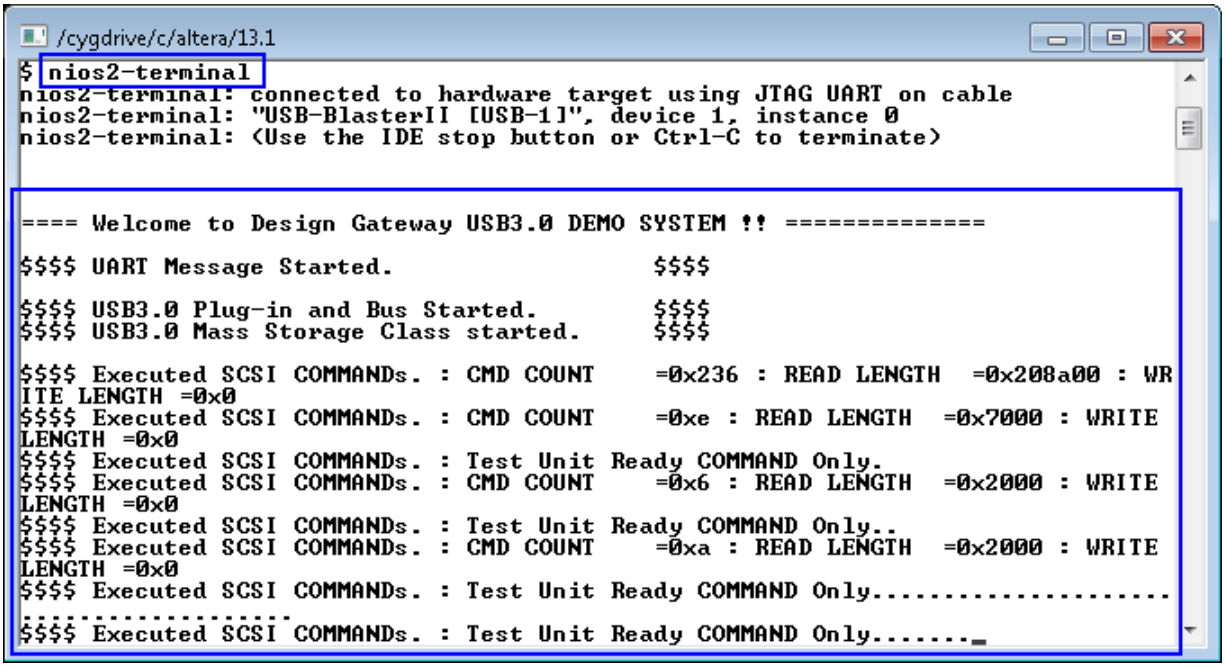


Figure 3 Open NiosII terminal and bootup message

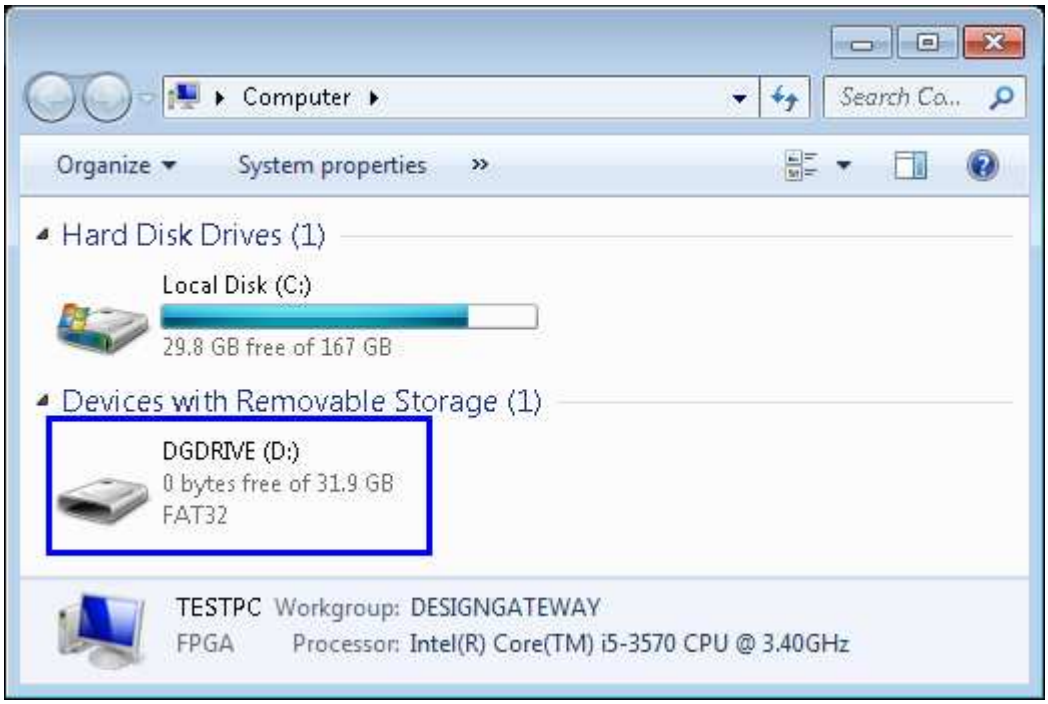


Figure 4 DG Drive Detect on TestPC

- LED[0]-[3] for release version will be OFF/ON/OFF/ON in a sequence, as shown in Figure 5. All LEDs will be ON if hardware is overflowed (PC cannot read data in time).

Figure 5 Default LED[0]-[3] after configuration complete

- Set DIPSW[0] on FPGA board to select test pattern.
  ON: 32-bit increment pattern, OFF: 32-bit decrement pattern
- Run “recv_fat32_rec.exe” application on TestPC by typing command
  >> recv_fat32_rec [DG Drive Letter] [mode] [pattern]
  mode: ‘0’-No data verification, ‘1’-Enable data verification
  pattern: ‘0’-32-bit increment pattern, ‘1’-32-bit decrement pattern
  *Note: Data verification requires much resource on PC. To run this mode, please use high-performance PC and not run other application during the test. Also, pattern selection must be matched with DIPSW[0] setting on FPGA board.*


Figure 6 Run "recv_fat32_rec" application

- After running “recv_fat32_rec”, “R0: 0000” message will be displayed on command prompt.
  R0: 0 means the loop number starting from 0. The loop number will be increment when end of reading F0944.BIN file and next file is F0000.BIN.
  0000: 4-DIGIT number is referred to the read file number. 0000 means F0000.BIN.
- Press “PB SW1” to start data recording. Then, file number will be increased and updated on the console every second, as shown in Figure 8.


Figure 7 USER PB[1]-[2] to start/stop data recording


Figure 8 Update File number during data recording

- User can stop data recording by press “PB SW2”. “Cancel operation” message will be displayed on the console.


Figure 9 Message when operation stopped

- “Hardware Overflow” will be displayed on NiosII terminal if overflow is detected. Also, LED[0]-[3] on FPGA board will be all ONs, as shown in Figure 10 - Figure 11.

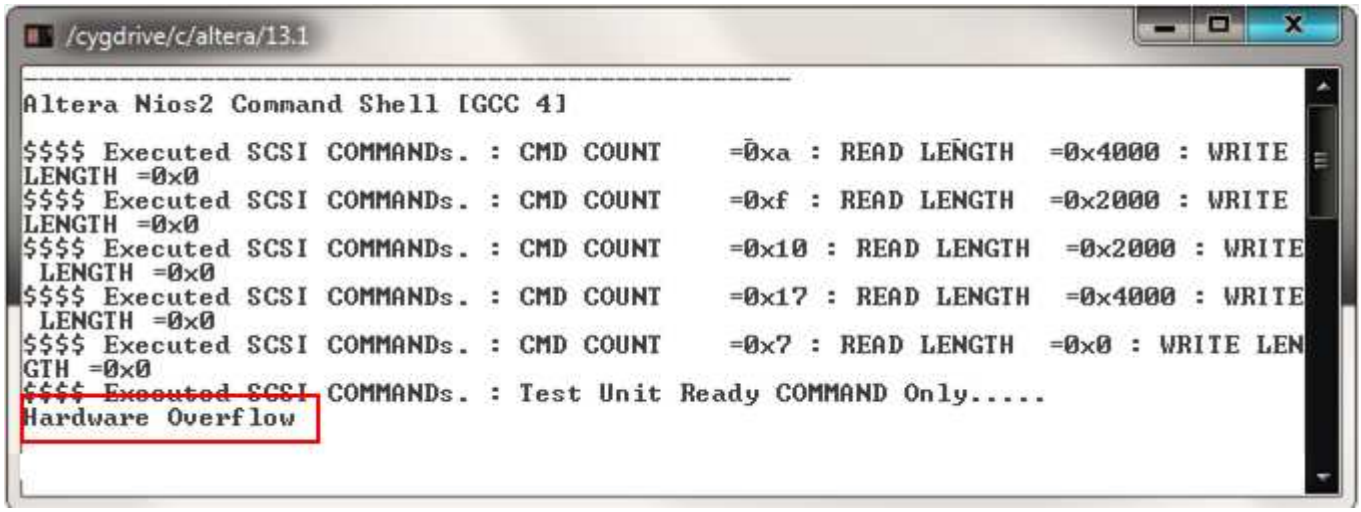


Figure 10 Overflow message on NiosII terminal

Figure 11 LED Status after hardware overflow

- If data verification within test application finds error data, error message will be displayed on the console, as shown in Figure 12. Test application will be cancelled and hardware will be stopped by overflow.

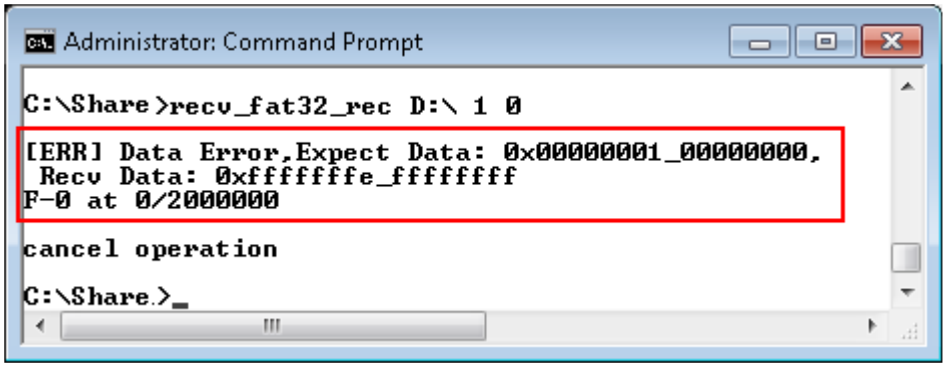


Figure 12 Error message when data verification failed

# 3 Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 13-Mar-15 | Initial version release |