

## JtagLink Data Sheet

Ver1.3 Oct/22/2003

- Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	-0.5	+4.6	V
Tstg	Storage temperature	-55	+125	Celsius
Topr	Operating temperature	-20	+85	Celsius
Vin	DC input voltage	-2.0	+5.75	V

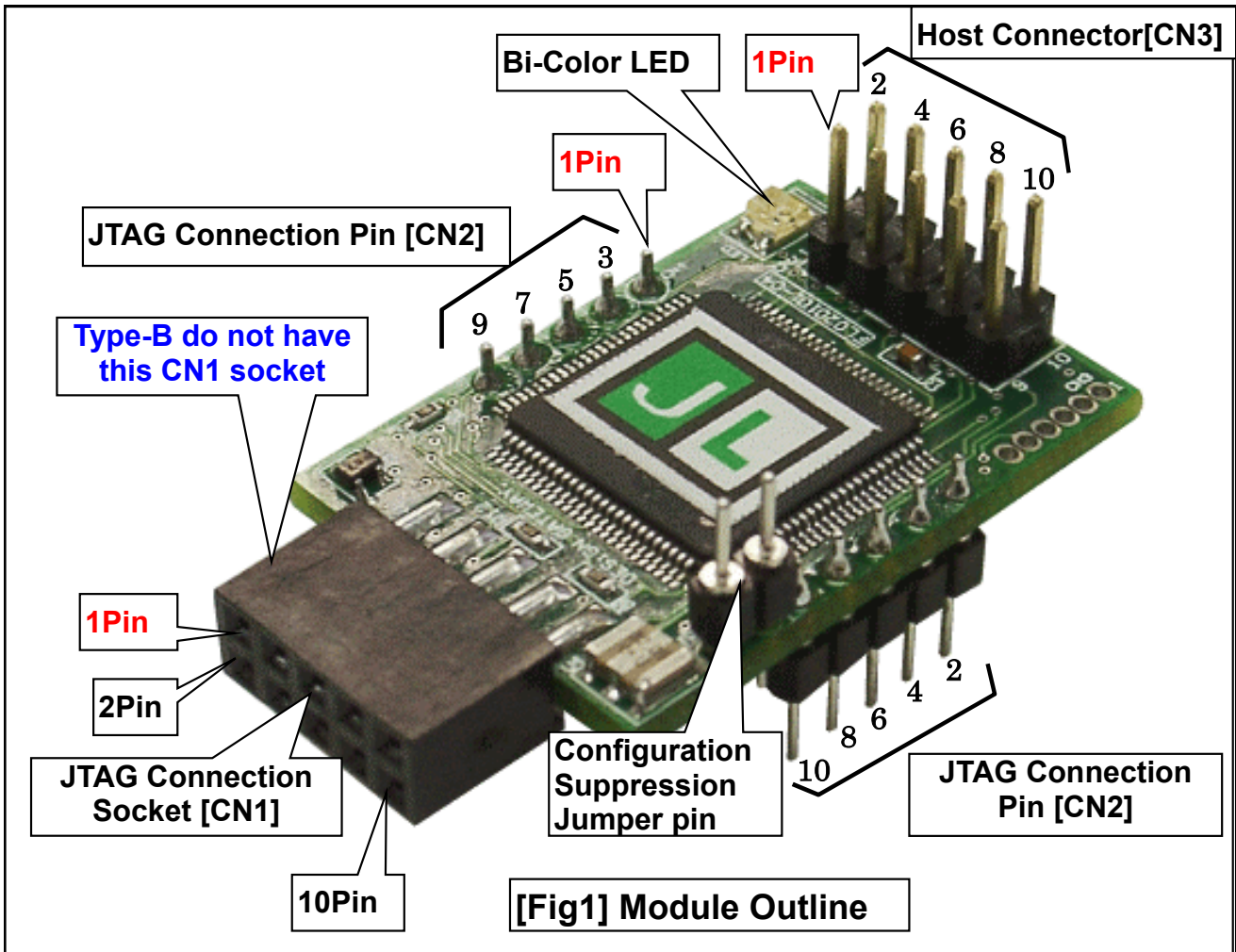
[Table1] Absolute Maximum Ratings

- Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	+3.0	+3.6	V
Topr	Operating temperature	0	+70	Celsius
Vih	High level input voltage	+1.7	+5.25	V
Vil	Low level input voltage	-0.5	+0.8	V
Voh	High level output voltage	+2.4	Vcc	V
Vol	Low level output voltage	0	+0.7	V

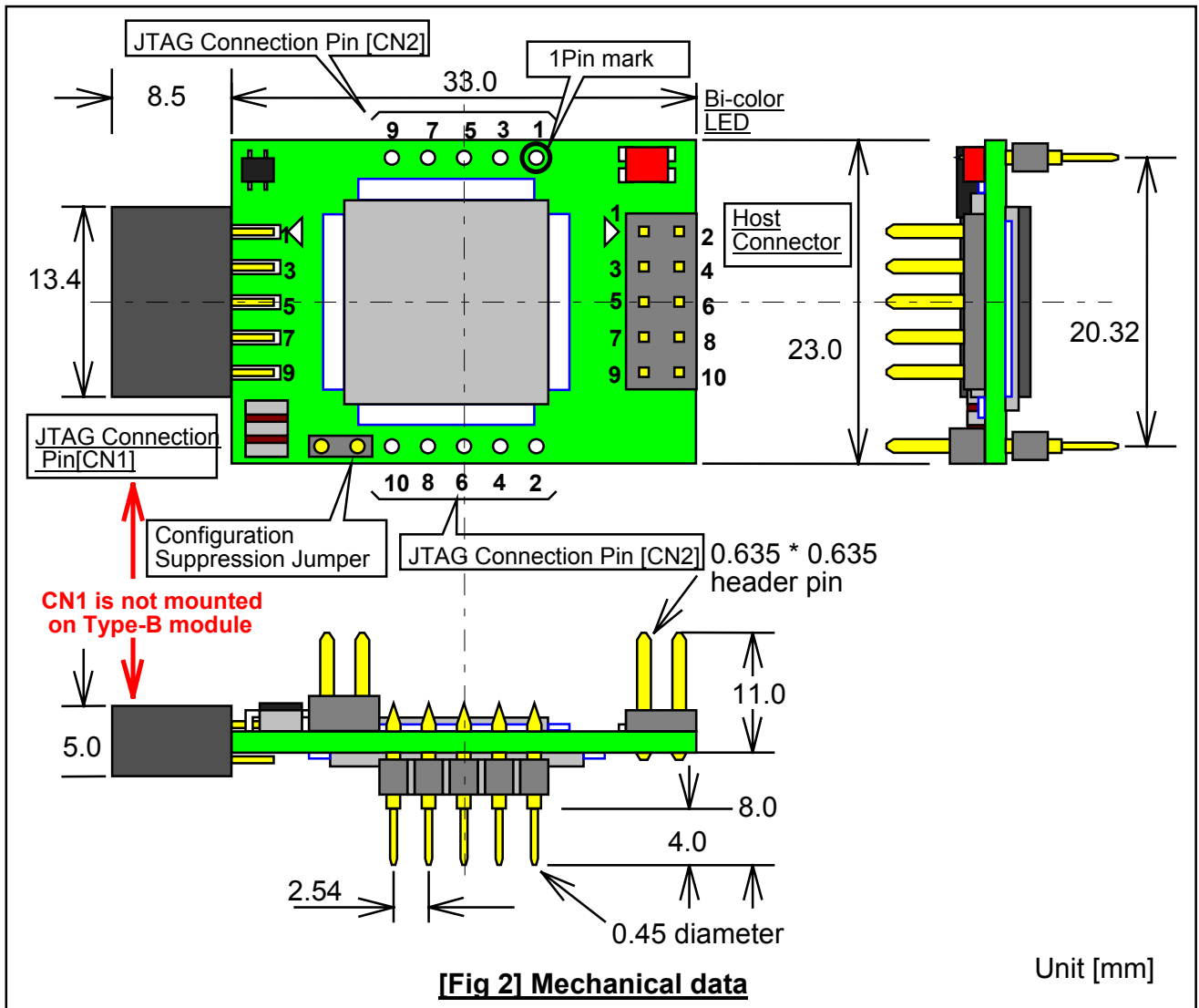
[Table2] Recommended Operating Conditions

- Module Outline



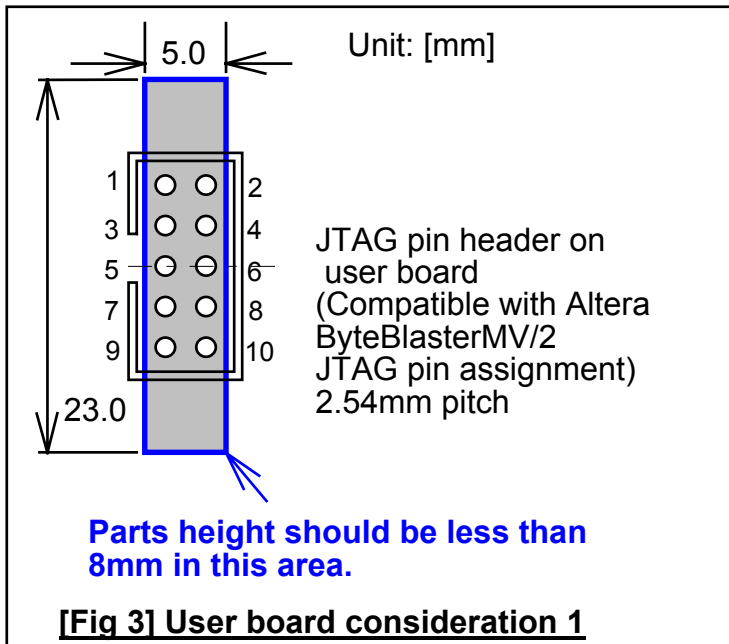
- Figure-1 shows Type-A module outline. For Type-B, module appearance is identical to Type-A except CN1 that is not mounted on Type-B module.
- Host Connector[CN3] connect with ByteBlasterMV/2 for Altera or ParallelCable3/4 for Xilinx.
- Connect with JTAG on a user board using JTAG Connection Socket[CN1] or JTAG Connection Pin[CN2]. Same signal is assigned to the same pin numbers by CN1 and CN2.
- JTAG Connection Socket[CN1] is based on standard JTAG pin assignment of ByteBlasterMV/2 for Altera.
- JTAG Connection Pin[CN2] is used in case where it connects directly with user board through 2.54mm pitch DIP socket.
- [Bi-Color LED] displays configuration status or host communication status.

● Mechanical Data

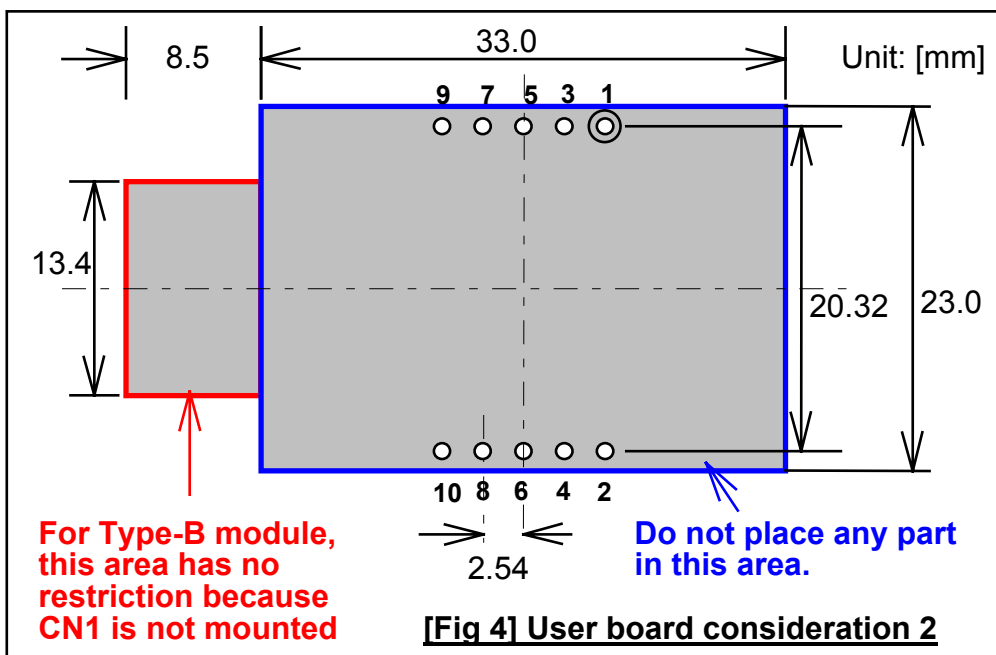


- ByteBlasterMV/2 from Altera or ParallelCable3/4 from Xilinx should be connected to [CN3] of the Host Connector.
- [CN1] of the JTAG Connector is not mounted on Type-B module.

- Note of user board 1: In case of connecting JTAG connection socket [CN1] and user board.



- Note of user board 2: In case of connecting JTAG connection pin [CN2] and user board.



- Signal pin assignment of JTAG connection socket [CN1] or pin [CN2].

CN1	CN2	Signal	I/O	Logic	Description
1	1	TCK	OUT	Positive	TCK signal which JtagLink supplies to the JTAG chain all device on the user board. TCK pattern on the user board is drawn one way for measure against reflective noise, and set terminal resistor. (*1)
2	2	GND	Power		Signal Ground.
3	3	TDO	IN	Positive	TDO signal which is inputted to JtagLink from the end of device of JTAG chain on the user board. This signal from the user board is 3.3V-LVTTL level signal. And It has 10Kohm internal pull-up on JtagLink.
4	4	+3.3V	Power		Power Supply. Supply +3.3V (+10% / -10%)
5	5	TMS	OUT	Positive	TMS signal which JtagLink supplies to the JTAG chain all device on the user board. TMS pattern on the user board is drawn one way for measure against reflective noise, and set terminal resistor. (*1)
6	6	(N.C)			(No Connect)
7	7	nWAIT	IN	Negative	Configuration Initialize wait signal. This wait signal waits to execute configuration when ConfigurationRom mounted on the user board and effective circuit data will be executed automatic configuration at power on. And It has 10Kohm internal pull-up on JtagLink. When these is no ConfigurationRom on the user board, set NoConnect (*2).
8	8	(N.C)			(No Connect)
9	9	TDI	OUT	Positive	TDI signal which JtagLink outputs to head device of JTAG chain on the user board. It outputs 3.3V-LVTTL level signal.
10	10	GND	Power		Signal Ground.

[Table 3] Signal Description of JTAG socket [CN1] / pin [CN2]

Note:

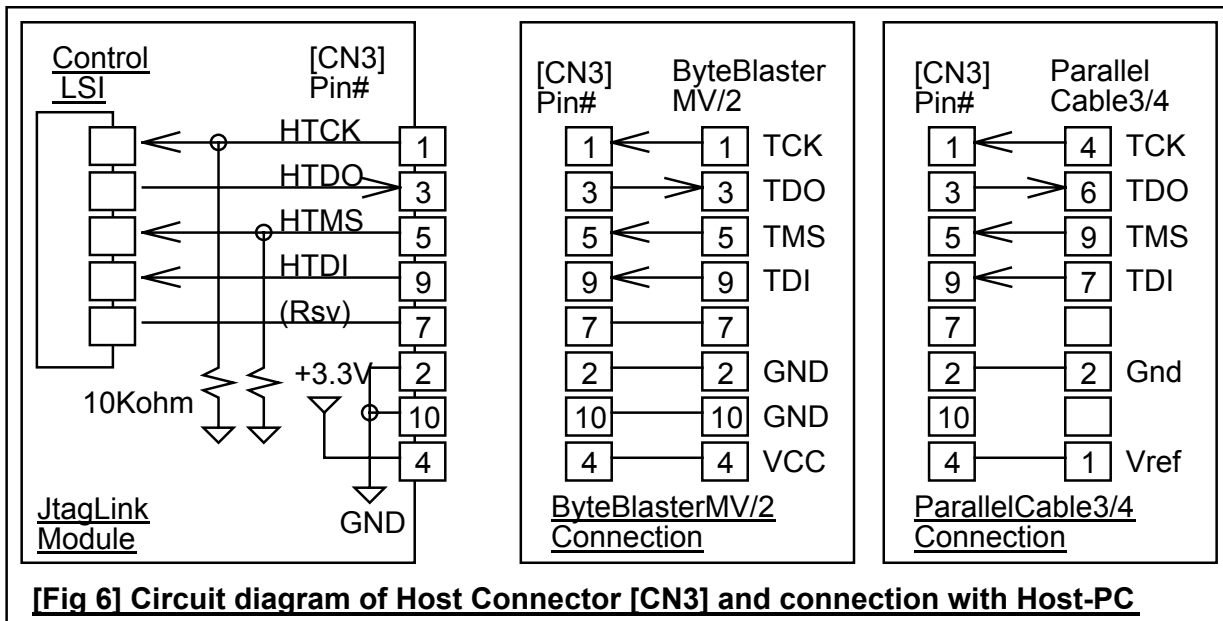
(\*1) When TCK pattern on the user board is not one way and unsuitable pattern with stub (branch), glitch noise may overlap by reflecting TCK signal. In this case JTAG configuration may be unsuccessful. And it is necessary to keep up signal quality according to TCK signal because TMS signal is also connected all device and wiring length is extended. In order to prevent this, **TCK/TMS are drawn one way pattern. And Set about 1Kohm Pull-Up or Pull-Down terminal resistor.**

(\*2) When ConfigurationROM (Altera EPC16 or Xilinx XC18V04 etc.) that is mounted on the user board, execute automatic configuration to FPGA at power on, it is necessary to avoid competition of configuration by ROM on the user board, and configuration by JtagLink. In this case JtagLink execute JTAG configuration like a overwriting circuit after ROM on the user board makes configuration complete by connecting (CONF)DONE pin to nWAIT input of JtagLink.

(\*3) CN1 exists only on Type-A module. (CN1 is not mounted on Type-B module.)



● Circuit Diagram of Host connector



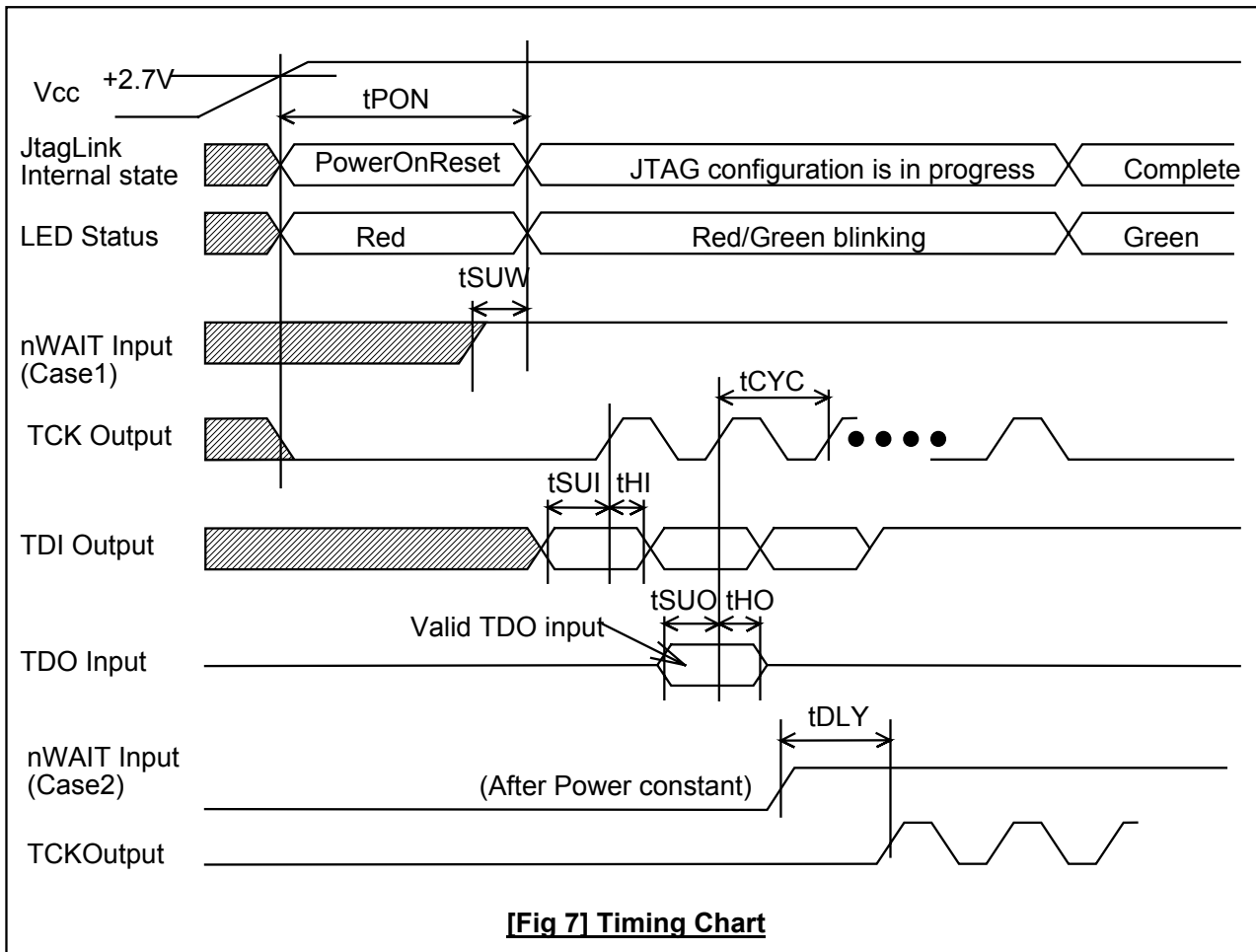
Each signal line of host connector is named similar to JTAG signal ('H' which means host connector is put on head of signal name). When iMPACT on the HostPC or Programmer of Quartus2 execute FPGA configuration on the user board directly bypass JtagLink (Bypass function running), access from HostPC by the protocol based on JTAG signal specification. Another side when JtagLink software on the HostPC access to Flash memory on JtagLink, Communicate by original protocol which is not based on JTAG signal specification.

● Signal Description of Host Connector

CN3	Signal	I/O	Description
1	HTCK	IN	Communication signal from Host-PC to JtagLink. Connect 1pin of ByteBlasterMV/2 or 4pin of ParallelCable3/4 (TCK). This signal is internally pulled-down with 10Kohm.
2	GND	Power	Signal Ground Connect 2pin of ByteBlasterMV/2 or 2pin of ParallelCable3/4.
3	HTDO	OUT	Communication signal from JtagLink to Host-PC. Connect 3pin of ByteBlasterMV/2 or 6pin of ParallelCable3/4 (TDO).
4	+3.3V	Power	Power Supply. Connect 4pin of ByteBlasterMV/2 or 1pin of ParallelCable3/4 (Vref).
5	HTMS	IN	Communication signal from Host-PC to JtagLink. Connect 5pin of ByteBlasterMV/2 or 9pin of ParallelCable3/4 (TMS). This signal is internally pulled-down with 10Kohm.
6	(N.C)		(No Connect)
7	(Rsv)	OUT	Reserved signal. This signal is not used for communication.
8	(N.C)		(No Connect)
9	TDI	IN	Communication signal from Host-PC to JtagLink. Connect 9pin of ByteBlasterMV/2 or 7pin of ParallelCable3/4 (TDI).
10	GND	Power	Signal Ground. Connect 2pin of ByteBlasterMV/2.

[Table 4] Signal Description of Host connector [CN3]

● Timing Chart



Symbol	Description	Min	Typ	Max	Unit
tPON	PowerOn reset time from Power-On (over +2.7V) to JTAG configuration start	240	400	600	ms
tSUW	nWAIT input required setup time before PowerOn reset release	188			ns
tSUI	Guarantee setup time of TDI output to TCK (standup) edge	56	62.5		ns
tHI	Guarantee hold time of TDI output to TCK (standup) edge	56	62.5		ns
tCYC	Cycle time of TCK		125		ns
tSUO	Required setup time of TDO input to TCK (standup) edge	12.5			ns
tHO	Required hold time of TDO input to TCK (standup) edge	12.5			ns
tDLY	nWAIT release to 1 <sup>st</sup> TCK pulse after power constant		920		ns

[Table 5] Timing Characteristics

(Note: Timing Characteristics are tentative and might be changed without notice.)