PCB design guide for alternative configuration by ROM or SDLink

Ver1.0E 1 November 2018

This document describes design guide for PCB that mounts both Configuration ROM and SDLink for alternative configuration. This design can apply to such case that user executes FPGA configuration by SDLink during prototype stage, then switch to Configuration ROM after design verification is completed. By using analog switch device, user can design flexible PCB with alternative configuration regardless of signal direction and configuration voltage.

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When FPGA configuration method is selectable between SDLink and ROM, FPGA configuration clock (CCLK/DCLK) is input direction for FPGA in SDLink case, but clock direction is reversed to output in ROM case. In such case of signal direction reverse, analog switch device usage is the most suitable. This document introduces example of signal direction reverse application by analog switch device. TS3A5018 from Texas Instruments is used for this example

About Analog switch device

- Following is description of TS3A5018.
- This analog switch has 2-to-1 SPDT function, and COM port connection can be alternatively selected between NC port and NO port by H/L level of IN port.
- Power supply voltage range is 1.8V – 3.6V.
- Very low impedance (around 10 ohm) between connected two ports.
- Not selected port is in high impedance state and isolated from another port.
- Selectable of connection or disconnection regardless of signal direction.
- TS3A5018 includes 4 channels of 2-to-1 SPDT switch function.
- User can select each port signal voltage level from 1.8V, 2.5V, or 3.3V.
- Following figure1 shows block diagram of TS3A5018 and function.

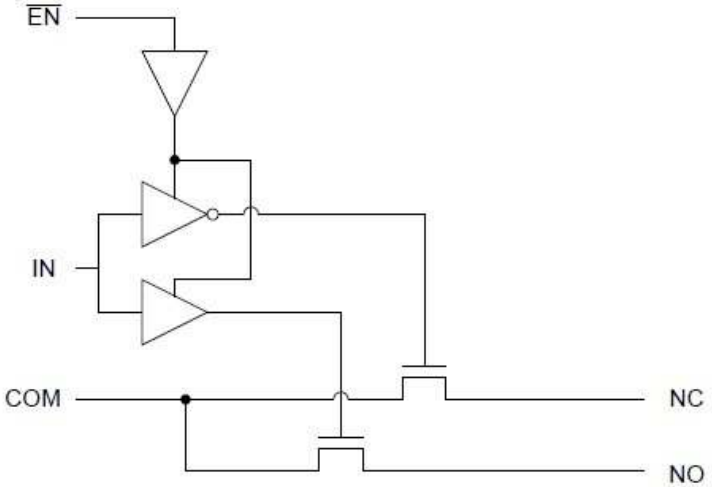

Table 1. Function Table

$\overline{EN}$	IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
L	L	OFF	ON
L	H	ON	OFF
H	X	OFF	OFF

Figure 1: TS3A5018 block diagram and function table

TS3A5018 URL: http://www.ti.com/product/TS3A5018/

Basic Connection

- Basic connection of each configuration signal is shown figure2 below.
- Use IN port to select between ROM (IN=Low) or SDLink (IN=High).
- Connect configuration signal of FPGA to COM port.
- Connect configuration signal of ROM to NC (selected when IN=Low) port
- Connect configuration signal of SDLink to NO (selected when IN=High) port
- Set EN=Low to force always enabled.

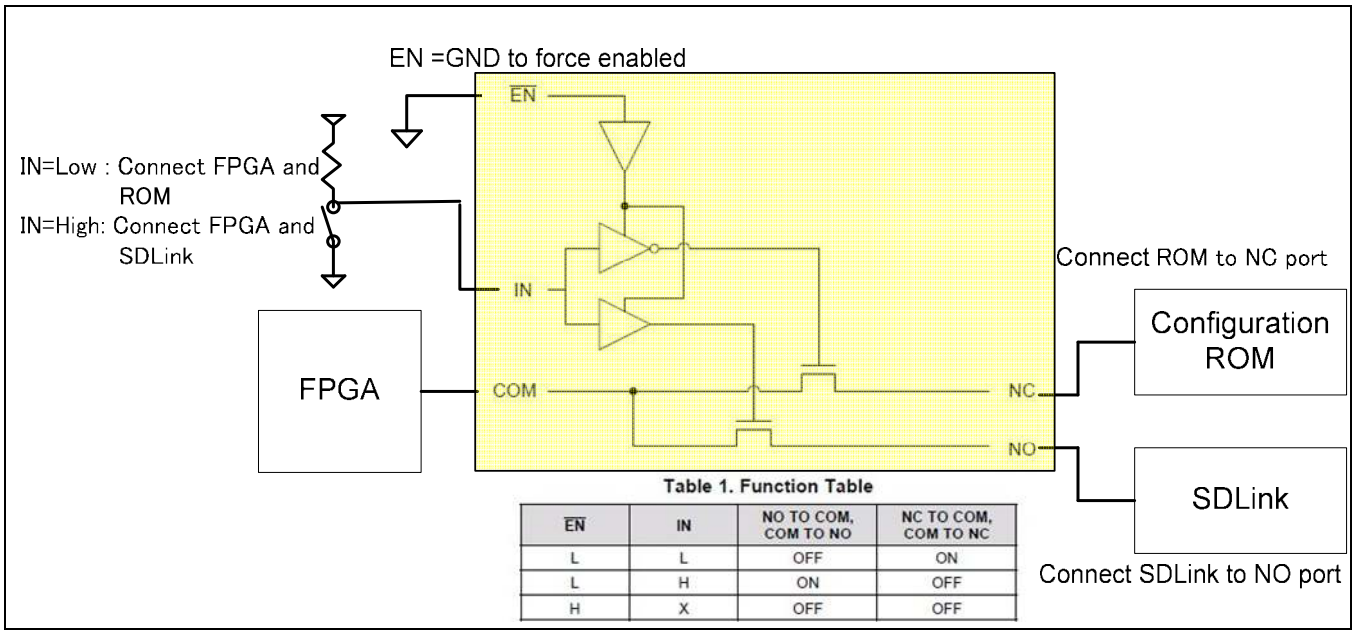

Table 1. Function Table

$\overline{EN}$	IN	NO TO COM, COM TO NO	NC TO COM, COM TO NC
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Figure2: Basic connection using TS3A5018

Consideration for Configuration Clock

- Configuration clock (CCLK/DCLK) direction is different between SDLink and ROM.
- Basically, ROM should be located adjacent to FPGA to reduce signal trace length as short as possible.
- Also, minimize trace length between analog switch and FPGA for clock signal.
- In some case, SDLink position is away from FPGA.
- When SDLink is away from FPGA, it's possible that clock signal quality from SDLink is degraded.
- In such case, place Thevenin termination resistor network adjacent to NO port.
- Pattern trace between this Thevenin termination and analog switch will be the stub, but it can keep clock signal quality by minimizing stub trace length.
- Figure3 below shows clock signal connection diagram.

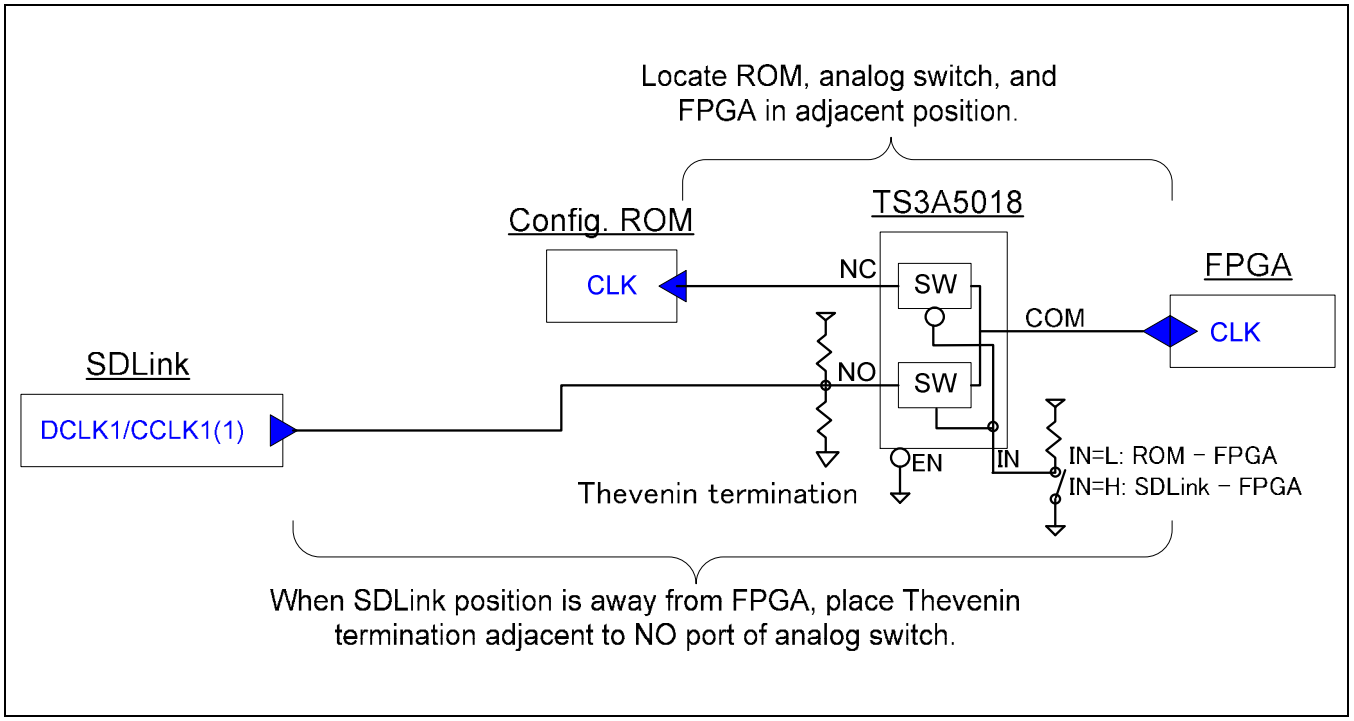

Figure3: Configuration clock using TS3A5018

nCONFIG/nPROG signal connection

- Though there is no configuration start signal (nCONFIG/nPROG) in ROM and this signal connection target is SDLink only, this signal cannot directly connect between FPGA and SDLink.
- This is because even if ROM is selected, SDLink will assert this signal to FPGA.
- So it needs to connect this signal with FPGA only when SDLink is selected.
- Following figure 4 shows configuration start signal connection using TS3A5018.
- If configuration start signal is connected to FPGA only when SDLink is selected, it's also OK not use analog switch but use another device.

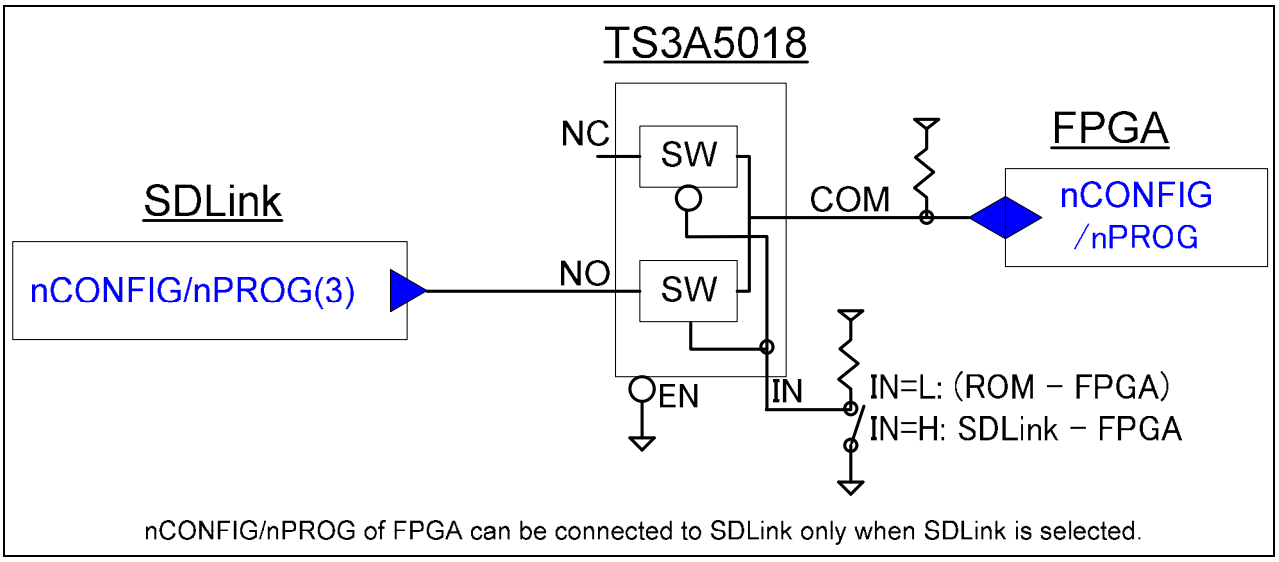

Figure 4: nCONFIG/nPROG signal connection using TS3A5018

CONF_DONE/DONE and nSTATUS/nINIT signal connection

- Configuration completion signal (CONF_DONE/DONE) and configuration error signal (nSTATUS/nINIT) are not connected to ROM but only connected to FPGA.
- Both these two signals are output from FPGA and input to SDLink so SDLink does not drive them, so that it can directly connect between FPGA and SDLink.
- Signal switch circuit by analog switch or other device is not necessary.

Other configuration signals for ROM only

- For each FPGA configuration signals that connection target is only ROM, it can directly connect between ROM and SDLink directly.

Revision History

Rev.	Date	Description
1.EJ	1st-Nov-2018	English version initial release