XXVGMACRSFEC-IP Demo Instruction

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1 Overview

This document provides the instructions for preparing the test environment and setting up the loopback demo using the XXVGMACRSFEC-IP on an FPGA development board. The purpose of the demo is to measure the round-trip latency time of the XXVGMACRSFEC-IP using an SFP28 loopback module. Additionally, the demo offers a menu to check the signal quality transferring from Tx interface to Rx interface via the loopback module, which is presented as an error count that is monitored by the received RS-FEC module inside the IP.

The following section presents the hardware and software lists used in the loopback demo test. The process for setting up the hardware and software is explained as step-by-step in section 3. Finally, section 4 provides an example of the test results for each test menu and explains the results in detail. For further information of each topic, please refer to the respective sections.

2 List of Test environment

To run the loopback demo of the XXVGMACRSFEC-IP, the following test environment must be prepared.

- FPGA development board: KCU116
- (Optional for external loopback mode) SFP28 Loopback connector
- Two micro USB cables for FPGA programming and Serial console monitoring on PC
- Serial console software such as TeraTerm installed on PC. The console settings should be Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1-bit.
- Vivado tool installed on PC for programming the FPGA

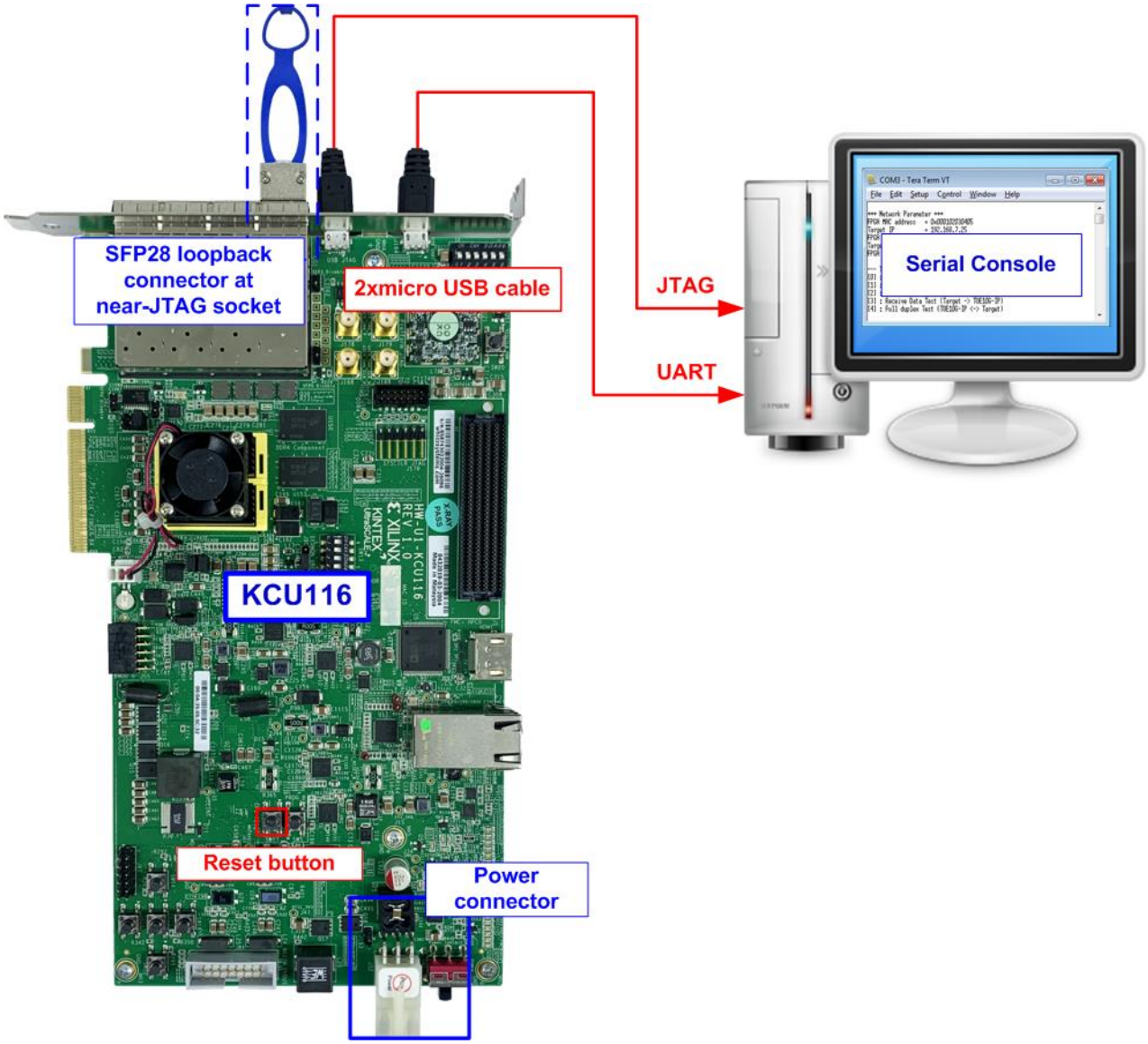

Figure 2-1 XXVGMACRSFEC-IP loopback demo on KCU116

3 Test environment setup

To se up the test environment, follow the steps below.

1) Connect two micro USB cables between the FPGA and PC for JTAG programming and Serial console through USB UART.
2) Connect the Xilinx power adapter 60W (12V) to the FPGA development board.
3) (Optional for external loopback mode) Connect the SFP28 loopback connector at the near-JTAG socket, as shown in Figure 3-1.

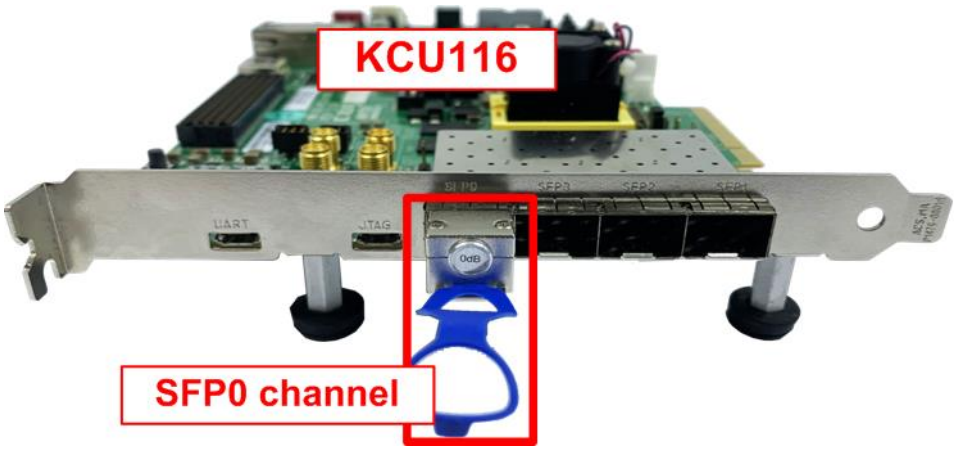

Figure 3-1 SFP28 loopback connector on KCU116 board

4) Open the Serial console. When connecting the FPGA board to the PC, several COM ports from the FPGA connection are detected and displayed on the Device Manager.

   For KCU116, select the standard COM port as the Serial console.

   On the Serial console, use the following setting: Buad rate=115,200, Data=8-bit, Non-Parity, and Stop=1.

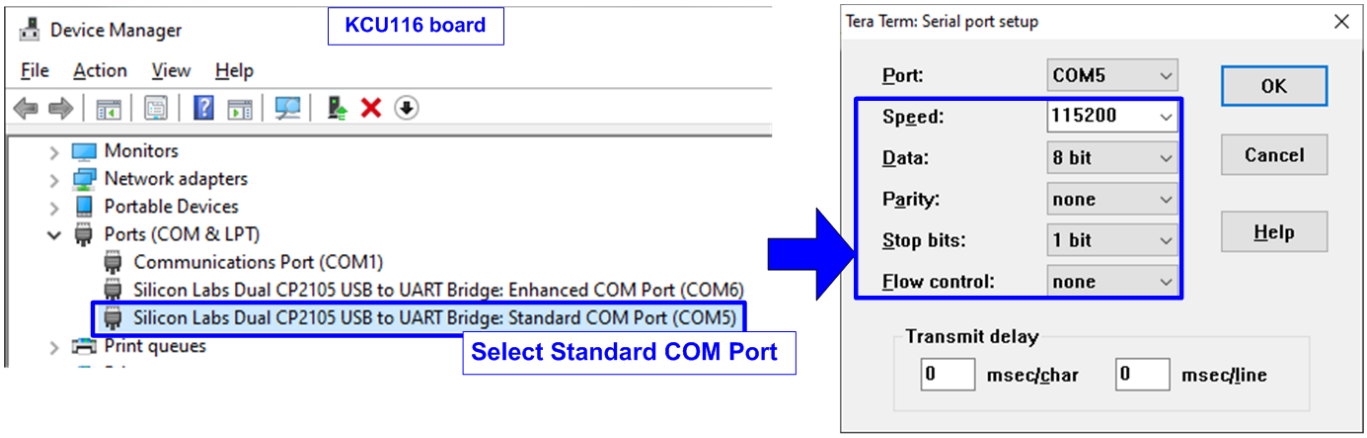

Figure 3-2 COM port selection for Serial console

5) For KCU116, set programmable clock to 322.265625 MHz using “KCU116 – Board User Interface” application as shown in Figure 3-3.

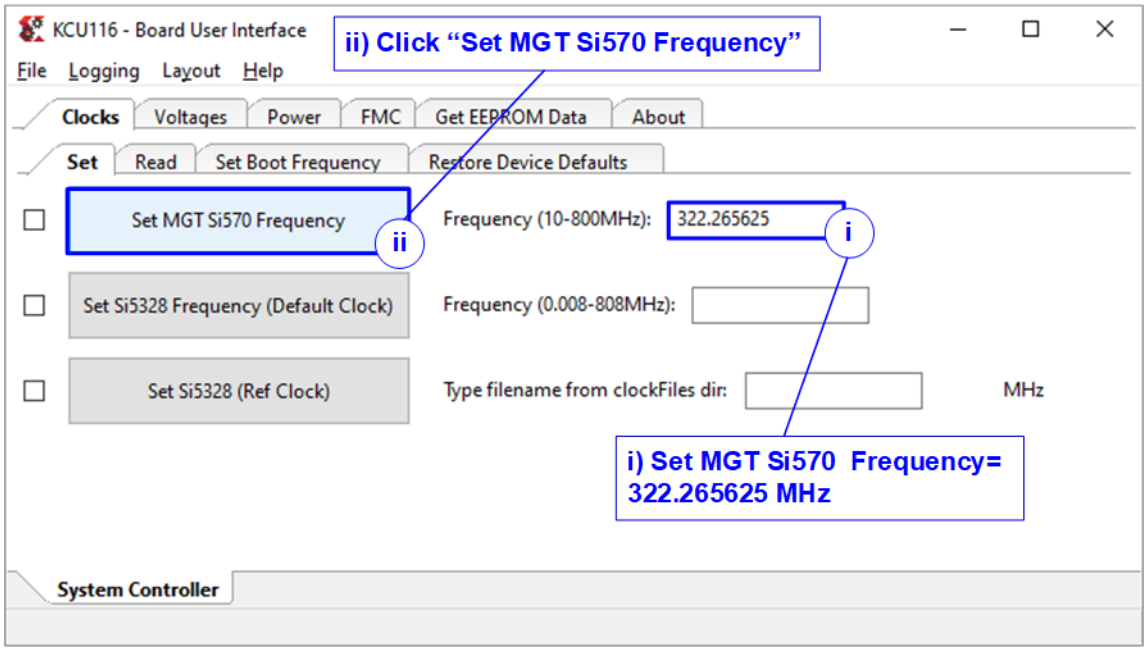

Figure 3-3 Reference clock programming for KCU116

6) Download the configuration file and firmware to the FPGA board using the Vivado tool to program configuration file (bit file), as shown in Figure 3-4.

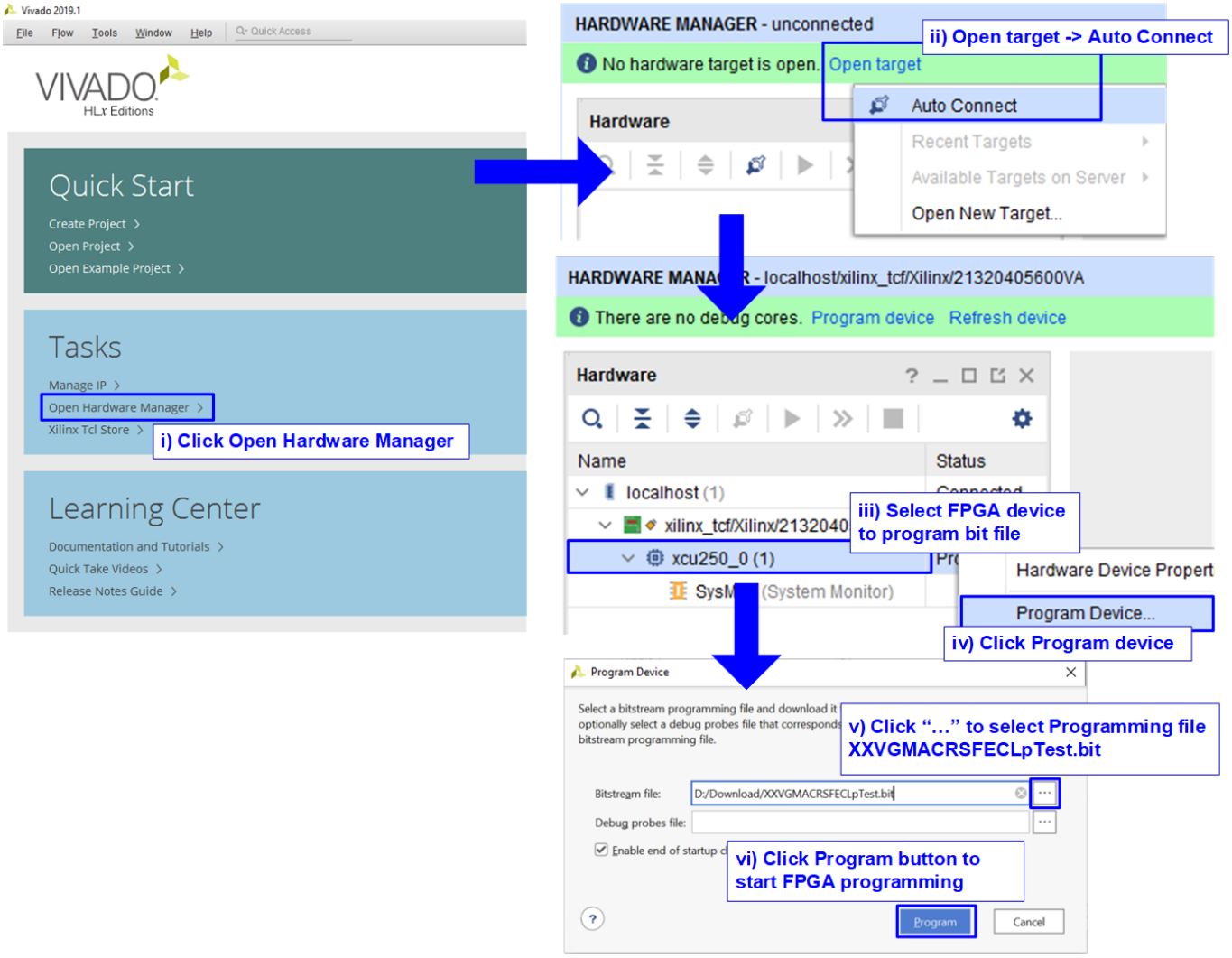

Figure 3-4 Program FPGA by Vivado

7) The Serial console displays the system initialization and welcome message as shown in Figure 3-6.
   i) Input '0' to initialize the system using an external loopback mode (SFP28 loopback module is used) or input '1' to initialize the system using an internal loopback mode. Further details about loopback modes are described in section 4.1 Reset EMAC and Transceiver.
   ii) As the system initializes, the console displays "Resetting the EMAC and Transceiver".

   If the external loopback mode is selected without plugging in the SFP28 loopback connector, the console displays an error message to indicate an incomplete initialization.

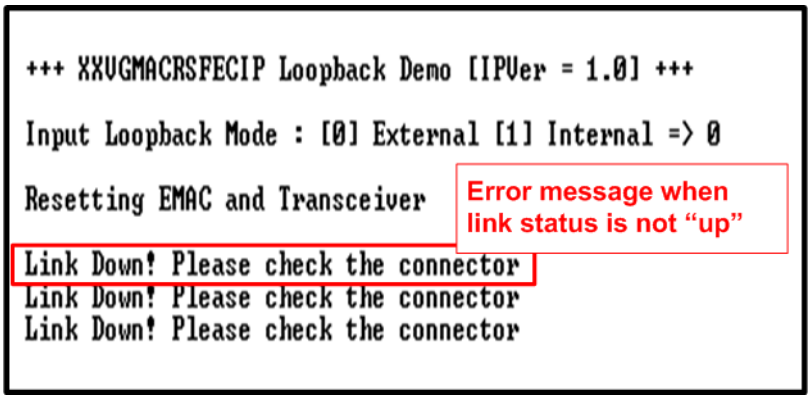

Figure 3-5 Error message when link connection status is down

   iii) Upon completion of system initialization, the console displays the message "Initialization complete" and the main menu of the XXVGMACRSFEC-IP loopback demo.

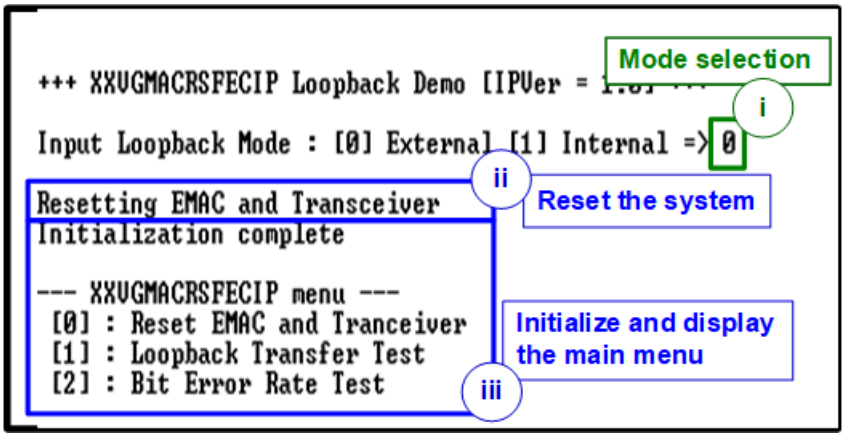

Figure 3-6 System initialization and main menu

4 Test result

4.1 Reset EMAC and Transceiver

Select ‘0’ in the demo to change the loopback mode or reset the IP and its peripherals.

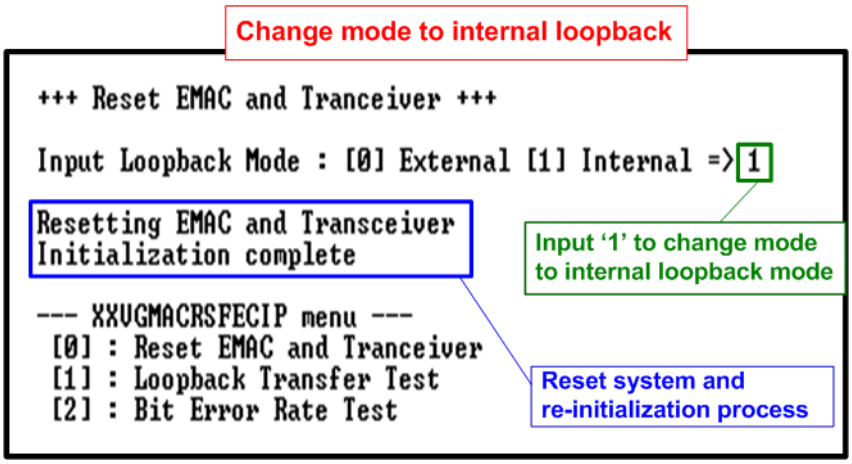

Figure 4-1 Reset and change the loopback mode to an internal mode

There are two modes available for this demo.

- Mode 0: External loopback mode is achieved by setting the loopback ports of the transceiver to “Normal operation” and using an SFP28 loopback module.
- Mode 1: Internal loopback mode is achieved by setting the loopback ports of the transceiver to “Near-End PMA loopback” mode (no SFP28 loopback module required).

After the mode is selected, a reset signal is sent to the physical layer to initiate the system reset and re-initialization process. If the external loopback mode is chosen but no SFP28 loopback module is plugged in, an error message will be displayed, as shown in Figure 3-5. Once the link up status is detected, the system initialization process is complete, and a completion message will be displayed.

4.2 Loopback Transfer Test

To initiate the loopback test, select '1' from the main menu and enter the required test parameters: packet length and the number of packets to be used in the loopback transfer test. The following sequence describes the test.

1) Under the Loopback Transfer Test menu, input two parameters.
   a) Packet length: The packet length unit is in bytes, and the valid range is 1 – 9014 bytes. The input is in decimal units if only a digit number is entered. To input the value in hexadecimal units, adds "0x" as a prefix.
   Note: If the packet length is less than 60 bytes, the IP will perform zero-padding.
   b) Number of packets: Input the number of packets to be tested. The valid value is 1 – 256. The input is in decimal units if only a digit number is entered. To input the value in hexadecimal units, adds "0x" as a prefix.
2) After valid inputs are provided, the transfer test initiates and the console displays "Send data transferring…". Once the transfer test is finished, the message "Loopback test complete" is displayed on the console. However, if any invalid inputs are entered, the console displays "Out-of-range input". The test operation is cancelled and returns to the main menu, as shown in Figure 4-3.
3) The latency performance is then calculated and displayed on the console.

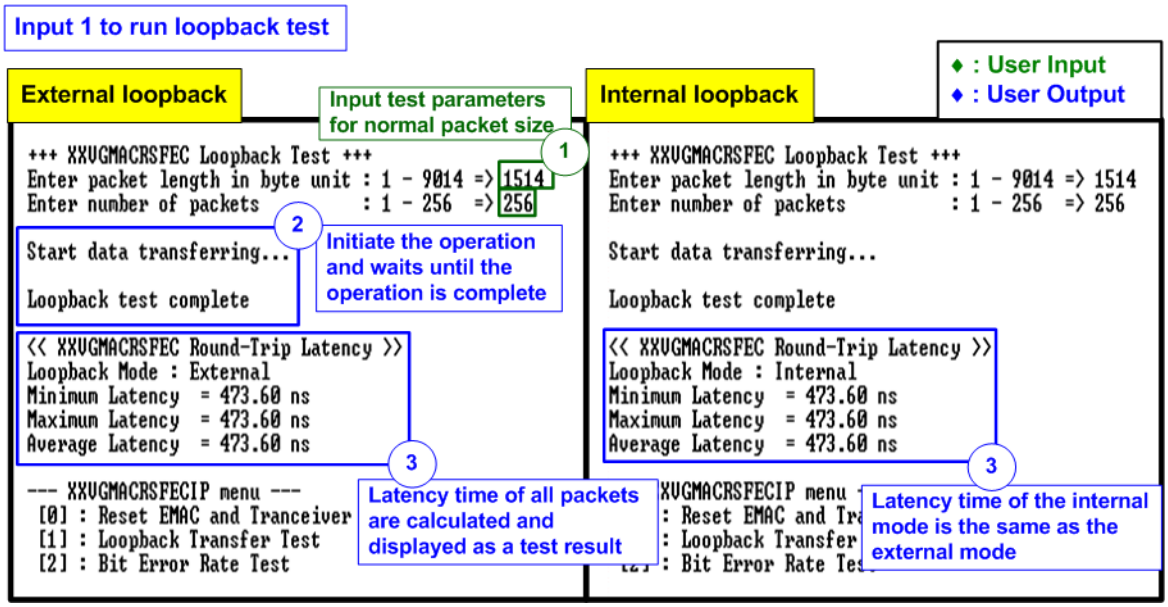

Figure 4-2 Test results of running Loopback Transfer Test

Figure 4-2 shows an example of the Loopback Transfer test results using the normal packet size (1514 bytes). The left-side window displays the result using the external loopback mode, while the right-side window displays the result using internal loopback mode. It can be observed that both tests exhibit the same latency performance of 473.60 ns. This indicates that the timer resolution used for measuring latency time (2.56 ns) is not fine enough to detect any differences in the latency time between the external and internal loopback modes.

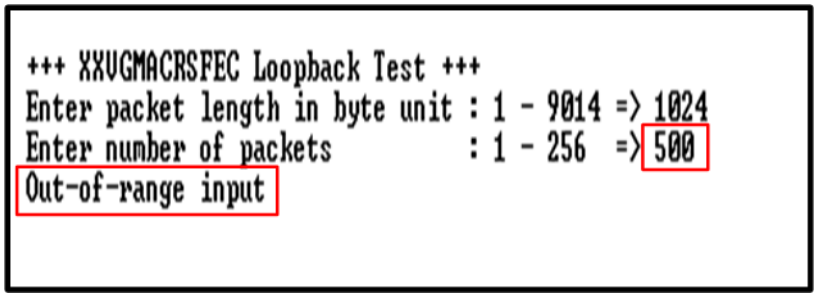

Figure 4-3 Error from invalid user input

Figure 4-4 shows two test results obtained by adjusting the packet length from the normal packet size. The left-side window displays the result using the minimum packet size (1 byte), while the right-side displays the result using the maximum packet size (9014 bytes). The latency performances of both tests result in the same number (473.60 ns), indicating that changes in packet size do not affect latency performance. These results demonstrate the IP functionalities of the jumbo-frame feature by transferring the 9014-byte data packet and also the zero-padding feature by transferring the 1-byte data packet, which is below the minimum frame size threshold.

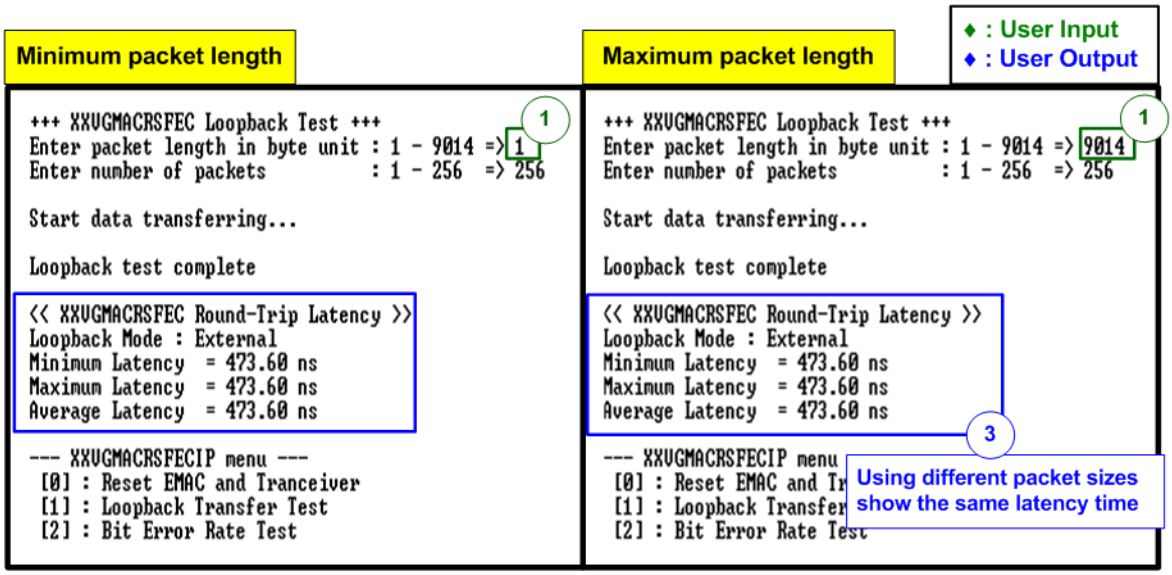

Figure 4-4 Loopback Transfer Test results of setting the minimum and maximum packet length

In this demo, the latency time is measured using a timer that operates at 390.625 MHz, providing a time unit resolution of 2.56 ns. However, the physical layer logics in this design use different clocks than the timer, which result in asynchronous logic to convert signals from other clock domains to the timer clock. This conversion causes the measured latency time to vary by one time unit or 2.56 ns.

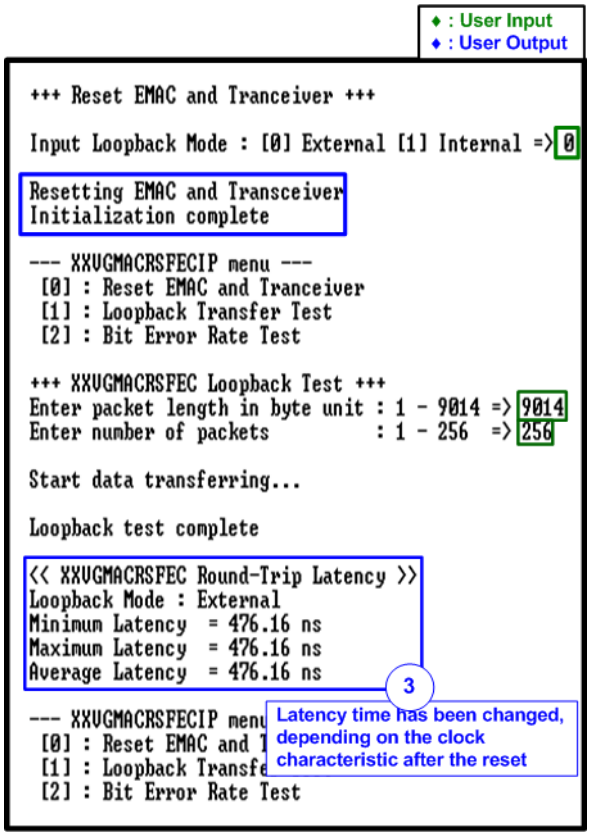

Figure 4-5 Loopback Transfer Test result has been changed

Figure 4-5 demonstrates an example where the latency time is 2.56 ns greater than the result shown in Figure 4-4. Typically, such variations in latency time can occur when the system is reset, which causes all clock signals on the FPGA to be re-locked. This, in turn, changes the phase difference of each clock, leading to variations in the measured latency time.

4.3 Bit Error Rate Test

To initiate the bit error rate test, select '2' from the main menu and enter the desired run time in seconds. The test will automatically stop after the run time has elapsed or if the user cancels the operation.

1) Input the run time in seconds. The valid range is 1 – 10,800 (3 hours). The input is in decimal units if only a digit number is entered. To input the value in hexadecimal units, adds "0x" as a prefix.
2) Verify the input values. If the input is invalid, the operation is cancelled. Otherwise, the previous test results will be reset, and the console will display "Reset Error Counter".
3) While the test is running, the console will show two optional menus.
   a) Read Rx RSFEC Error Count: This option allows the user to read the current value of all counters.
   b) Cancel operation: This option allows the user to cancel operation and return to the main menu.
4) If option '0' is selected while running, the console will display three values: the total number of received RSFEC Blocks, the number of received RSFEC Blocks with correctable error data, and the number of received RSFEC Blocks with uncorrectable error data. After that, the optional menus will be displayed on the console again.
5) When the operation is completed or cancelled by the user, the console will show the test results, including the total run time, the number of received RSFEC Blocks, the number of received RSFEC Blocks with correctable error data, and the number of the received RSFEC Blocks with uncorrectable error data.

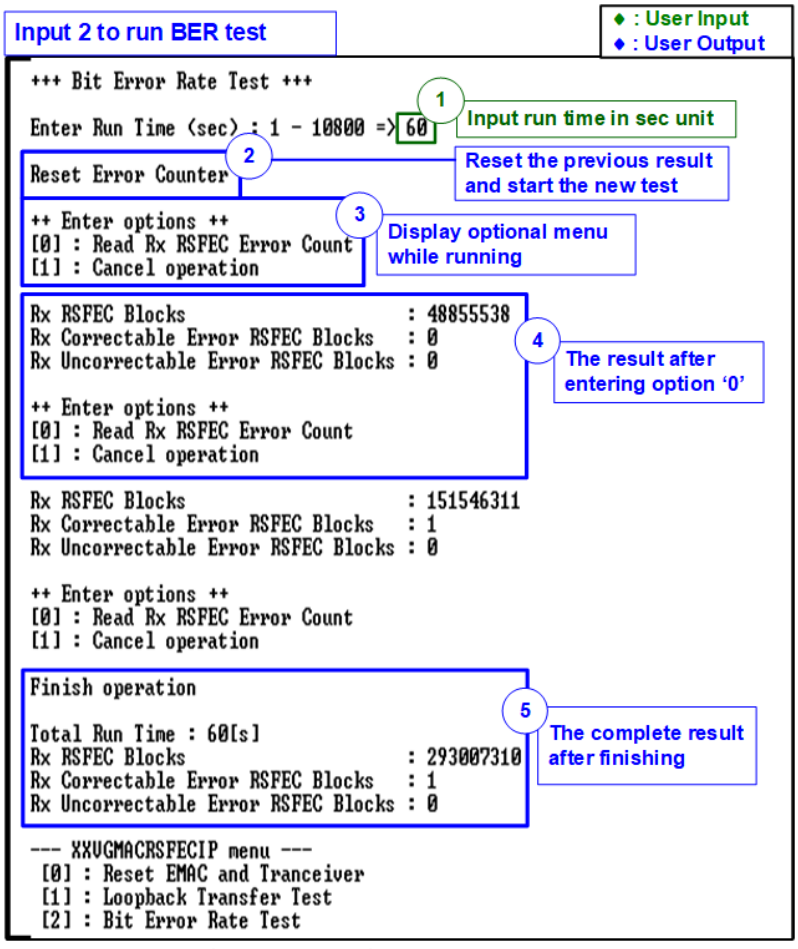

Figure 4-6 Bit Error Rate Test

An example result obtained from using the external loopback module to check the error rate for 60 seconds is illustrated in Figure 4-6. The test detected one correctable error blocks out of a total of 293,007,310 blocks, resulting in an error rate of 3.41 x 10^{-9}.

Figure 4-7 shows an example test where the user cancels the operation before completion. The console displays the latest result obtained before the cancellation.

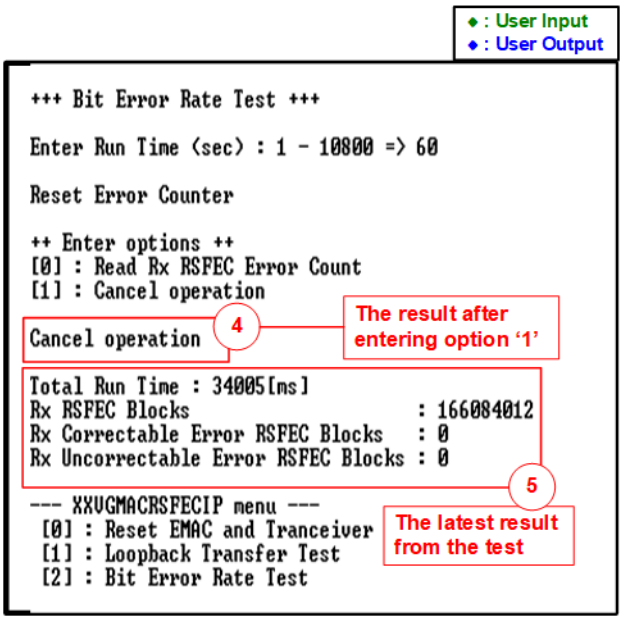

Figure 4-7 Bit Error Rate Test when cancelling the operation

5 Revision History

Revision	Date	Description
1.0	7-Apr-23	Initial version release