

Ultimate IP cores for Storage & Networking Solution



**DesignGateway is Xilinx
Alliance Program Certified Partner**

Features of **Gigabit IP core** series

■ Ultimate IP

High performance, High reliability,
Compact resource, Simple user interface

■ Support the Latest Devices

■ Ready to Evaluate on Real FPGA Boards

Able to evaluate IP core performance before purchasing
and watch performance demo on Youtube

■ Reference Design Attached with IP core License

Able to start development from the design bit by bit
to shorten time and reliable development

■ Rich Technical Documents

All technical information are available on official website

IP core Security & Configuration

FPGA logic Security System



High-speed
FPGA configuration module



DESIGN GATEWAY

C O M P A N Y L I M I T E D

NVMe IP core

Directly connect PCIe SSD without external memory!!

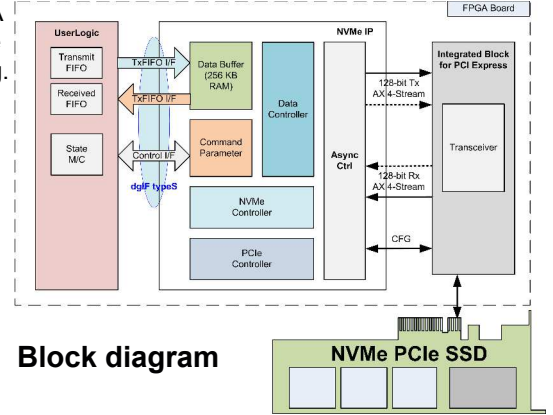
32Gbps
 Gen3 x4 Lane



Evaluation on KCU105 with Samsung SSD 960 Pro

NVMe IP core interfaces Ultra high-speed PCIe SSD without CPU and external memory. It is the best solution for applications which require ultra high-speed performance with compact system. The IP core license includes the reference design for Xilinx FPGA boards to shorten development time and reduce the cost.

Free evaluation bit files for Xilinx FPGA boards are available. You can evaluate IP core performance before purchasing.



Block diagram

Features

- Implement application layer to access PCIe SSD **without CPU and external memory**
- Support **PCIe Gen3**, theoretical upper limit 4GB/sec
- **Small resource**, the best solution for building a compact system
- **FAT32 access without CPU** * with optional FAT32-IP
- Support PLDA PCIe Gen3 Soft IP
- Free evaluation **before purchasing**

Reference Designs are available for practical applications

Easy to apply for high-end products such as ultra high-speed data recorder



2ch RAID

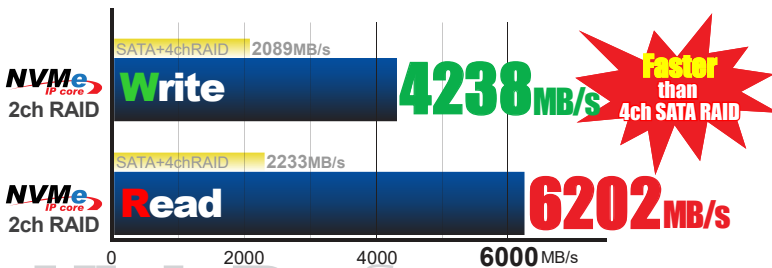


Linux driver

Suitable for high-speed data recording and stand-alone data analysis on SoC

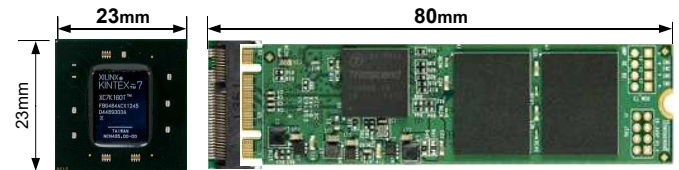
Performance/ Application

Able to build Gen3 PCIe SSD **2ch RAID** system!!



* SATA IP with Plextor PX-256M5S 4pcs
 * NVMe IP with Samsung 960Pro 2pcs

The best solution for **Compact Ultra High-speed storage system!!**



Kintex-7 (FBG484)
 NVMe IP+ user logic

M.2 SSD
 for data storage

System space image by 484pin FBG package FPGA with M.2 SSD

Product Line up

IP core	
NVMe-IP-VUP	1 project Netlist License for Virtex®UltraScale+
NVMe-IP-ZUP	1 project Netlist License for Zynq®UltraScale+
NVMe-IP-KU	1 project Netlist License for Kintex®UltraScale
NVMe-IP-VT7	1 project Netlist License for Virtex®-7
NVMe-IP-KT7	1 project Netlist License for Kintex®-7
NVMe-IP-AT7	1 project Netlist License for Artix®-7
NVMe-IP-ZQ7	1 project Netlist License for Zynq®-7000
NVMe-IP-FAT32-X	FAT32 file system for NVMe-IP. Purchase with NVMe-IP core.

Please ask us about Multi-License, Evaluation License and Maintenance support License.

Accessories for evaluation

AB16-PCIeXOVER	PCIe Crossover Adapter board for NVMe IP evaluation
AB17-M2FMC	M.2-FMC adapter board for NVMe-IP evaluation Able to connect 2 NVMe SSDs. * SSD is not included.

For more detail and technical information on our web site http://www.dgway.com/NVMe-IP_X_E.html



Designgateway IP core

検索

IP core Evaluation Demo are available on youtube



SATA IP

Serial ATA Transport & Link Layer IP Core

high-reliability & high-performance IP core proven by NASA!!

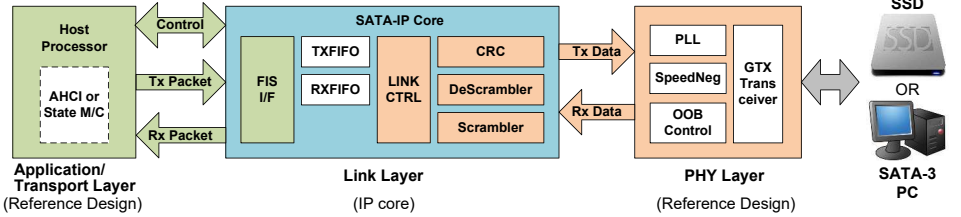
6Gbps



RAID evaluation on KC705 with 4 SSDs

SATA IP core compliant with the Serial ATA specification revision 3.0 and works on Xilinx UltraScale, 7-Series, Virtex5/6 and Spartan-6 device. This IP core provides link layer. Design Gateway provide transport layer and 150MHz GTX physical layer design for 6.0Gbps SATA3 interface as reference design. It can connect with SATA3 SSD/HDD directly without external PHY chip. The IP core license includes the reference design for Xilinx FPGA boards to shorten development time and reduce the cost.

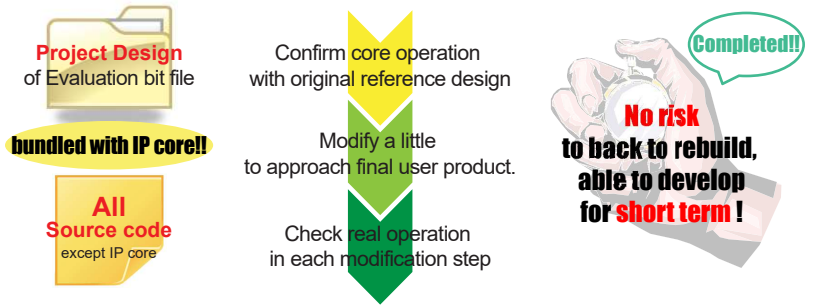
Block diagram



Features

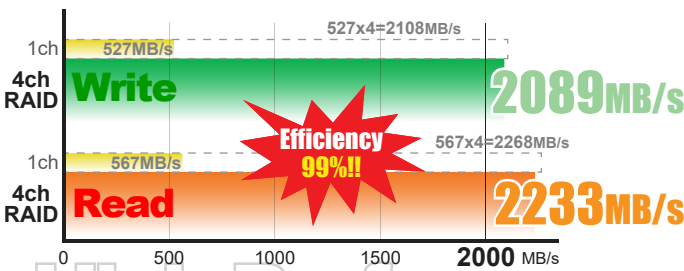
- Compliant with SATA 3.0 6Gbps
- Support both Host and Device
- AHCI for Linux boot up from Zynq-7000
- FAT32 access without CPU
* with optional HCTL-IP and FAT32-IP
- Free evaluation before purchasing
IP core Evaluation Demo are available on youtube
- Reference Design is contained with IP core license

Enhanced development support



Suitable for RAID System

High-Efficiency Loss less RAID system !!



SATA HOST IP 4ch RAID Transfer performance on KC705

Able to build RAID system by Small Resource !!

Name	1 / 1	Slice LUTs (218600)	Slice Registers (437200)	F7 Muxes (109300)	F8 Muxes (54650)	Slice (54650)
HSATARAid0x4		8142	8637	62	1	3436
u_AllIdenRam[0].u_IdenRam (Ram128x32)		1	0	0	0	1
u_AllIdenRam[1].u_IdenRam (Ram128x32_HD172)		1	0	0	0	1
u_AllIdenRam[2].u_IdenRam (Ram128x32_HD179)		1	0	0	0	1
u_AllIdenRam[3].u_IdenRam (Ram128x32_HD186)		1	0	0	0	1
u_CpuLaxi2Reg (LAXI2Reg)		209	195	18	0	116
u_IP2UFF (FIFO512x128)		51	63	0	0	28
u_SATARAid0x4IP (SATARAid0x4IP)		6769	7056	43	1	2839
u_HSATAIP0 (HSATAIPM)		1568	1628	10	0	716
u_HSATAIP1_3[1].u_HSATAIP1 (HSATAIPS)		1551	1581	10	0	658
u_HSATAIP1_3[2].u_HSATAIP1 (HSATAIPS_0)		1551	1581	10	0	657
u_HSATAIP1_3[3].u_HSATAIP1 (HSATAIPS_1)		1552	1586	10	0	675
u_Raid0x4 (Raid0x4)		302	444	3	1	139
u_TxP		27	31	0	0	12
u_TxR		35	28	0	0	14
u_TxR[1].u_RxR1 (R128x128)		27	31	0	0	13

Resource consumption of SATA IP+HCTL IP 4ch RAID reference design for KC705

Product Line up

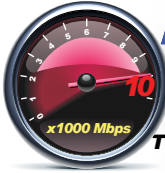
IP core	
SATA-IP-KU	1 project Netlist License for Kintex [®] UltraScale
SATA-IP-ZUP	1 project Netlist License for Zynq [®] UltraScale+
SATA-IP-KT7	1 project Netlist License for Kintex [®] 7
SATA-IP-ZQ7	1 project Netlist License for Zynq [®] 7000
SATA-IP-AT7	1 project Netlist License for Artix [®] 7
SATA-IP-VT7	1 project Netlist License for Virtex [®] 7
SATA-IP-HCTL-X	HOST IP for SATA-IP. Purchase with SATA-IP core
SATA-IP-AHCI-A	AHCI function for LinuxOS. Purchase with SATA-IP core
SATA-IP-FAT32-X	FAT32 file system for SATA-IP. Purchase with SATA-IP core
SATA-IP-exFAT-X	exFAT file system for SATA-IP. Purchase with SATA-IP core

Accessories for evaluation

AB02-CROSSOVER	SATA- SATA crossover board for SATA Device IP evaluation
AB09-FMCRAID	FMC-SATA(10ch) adapter board for SATA-IP with RAID evaluation * Available on Mouser
AB14-CLKSMA	SMA clock module for AC701

SATA-IP core for Virtex-5, Virtex-6and Spartan-6 are also available. Please ask us about Multi-License, Evaluation License and Maintenance support License. For more detail and technical information on our web site http://www.dgway.com/SATA-IP_X_E.html





TOE 10G IPcore
 TCP Offloading Engine IP Core

10GbE TCP/IP Stack Implementation by All HW Logic without CPU

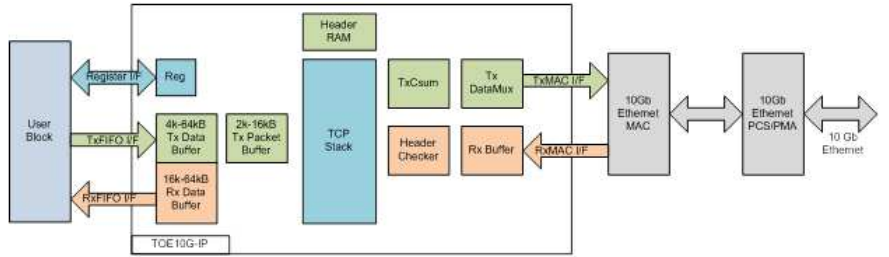
10G bit Ether

10GbE TCP Off-loading Engine(TOE10G-IP) IP core is the epochal solution implemented without CPU. Generally, TCP processing is so complicated that expensive high-end CPU is required. TOE10G-IP built by pure hardwired logic can take place of such extra CPU for TCP protocol management. This IP product includes reference design which helps you to reduce development time. DesignGateway provide demo binary file for Xilinx FPGA boards. You can evaluate TOE10G-IP core on real board before purchasing.



Real time uncompressed HD image transmission

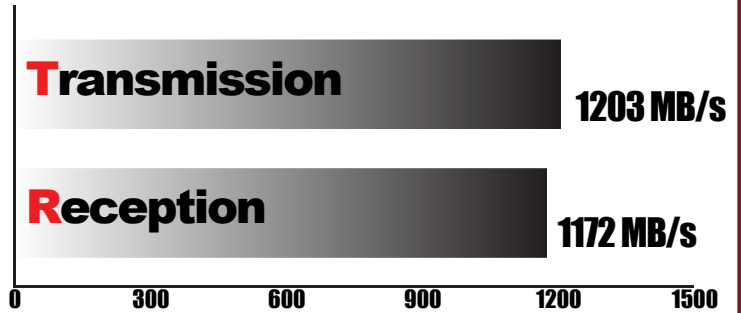
Block diagram



Features

- Over 1200MByte/sec real transfer speed
- Support Full Duplex
- Fully hard-wired TCP/IP protocol control to build CPU-less network system
- Support Multi-Session
- Free evaluation before purchasing

Performance



for 1Gbit Ethernet



1Gbit TCP Off-loading
 All Hardware Logic without CPU



Product Line up

TOE10G-IP core

TOE10G-IP-ZUP	1 project Netlist License for Zynq®Ultrascale+
TOE10G-IP-KU	1 project Netlist License for Kintex®Ultrascale
TOE10G-IP-ZQ7	1 project Netlist License for Zynq®7000
TOE10G-IP-KT7	1 project Netlist License for Kintex®7
TOE10G-IP-VT7	1 project Netlist License for Virtex®7

For more detail and technical information on our web site www.dgway.com/TOE10G-IP_X_E.html
 Please ask us about Multi-License, Evaluation License and Maintenance support License.

TOE1G-IP core

TOE1G-IP-ZQ7	1 project Netlist License for Zynq®7000
TOE1G-IP-AT7	1 project Netlist License for Artix®7
TOE1G-IP-KT7	1 project Netlist License for Kintex®7
TOE1G-IP-VT7	1 project Netlist License for Virtex®7
TOE1G-IP-SP6	1 project Netlist License for Spartan®6

For more detail and technical information on our web site www.dgway.com/TOE1G-IP_X_E.html



Ideal for network applications that require broadcast and low latency!!

- All hardware logic to achive CPU-less system
- Minimum overhead and very low latency
- Support Full Duplex
- Free evaluation before purchasing

For more detail and technical information on our web site www.dgway.com/UDP10G-IP_X_E.html and www.dgway.com/UDP-IP_X_E.html



Designgateway IP core 検索

IP core Evaluation Demo are available on youtube

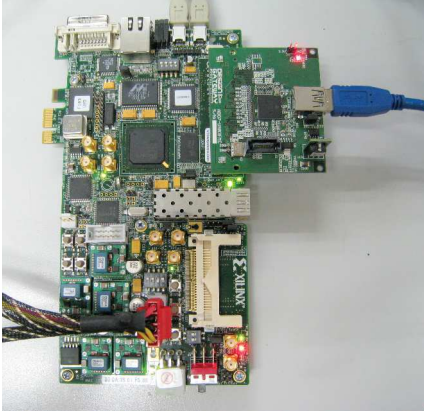


USB 3.0 IP

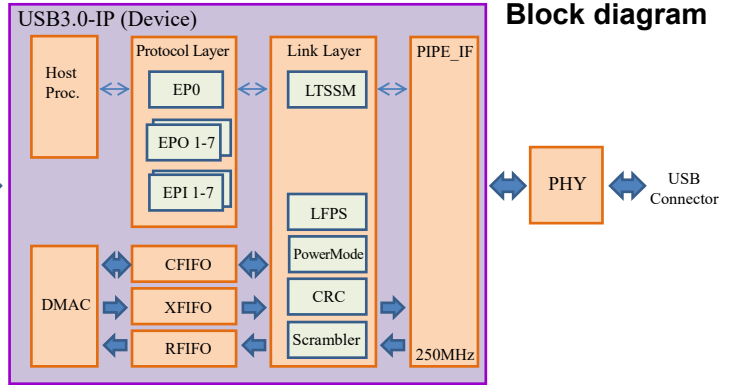
Universal Serial Bus 3.0
 Host & Device Controller IP Core

Easy to apply to FAT32 Data Recorder System!!

USB3.0 IP core compliants with the USB 3.0 specification Revision1.0. This IP core provides link layer and protocol layer. Physical layer interfaces to PHY chip by TI. Mass storage class reference design for Xilinx® FPGA board is included in the IP core license. You can start your development from the design step by step and shorten development time and reduce the cost.



USB3.0-IP Evaluation on SP605 with AB07-USB3FMC



Features



Line up both Host & Device



Ready to start Dev. on real board!!

Provide reference design for Xilinx® FPGA boards

Host IP FAT32 File access demo

Reference Designs for practical applications

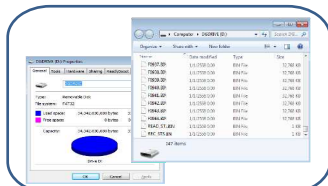
Device IP FAT32 Data recording demo

Compliant with USB 3.0 5Gbps

Support All transmission taps

Reference Designs are available for practical applications

FAT32 Data recording Design for USB3.0 Device IP core

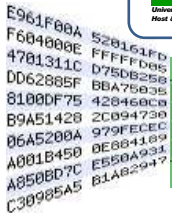


PC recognizes USB device as FAT32 external storage without any driver for Windows or Linux!!



Able to shorten development time for high-speed data recording/analysis system!!

No risk to back to rebuild, able to develop for short term!



FPGA records data and transfers it through USB3.0. At PC side, it is recognized as FAT32 files.

Product Line up

IP core	
USB3D-IP-SP6	Host IP. 1 project Netlist License for Spartan®6
USB3D-IP-VT6	Host IP. 1 project Netlist License for Virtex®6
USB3D-IP-KT7	Host IP. 1 project Netlist License for Kintex®7
USB3D-IP-VT7	Host IP. 1 project Netlist License for Virtex®7
USB3D-IP-ZQ7	Host IP. 1 project Netlist License for Zynq®7000
USB3H-IP-SP6	Device IP. 1 project Netlist License for Spartan®6
USB3H-IP-VT6	Device IP. 1 project Netlist License for Virtex®6
USB3D-IP-KT7	Device IP. 1 project Netlist License for Kintex®7
USB3H-IP-VT7	Device IP. 1 project Netlist License for Virtex®7
USB3H-IP-ZQ7	Device IP. 1 project Netlist License for Zynq®7000

Accessories for evaluation

AB07-USB3FMC AB07-USB3FMC-1.8VIF 	FMC-USB3.0 adaptor board USB3.0 TypeA to A cable (1m) is contained "-1.8VIF": FMC I/O voltage is 1.8V only.	
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Please ask us about Multi-License, Evaluation License and Maintenance support License. For more detail and technical information on our web site www.dgway.com/USB3-IP_X_E.html



YouTube Designgateway IP core 検索

IP core Evaluation Demo are available on youtube





Adapter Boards For IP Core Evaluation

AB Series is Extension Adapter Boards for Gigabit IP core evaluation. AB Series support Xilinx FPGA boards. By using AB Series, Gigabit IP cores work on Xilinx FPGA boards.

For Evaluation **before** Purchasing

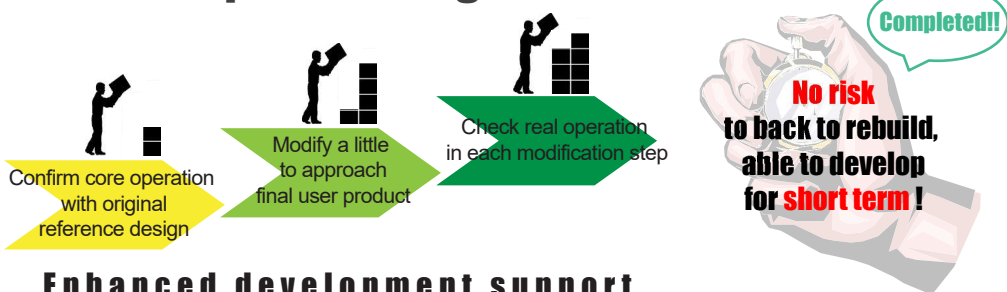


Easy and Quick Evaluation
 on Xilinx Board with **Adapter Board**

Able to confirm core operation and
 make good decision **before purchasing !!**

For Development **after** purchasing

Reference Design
 for Xilinx FPGA board
 is **included**
 in IP core license.,



Enhanced development support

Product Line up

Purchasing available on Mouser

Part Number	Description	IP core	FPGA Board
AB02-CROSSOVER	SATA- SATA crossover board for SATA Device IP evaluation Convert straight cable to SATA cross cable		
AB07-USB3FMC AB07-USB3FMC-1.8VIF	FMC-USB3.0 adaptor board USB3.0 TypeA to A cable (1m) is contained "-1.8VIF" : FMC I/O voltage is 1.8V only.		KC705, ZC706, SP605, ML605 VC707, VC709, KCU105
AB09-FMCRAID	FMC-SATA(10ch) adapter board for SATA-IP with RAID evaluation		KCU105, KC705, ZC706 AC701, VC709, VC707 Avnet Mini-ITX
AB14-CLKSMA	SMA clock module for AC701		AC701
AB16-PCIeXOVER	PCIe Crossover Adapter board for NVMe IP evaluation		ZCU106, KCU105 ZC706, KC705 VC707, VC709
AB17-M2FMC	M.2-FMC adapter board for NVMe-IP evaluation. Able to connect 2 NVMe SSDs. * SSD is not included.		ZCU102 and FMC I/F mounted Xilinx FPGA boards



IP Lock

Protect Intellectual Property from illegal copy

AES 128

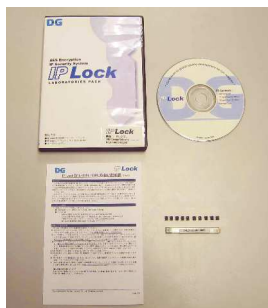
IPLock is FPGA logic security system which used very reliable AES encryption technology. IP properties in FPGA are protected from illegal copy by only including IP Lock in FPGA and connecting with encryption controller chip.

Features

- Strong security by **AES-128** encryption
- Change & encrypt true random authentication data
- Immediately stop user logic without the chip
- **Just 2 line** connection between FPGA and IP Lock
- **Laboratories Pack** for prototype, already written unique ID
- **Writer Set & Blank Encryption chip** for mass production



Laboratories Pack for prototype



Contents of Laboratories pack. Encryption chips unique ID inside

Laboratories Pack contains encryption chips which are already written unique ID at shipment by Design Gateway. No one can rewrite this fixed ID key. To avoid duplication, each Laboratories pack have different unique ID key, so user must use IP Lock core with encryption chips in same package. Design Gateway provide encryption chip 10 pcs package (IPL-010L) and 30 pcs package (IPL-030L). This product is suitable for prototype and small lot usage.

IPL-010L	IP core netlist + encryption controller chip (unique ID inside) 10pcs pack
IPL-030L	IP core netlist + encryption controller chip (unique ID inside) 30pcs pack

Writer Set for mass production



IPLock Writer and IPL-CHP

Writer pack is suitable for mass production. User can write any ID key to blank encryption chip by using IP Lock write. User can set and write optional ID key for each products or lot. Writer pack contains blank chip 3 pcs. For mass production, The Writer pack is used with Blank Chip



YouTube

Designgateway IPLock

IPLock Demo is available on youtube

Easy to protect your IP core & logic data !

- Step1: Prepare SOIC-8 pattern for security chip on your board
- Step2: purchase IP Lock for FPGA logic protection
- Step3: Compile your FPGA logic with IP Lock core
- Step4: Put IP Lock security chip on FPGA board
- Step5: Complete IP core protection!



IPL-003WR	IPLock Writer, IPLock core + IPL-CHP 3pcs (Blank Encryption chip)
IPL-CHP	Blank Encryption chip for IPL-003WR (MOQ 100pcs)



Purchasing available on Mouser

For more detail and technical information on our web site http://www.dgway.com/IPLock_E.html



SD LINK

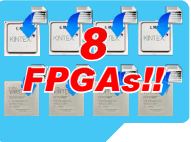
Convenient and High-Speed Configuration Module via microSD

**SDHC
microSD
bundled**



3sec!! Ultra High-Speed Programming!!

Just 3 second to program 20MBytes (=160Mbit) configuration data. (comparison with on board flash, it takes about 7 minutes...)



8 FPGAs!!

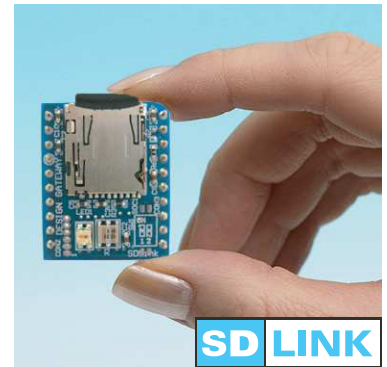
Only one SDLink can configure up to 8 FPGAs at same time.



Easy!!

Just **swap** microSD to update & change circuit data **immediately!!**

Convenient update without Programming tools, Download cable and System suspended.

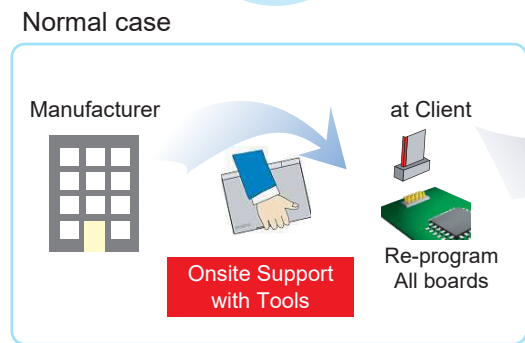


SDLink is a high speed FPGA configuration module which stores data on microSD card. FPGA configuration data is easily updated by just swapping microSD card.

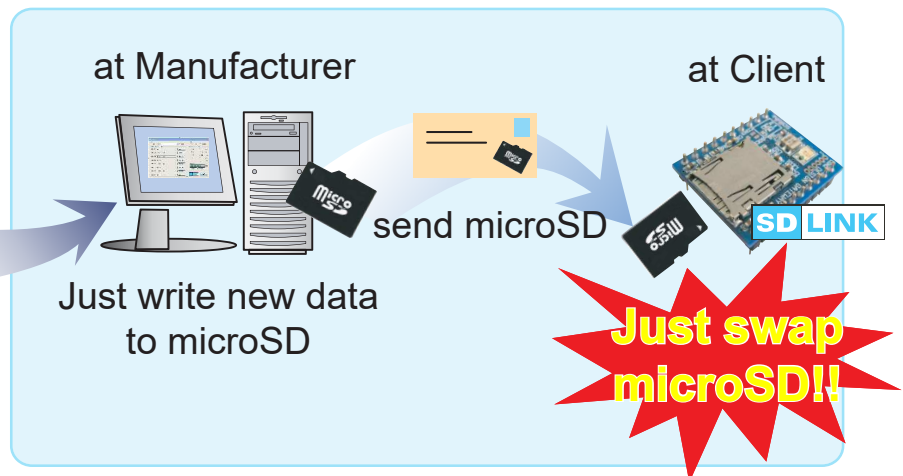
High-Speed Configuration Convenient field update
Tool free High-Speed Programming Easy to swap

Practical example

Re-programming or update after releasing product



In case of SD LINK



Product Line up

SL001	SDHC microSD 1pc bundled	Purchasing available on Mouser
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For more detail and technical information on our web site http://www.dgway.com/SDLink_E.html

Designgateway SDLink

SDLink Demo is available on youtube

