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FTP 10G Server FPGA Setup

Rev2.1 29-Jun-23

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This document describes how to setup FPGA board and prepare the test environment for running FTP 10G Server demo on FPGA development board by using FileZilla version 3.45.1 as FTP client. NVMe SSD is applied as the storage for storing file transferred with TestPC by using FTP protocol via 10Gb Ethernet. User sets the test parameters on FPGA and monitors the hardware status via Serial console.

1 Environment Requirement

To run FTP Server demo, please prepare following test environment.

- 1) FPGA development board: KCU105, ZCU106, or ZCU102
- 2) Test PC with 10 Gigabit Ethernet support or 10 Gigabit Ethernet card with the installed program as follows:
 - Vivado tool for program the FPGA
 - FileZilla version 3.45.1 to be test application
 - Serial console software such as HyperTerminal or TeraTerm installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- 3) 10 Gb Ethernet cable:
 - a) 10 Gb SFP+ Passive Direct Attach Cable (DAC) which has 1-m or less length
 - b) 10 Gb SFP+ Active Optical Cable (AOC)
 - c) 2x10 Gb SFP+ transceiver (10G BASE-R) with optical cable (LC to LC, Multimode)
- 4) The PCIe adapter board (AB18-PCIeX16, AB17-M2FMC or AB16-PCIeXOVR) provided by Design Gateway
https://dgway.com/ABseries_E.html
- 5) NVMe SSD connecting to PCIe adapter board
- 6) Two micro USB cables connecting between FPGA board and PC (one for programming FPGA and another for Serial console)
- 7) Xilinx power adapter for FPGA board
- 8) ATX power supply for AB18-PCIeX16 adapter board

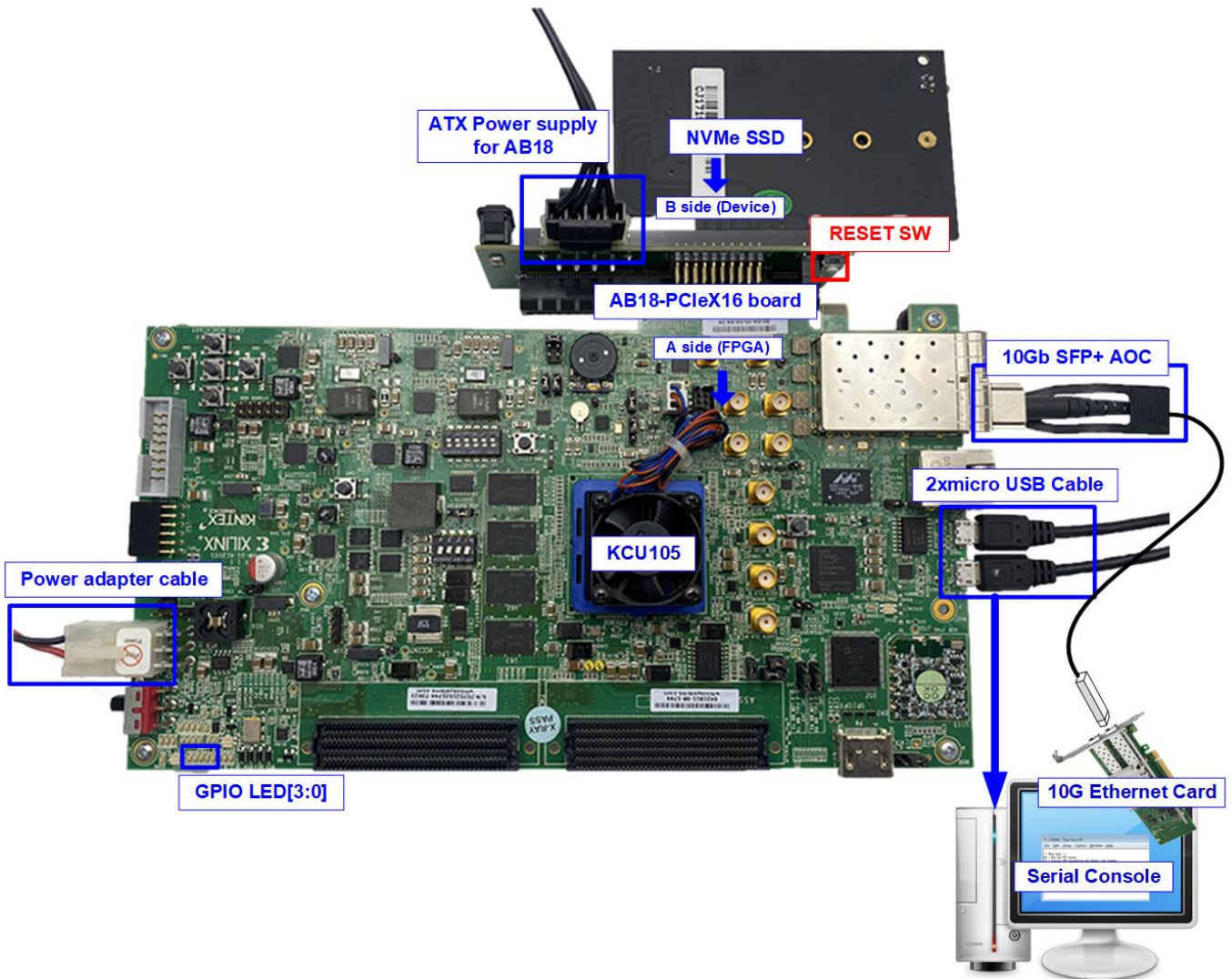


Figure 1-1 FTP Server demo on KCU105 with AB18

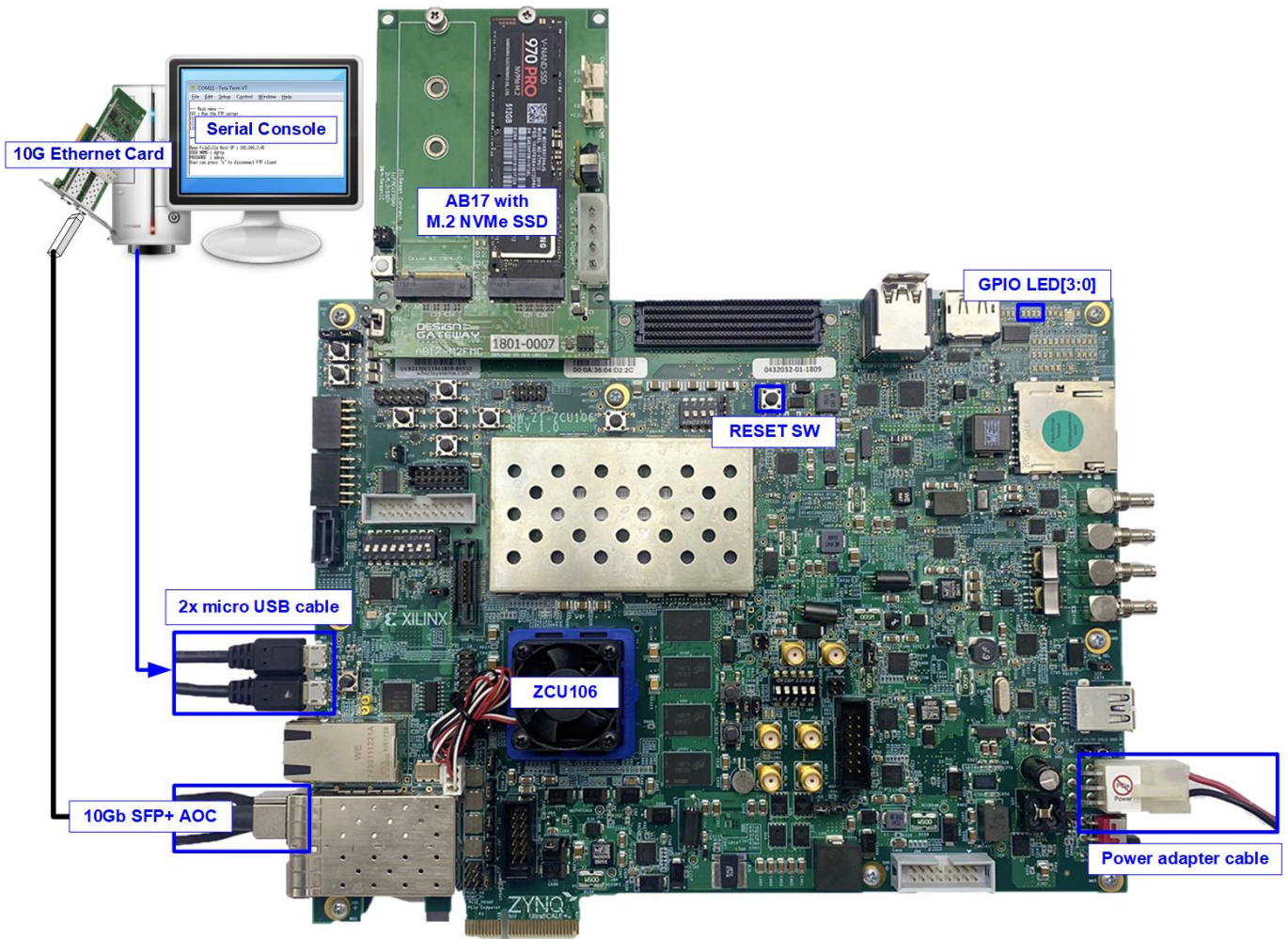


Figure 1-2 FTP Server demo on ZCU106 with AB17

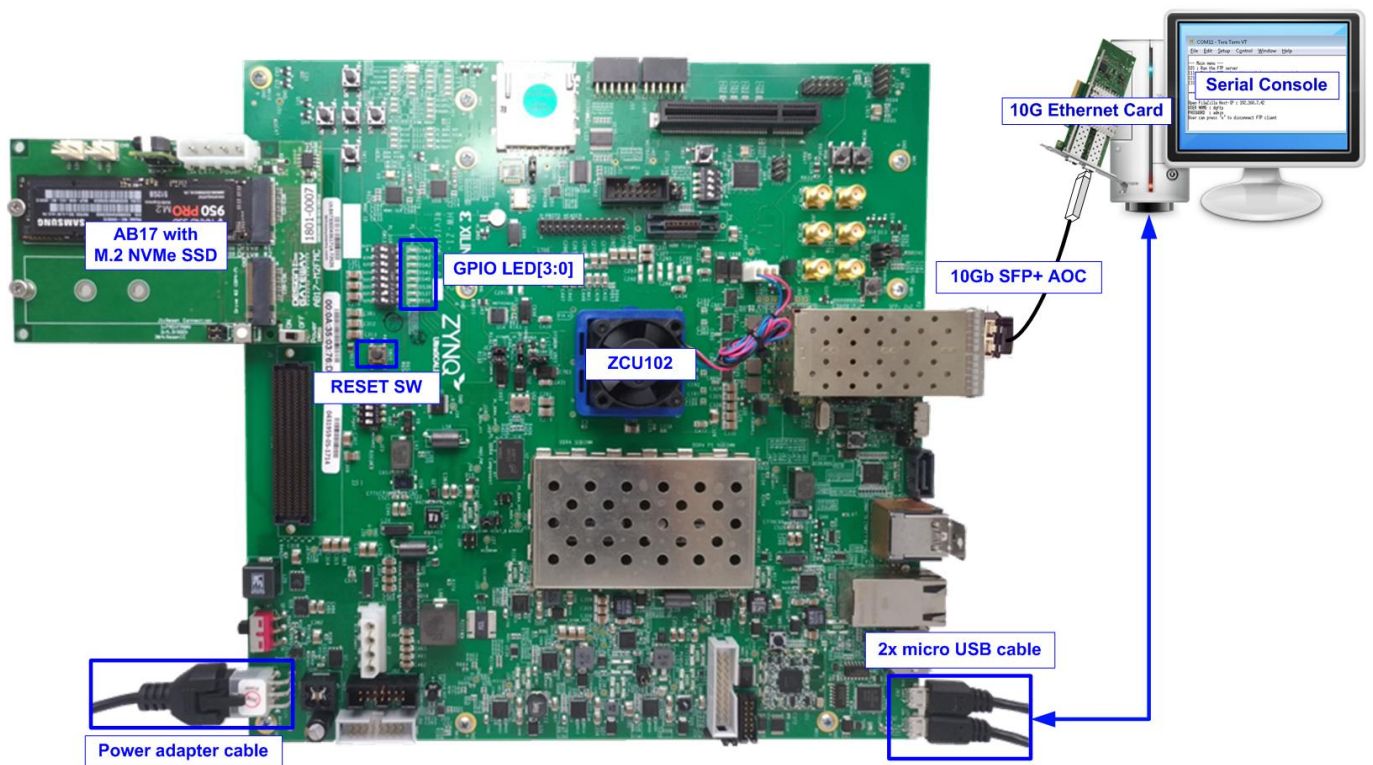


Figure 1-3 FTP Server demo on ZCU102 with AB17

2 FPGA board setup

- 1) Power off system.
- 2) Check board configuration as follows,
 - i) On KCU105 and ZCU105 board, insert jumper to enable Tx SFP+
 - For KCU105 board, insert jumper to J6
 - For ZCU102 board, insert jumper to J16

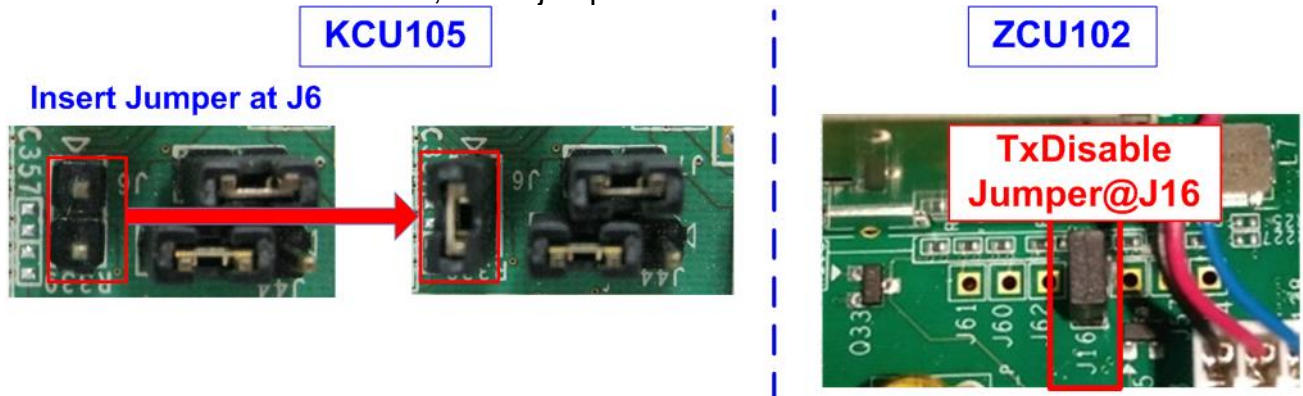


Figure 2-1 Insert jumper to enable SFP+ on KCU105/ZCU102

- ii) On ZCU106 and ZCU102, configure PS from JTAG by setting SW6=all ON

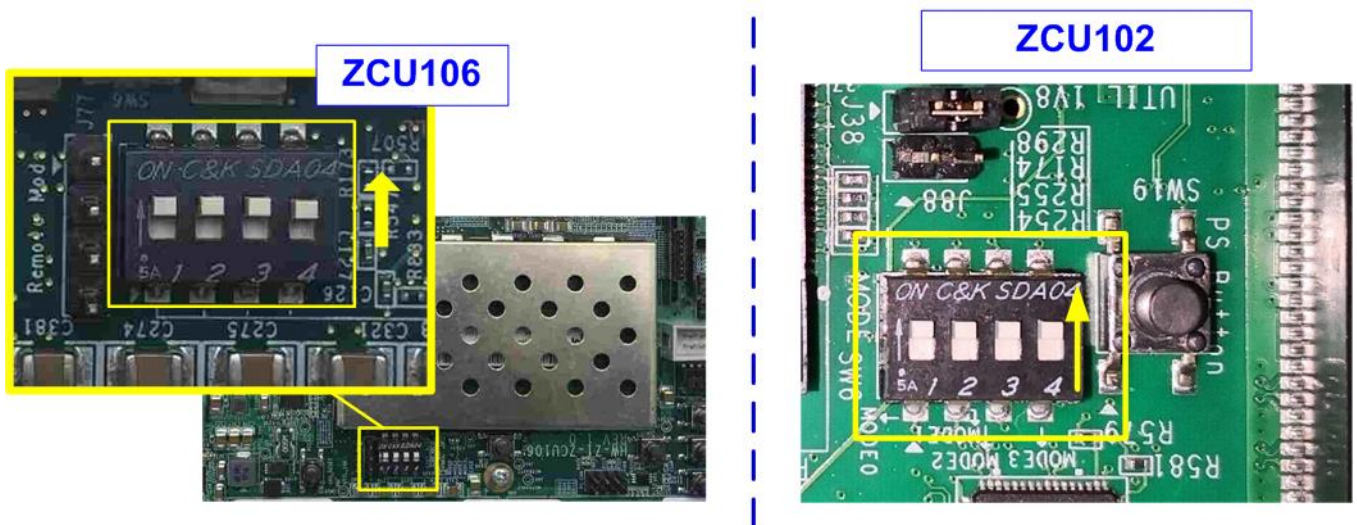


Figure 2-2 SW6 setting to configure PS from JTAG on ZCU106/ZCU102

- 3) Setup and connect NVMe SSD to PCIe adapter board.
 For KCU105, connect to AB18-PCIeX16 and AB16-PCIeXOVR.
 - i) Confirm that two mini jumpers are inserted at J5 connector on AB18.
 - ii) Connect ATX power supply to AB board.
 - iii) Connect PCIe connector on FPGA board to FPGA Side (A-side) and connect NVMe PCIe SSD to device side (B-Side) on AB board, as shown in Figure 2-3.

Caution: Please confirm that the SSD is inserted in the correct side of AB18 (B-side, not A-side) before power on system

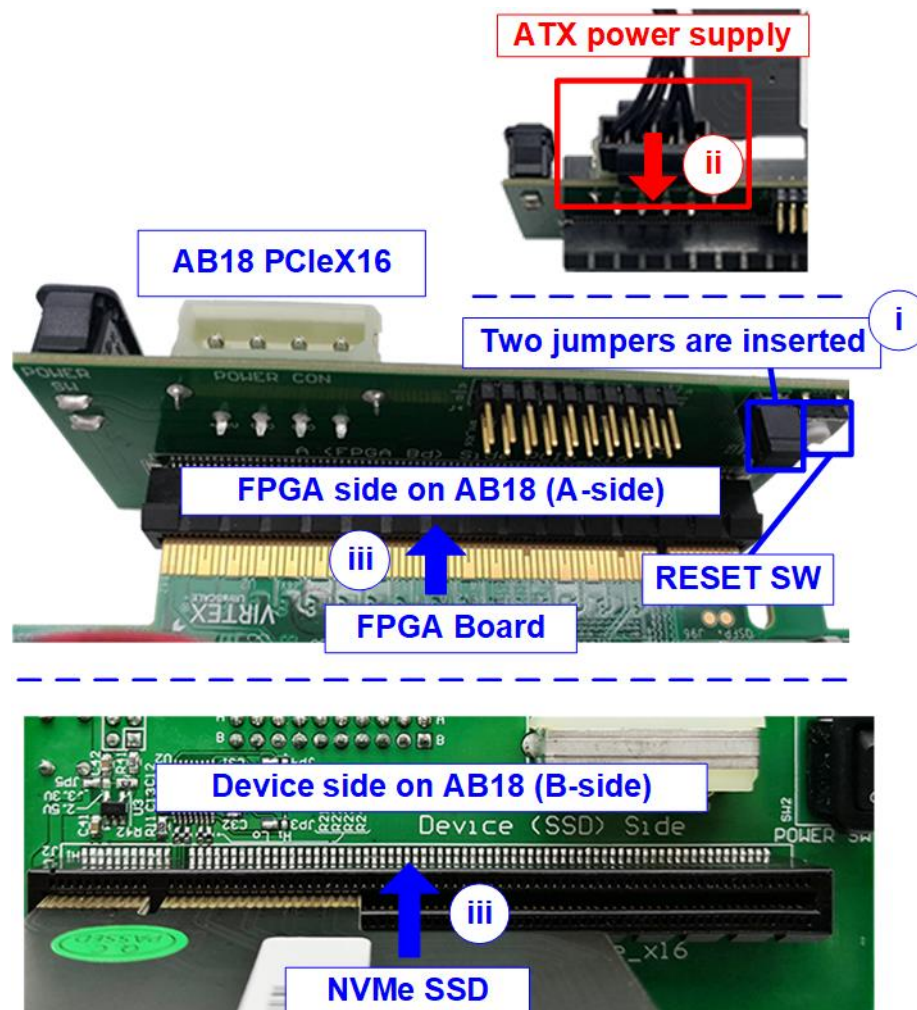


Figure 2-3 Connect AB18-PCIeX16 to KCU105

For ZCU106/ZCU102, connect to AB17-M2FMC.

- i) Connect M.2 NVMe SSD to Drive#1 M.2 connector on AB17-M2FMC.
- ii) Connect AB17-M2FMC to HPC/HPC1 connector on ZCU106(J5) or ZCU102(J4) as shown in Figure 2-4.

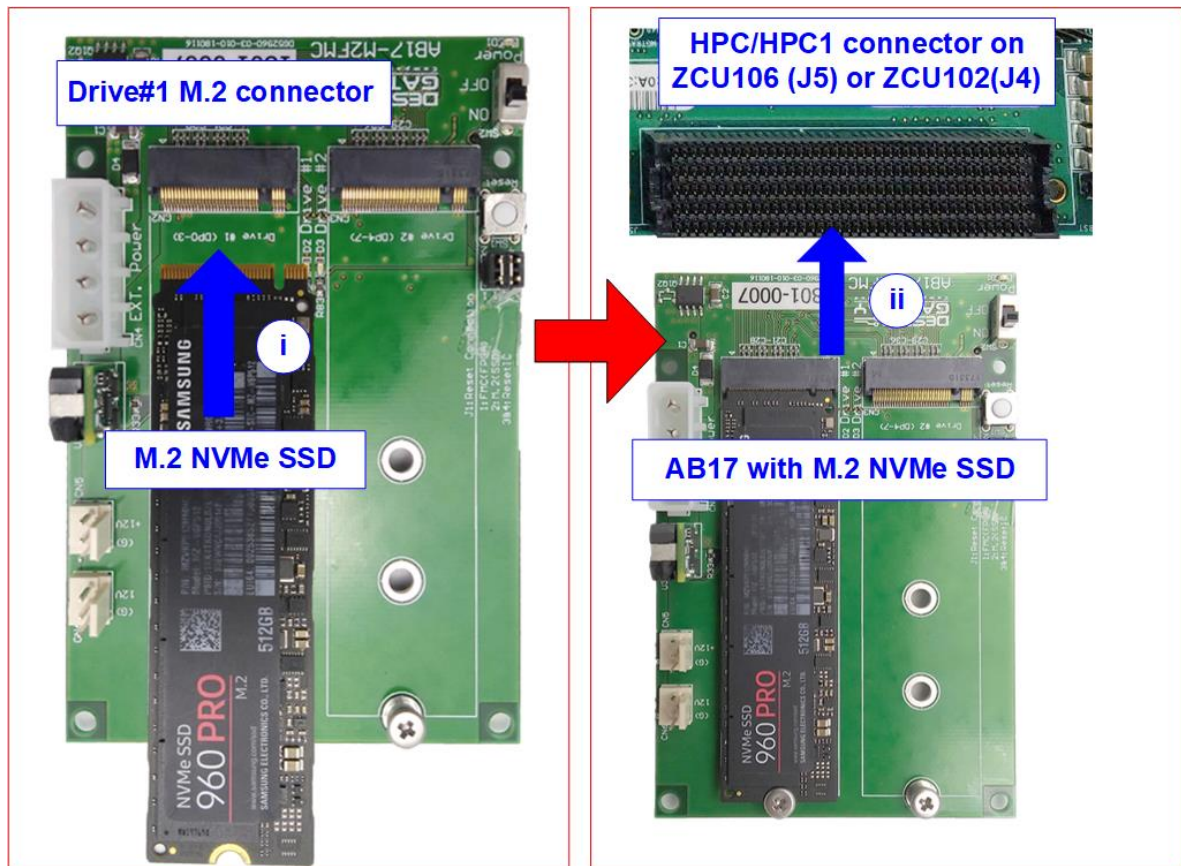


Figure 2-4 Connect AB17-M2FMC connection

- 4) Connect 10Gb Ethernet cable between FPGA board and PC by inserting 10 Gb SFP+ DAC (Length<1m), AOC or SFP+ transceiver with LC-LC cable, as shown in Figure 2-5.

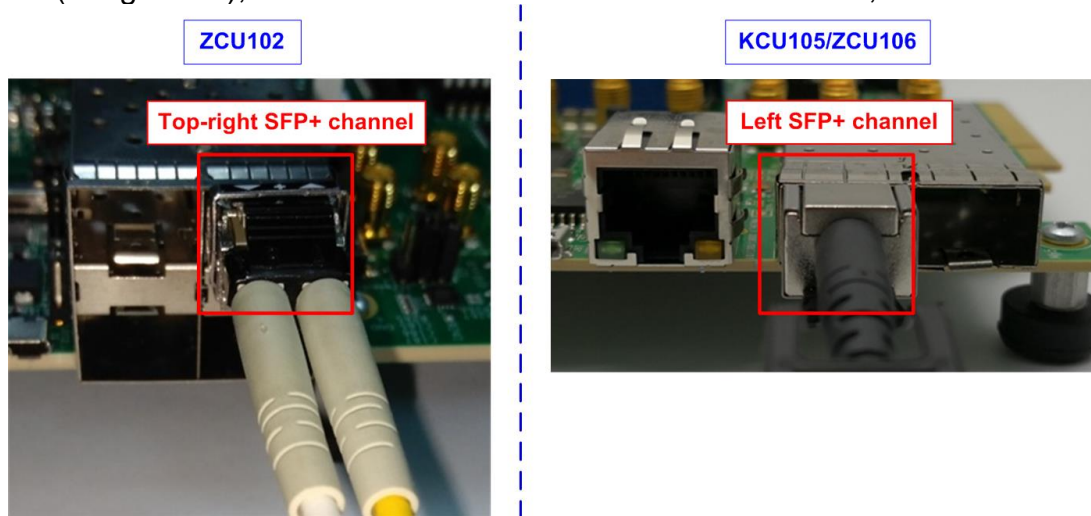


Figure 2-5 SFP+ channel using on ZCU102/ZCU106/KCU105 board

- 5) Connect two micro USB cables from FPGA board to PC for JTAG programming and Serial console.

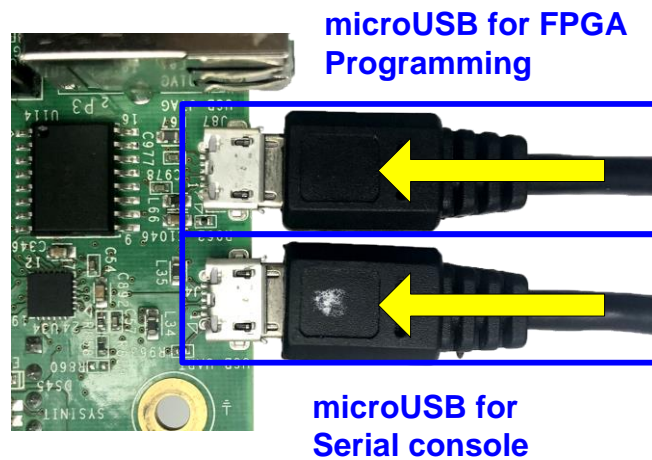


Figure 2-6 micro USB connection of FPGA

- 6) Turn on power switch on FPGA development board, and then turn on power switch on the adapter board, as shown in Figure 2-7.

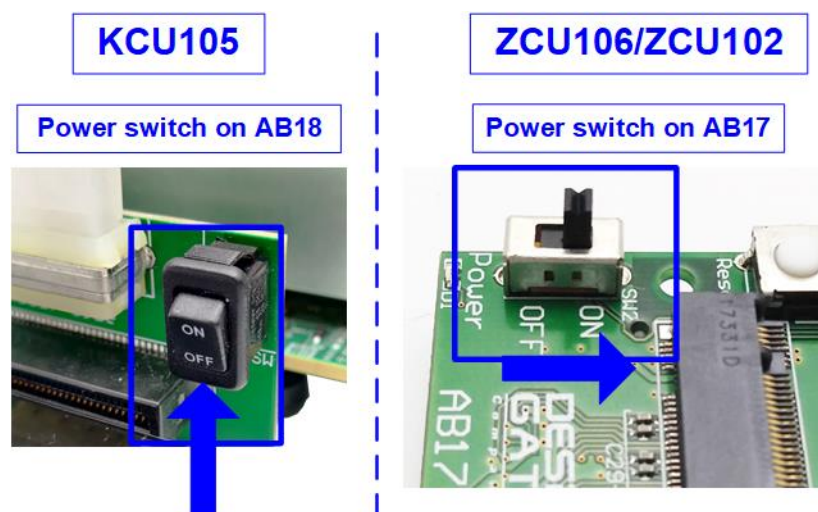


Figure 2-7 Turn on power switch on FPGA and adapter board

- 7) Open Serial console. When connecting FPGA board to PC, many COM ports from FPGA connection are detected and displayed on Device Manager. In case of KCU105, select Standard COM port. In case of ZCU106/ZCU102, select COM port number of Interface0. On Serial console, use following setting: Buad rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

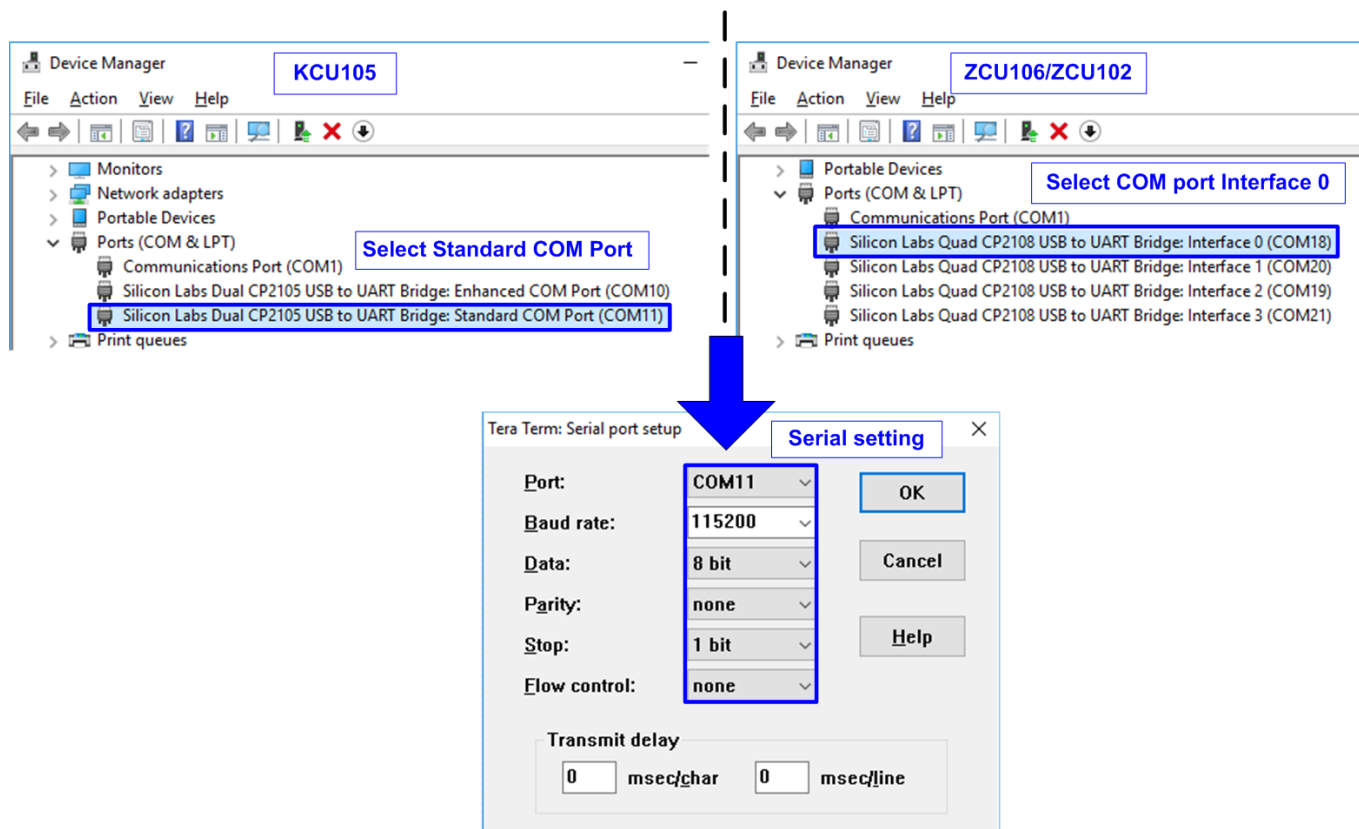


Figure 2-8 Select and set COM Port

- 8) Download configuration file and firmware to FPGA board
 For KCU105, configure FPGA by using Vivado, as shown in Figure 2-9.

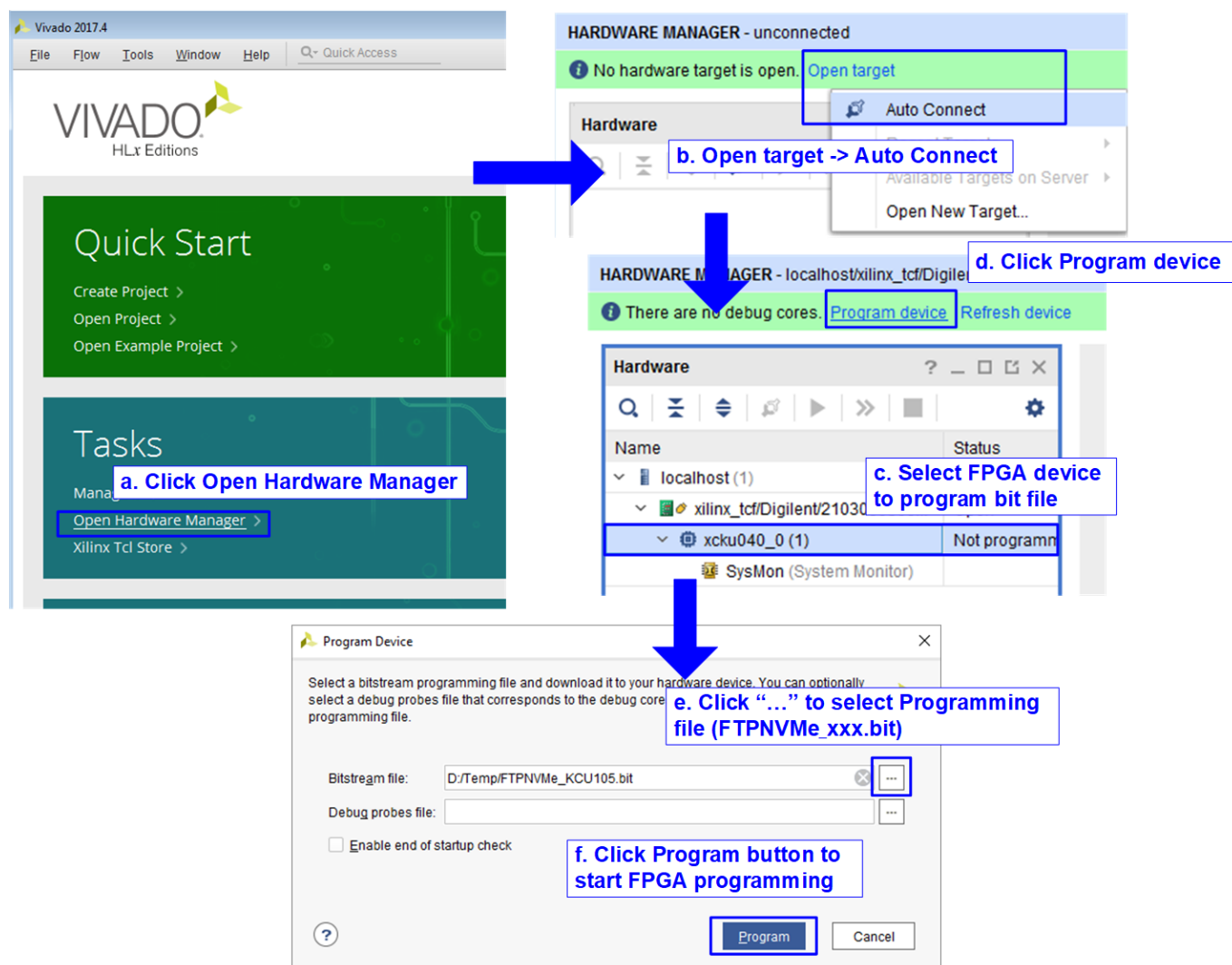


Figure 2-9 Program FPGA by using Vivado

For ZCU106/ZCU102 board, open Vivado TCL shell and run FTPNVMe_ZCU106/102, as shown in Figure 2-10.

```

C:\> Vivado 2017.4 Tcl Shell - C:\Xilinx\Vivado\2017.4\bin\vivado.bat -mode tcl

***** Vivado v2017.4 (64-bit)
**** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
**** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

Vivado% cd E:/Temp/download
Vivado% FTPNVMe_ZCU106.bat
  
```

Go to directory that batch file is located

Run script file to download bit and elf file

Figure 2-10 Command script to download demo file on Vivado TCL shell

3 Revision History

Revision	Date	Description
1.0	4-Apr-20	Initial version release
2.0	22-Jul-20	Remove instruction from the document and support ZCU106
2.1	14-Mar-22	Support ZCU102