NVMe IP with PCIe Gen3 Soft IP demo instruction

Rev1.1 20-Apr-20

This document describes the instruction to run NVMeG3 IP demo on FPGA development board by using the PCIe adapter board (AB18-PCIeX16 board, AB17-M2FMC adapter board, or AB16-PCIeXOVR board). The demo is designed to write/verify data with NVMe SSD. User controls the test operation through Serial console.

1 Environment Requirement

To run the demo on FPGA development board, please prepare following environment.

1) Supported FPGA Development board: ZCU102, VCU118, and KCU105
2) PC installing Xilinx programmer software (Vivado) and Serial console software such as TeraTerm
3) The PCIe adapter board, provided by Design Gateway
   https://dgway.com/ABseries_E.html
   - AB17-M2FMC adapter board: ZCU102
   - AB18-PCIeX16 board: KCU105, VCU118.
   - AB16-PCIeXOVR board: KCU105
4) Xilinx power adapter for FPGA board
5) ATX power supply for PCIe adapter board
6) NVMe SSD
   - Insert M.2 NVMe SSD to Drive#1 on AB17.
   - Connect PCIe NVMe SSD to B side on AB18/AB16.
7) Two micro USB cables for programming FPGA and Serial console, connecting between FPGA board and PC

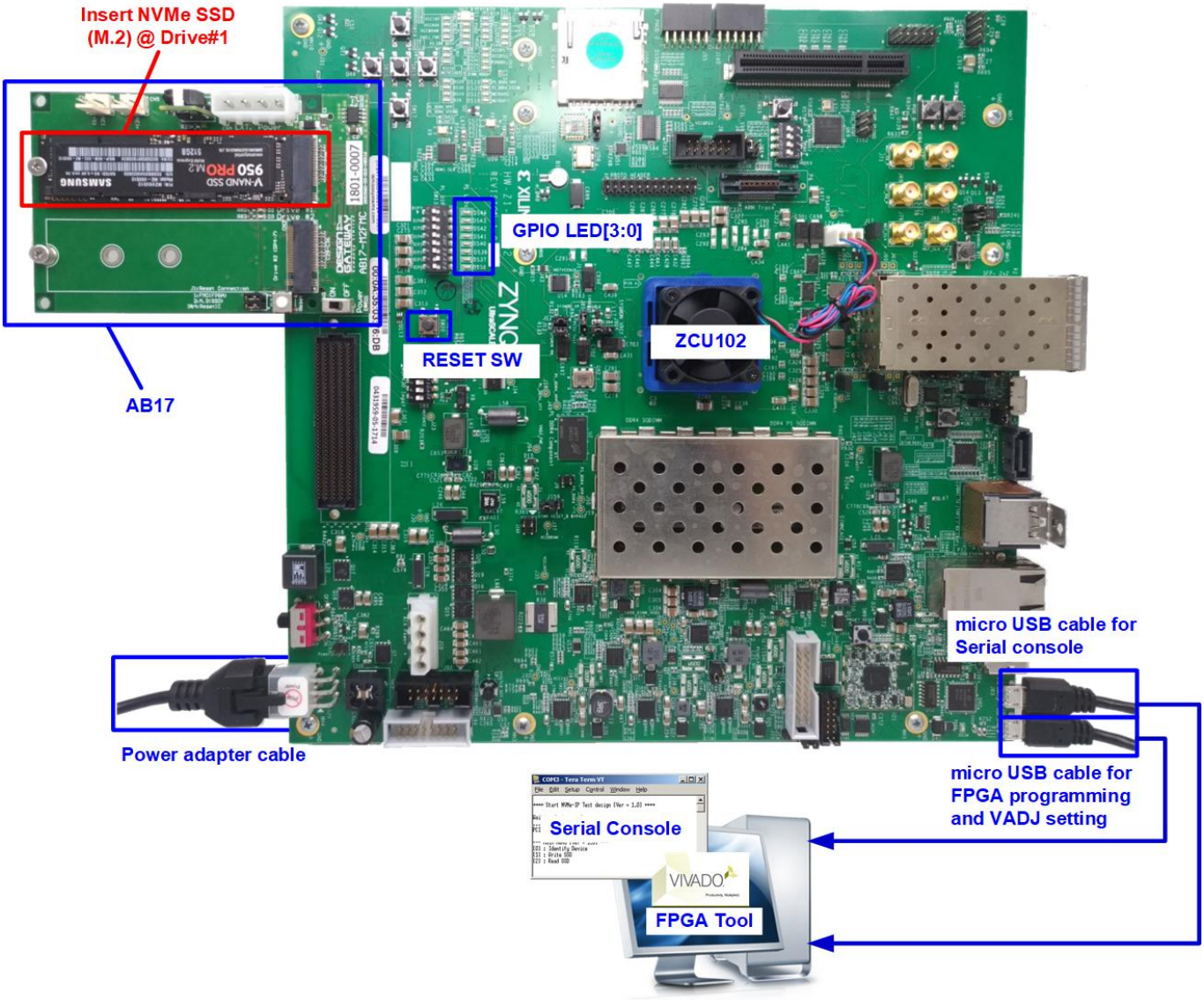


Figure 1-1 NVMeG3 IP demo environment setup on ZCU102

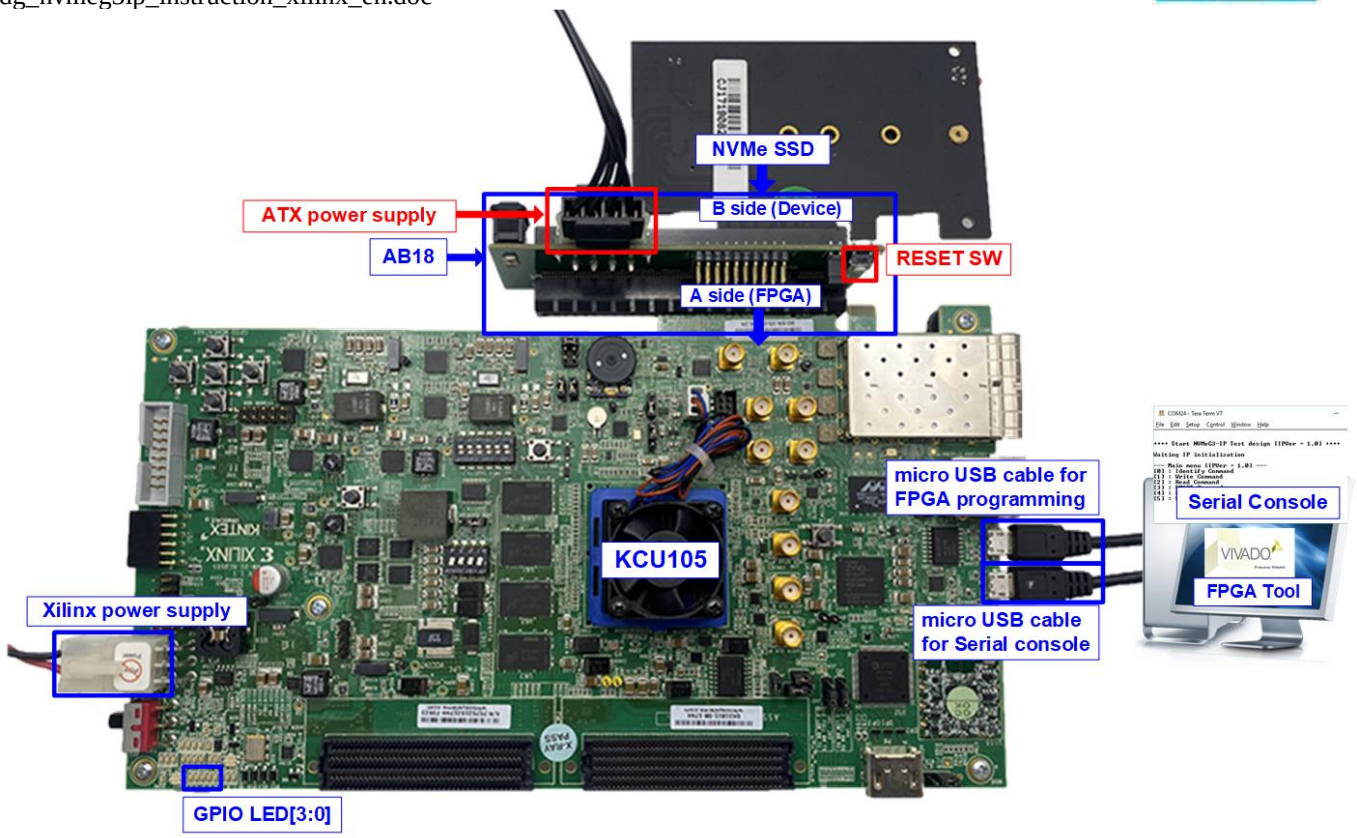


Figure 1-2 NVMeG3 IP demo environment setup on KCU105

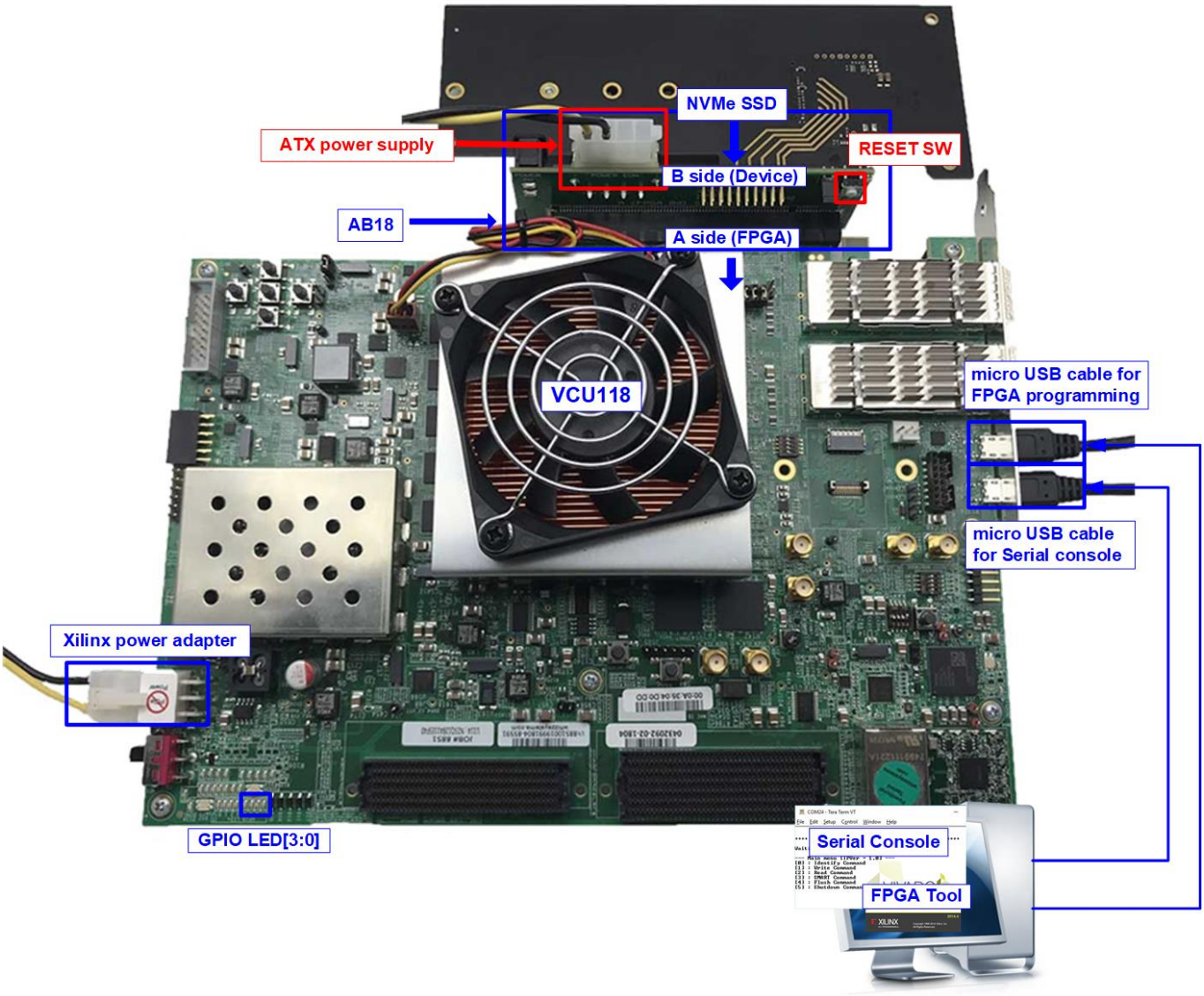


Figure 1-3 NVMeG3 IP demo environment setup on VCU118

2 Demo setup

1) Power off system.
2) For ZCU102, set SW6=all ON to configure PS from JTAG, as shown in Figure 2-2.

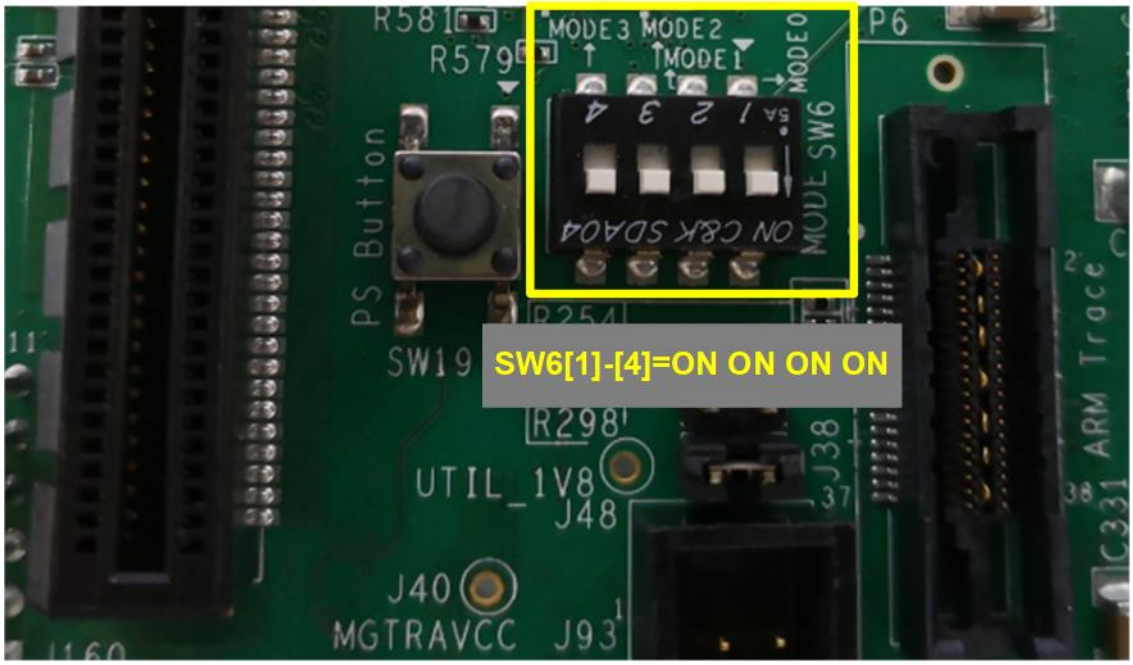


Figure 2-1 DIPSW for setting to configure PS from JTAG on ZCU102

3) Connect NVMe SSD to adapter board and then connect the adapter board to FPGA development board.
   a) For ZCU102, connect NVMe SSD (M.2) to Drive#1 M.2 connector on AB17-M2FMC and then connect AB17 to HPC1 connector on ZCU102 (J4).

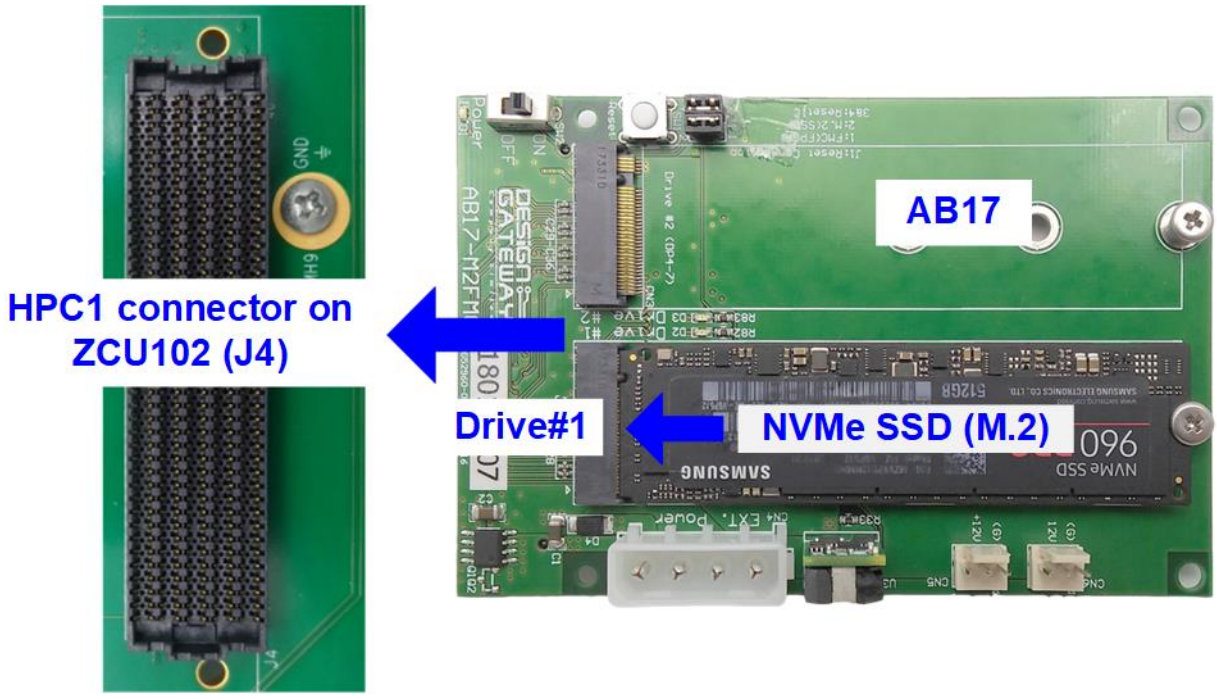


Figure 2-2 Connect M.2 NVMe to AB17

b) For KCU105 and VCU118,

- Connect ATX power supply to AB18/AB16 board.

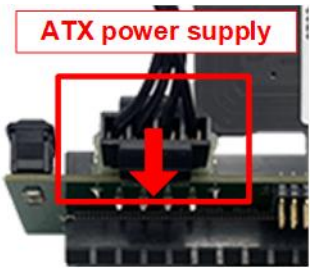


Figure 2-3 Connect ATX power supply to PCIe adapter board

- Confirm that two mini jumpers are inserted at J5 connector on AB18/AB16.
- Connect FPGA Side (A-side) on AB18/AB16 to PCIe connector on FPGA board
- Connect NVMe SSD (PCIe) to device side (B-Side) on AB18/AB16, as shown in Figure 2-4.

Warning: Please confirm that NVMe SSD is inserted in the correct side of AB18/AB16 (B-side, not A-side) before power on system.

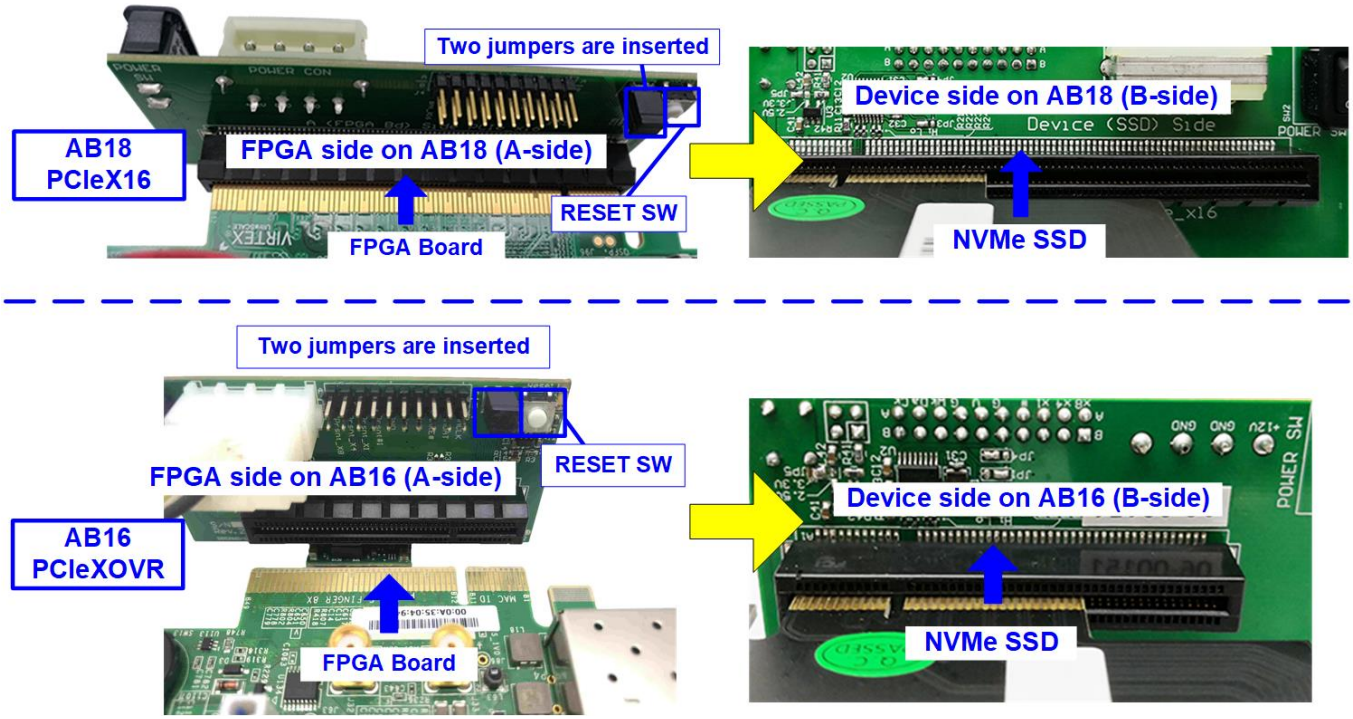


Figure 2-4 Connect Adapter board to NVMe SSD (PCIe) and FPGA board

4) Connect Xilinx power adapter to FPGA development board and connect two micro USB cables between FPGA board and PC for FPGA programming and Serial console.

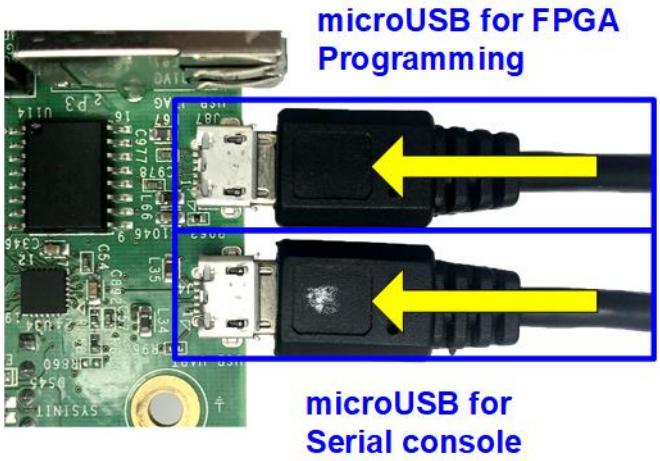
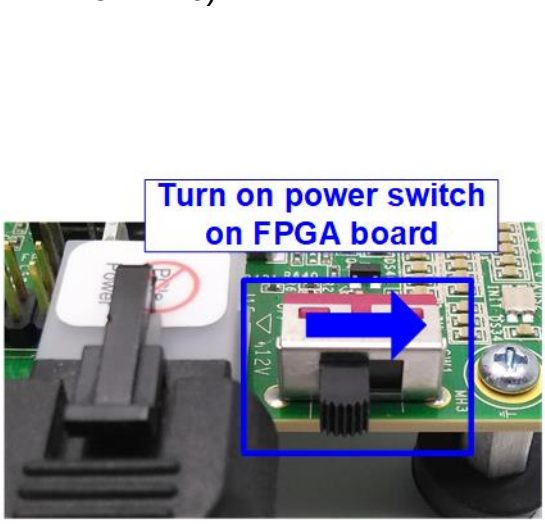


Figure 2-5 USB cable connection

5) Power on FPGA development board, ATX power supply, and adapter board (AB17, AB18, or AB16).



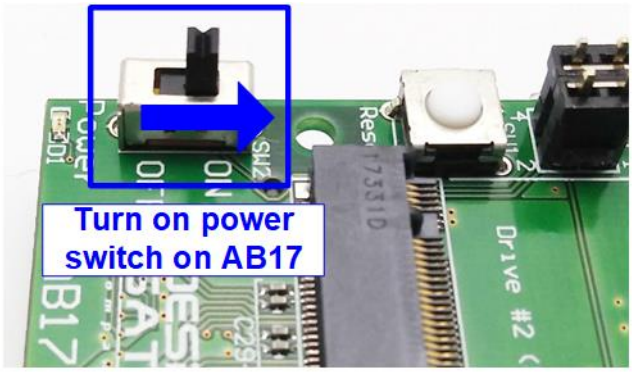


Figure 2-6 Turn on power switch

6) On PC, the additional COM ports are detected after connecting USB cables to FPGA board. Ultrascale/Ultrascale+ board, there are more than one COM ports detected.

   In case of ZCU102, select the lowest number of COM port (COM18 in Figure 2-7).
   In case of KCU105 and VCU118, select Standard COM port (COM11 in Figure 2-7).

   On Serial console, the setting is as follows. Buad rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

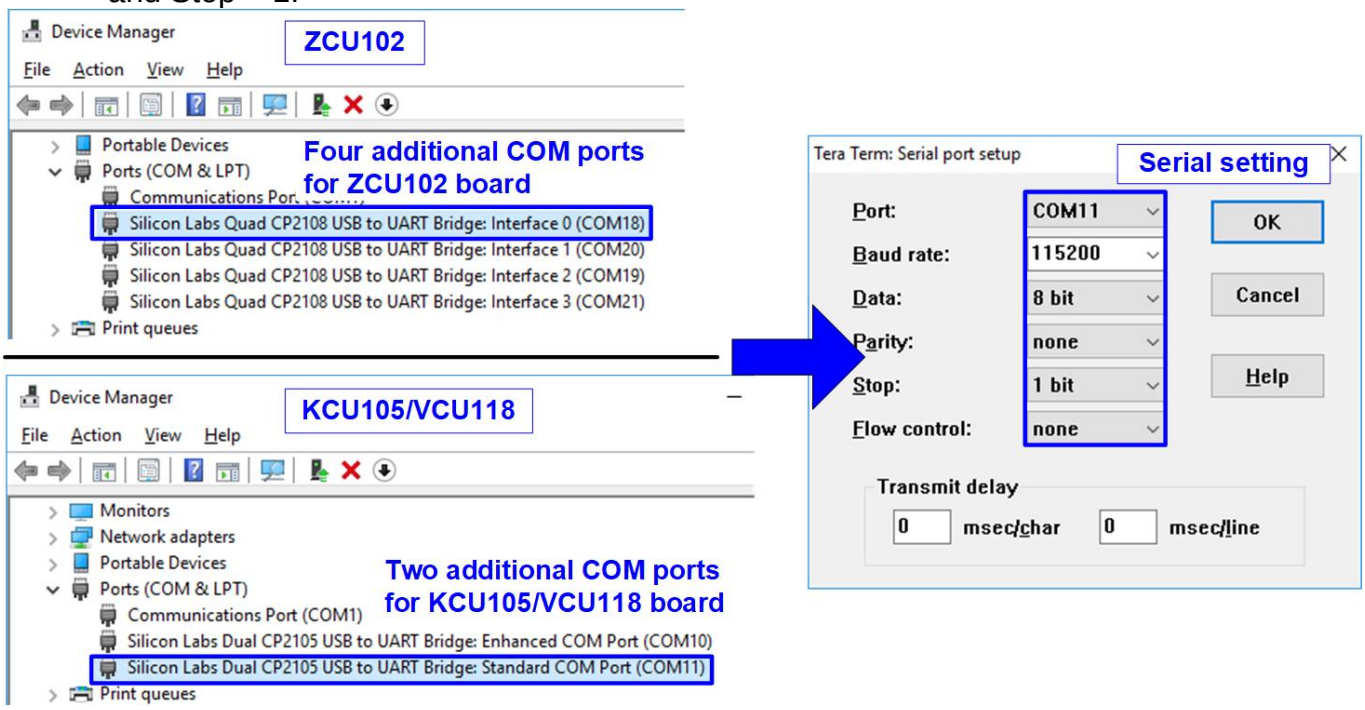


Figure 2-7 Select and set COM port

7) Download and program configuration file and firmware to FPGA board.
   a) For ZCU102, open Vivado TCL shell and change directory to ready_for_download or directory that batch file is located. Next, type NVMeG3IPTest_ZCU102.bat, as shown in Figure 2-8.

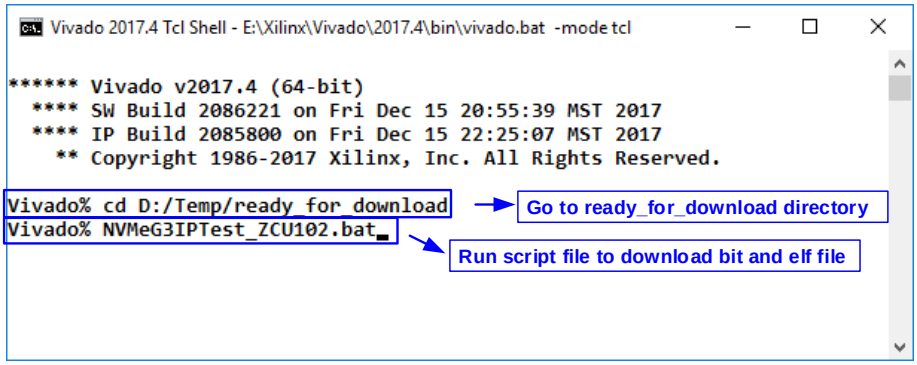


Figure 2-8 Command script to download demo file on Vivado TCL shell

b) For KCU105/VCU118, configure FPGA by using Vivado, as shown in Figure 2-9.

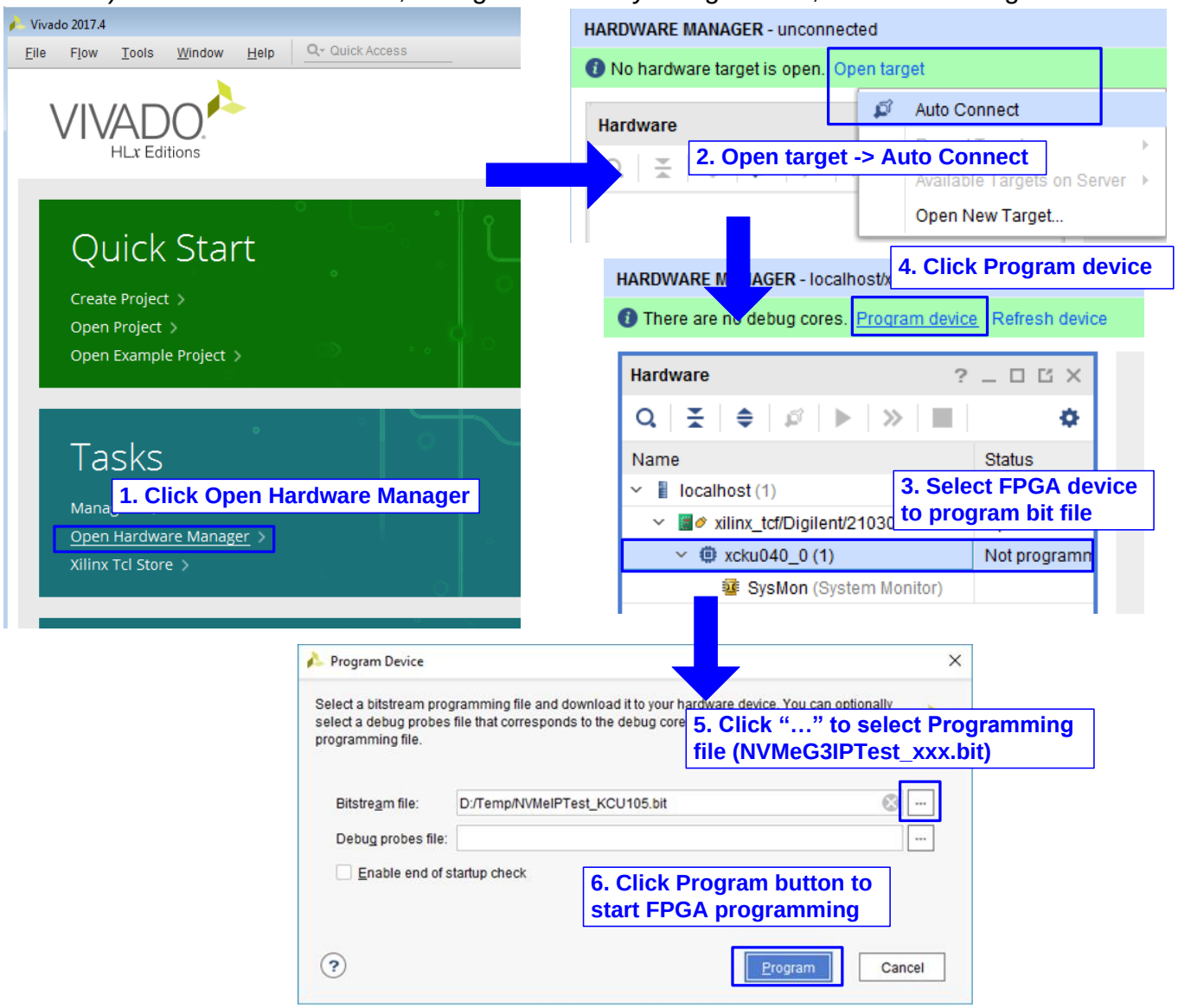


Figure 2-9 LED status after program configuration file and PCIe initialization complete

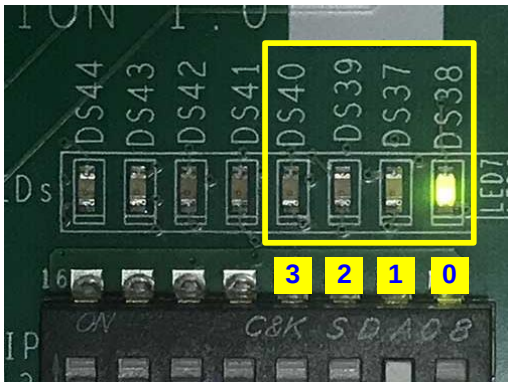
8) Check LED status on FPGA board. The description of LED is as follows.

Table 2-1 LED Definition

GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1	System is busy	Idle status
2	IP Error detect	Normal operation
3	Data verification fail	Normal operation

9) After completely FPGA programming, LED[0] and LED[1] turn on until finishing the initialization process. After that, LED[1] turn-offs.

ZCU102



KCU105/VCU118

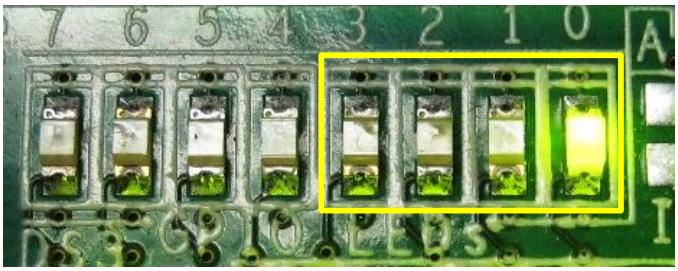


Figure 2-10 LED status after finishing program configuration file and PCIe initialization

10) On the console, the message is displayed to show current status as follows.
- "Waiting IP initialization" is displayed.
- After finishing IP initialization, Main menu is shown on the console as shown in Figure 2-11.

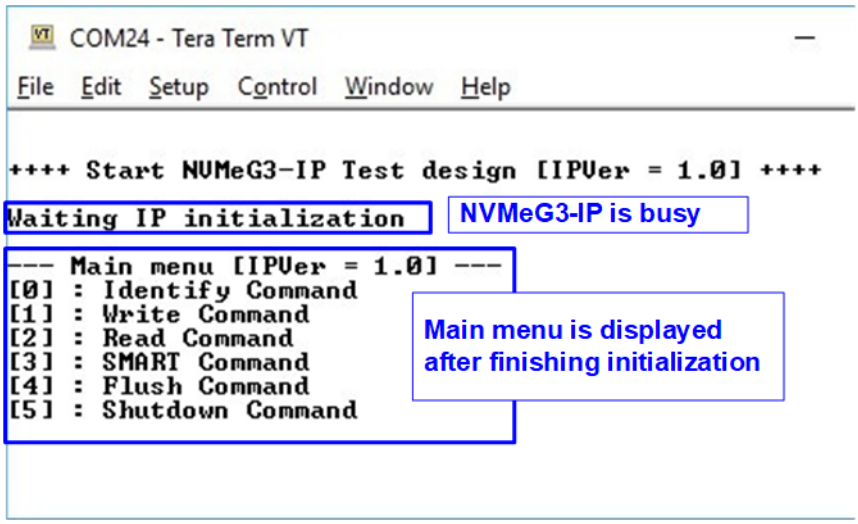


Figure 2-11 Main menu after finishing initialization

3 Test Menu

3.1 Identify Command

Select ‘0’ to send Identify command to NVMe SSD.

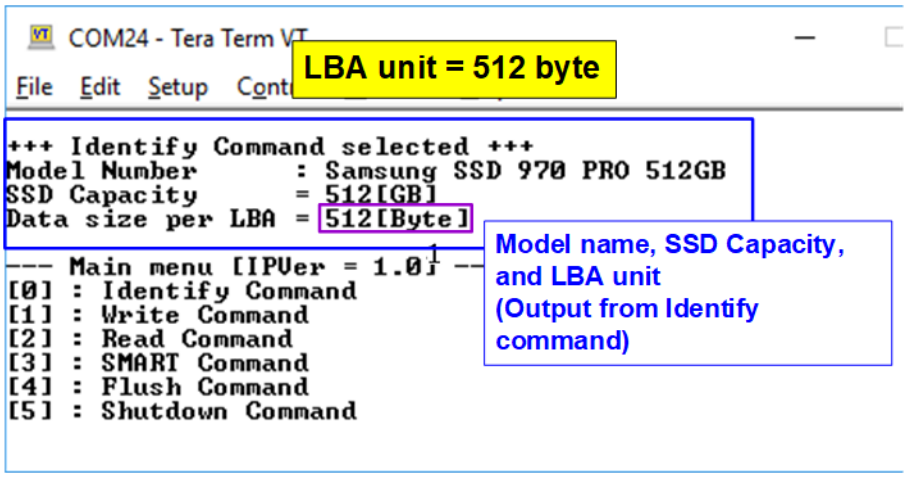


Figure 3-1 Test result when running Identify command

After finishing the operation, the SSD information output from Identify command will be displayed. The console shows three values.

1) SSD model number: This value is decoded from Identify controller data.
2) SSD capacity: This value is signal output from NVMeG3 IP.
3) Data size per LBA: This value is signal output from NVMeG3 IP. Two values are supported, i.e. 512 byte and 4 Kbyte.

3.2 Write Command

Select ‘1’ to send Write command to NVMe SSD.

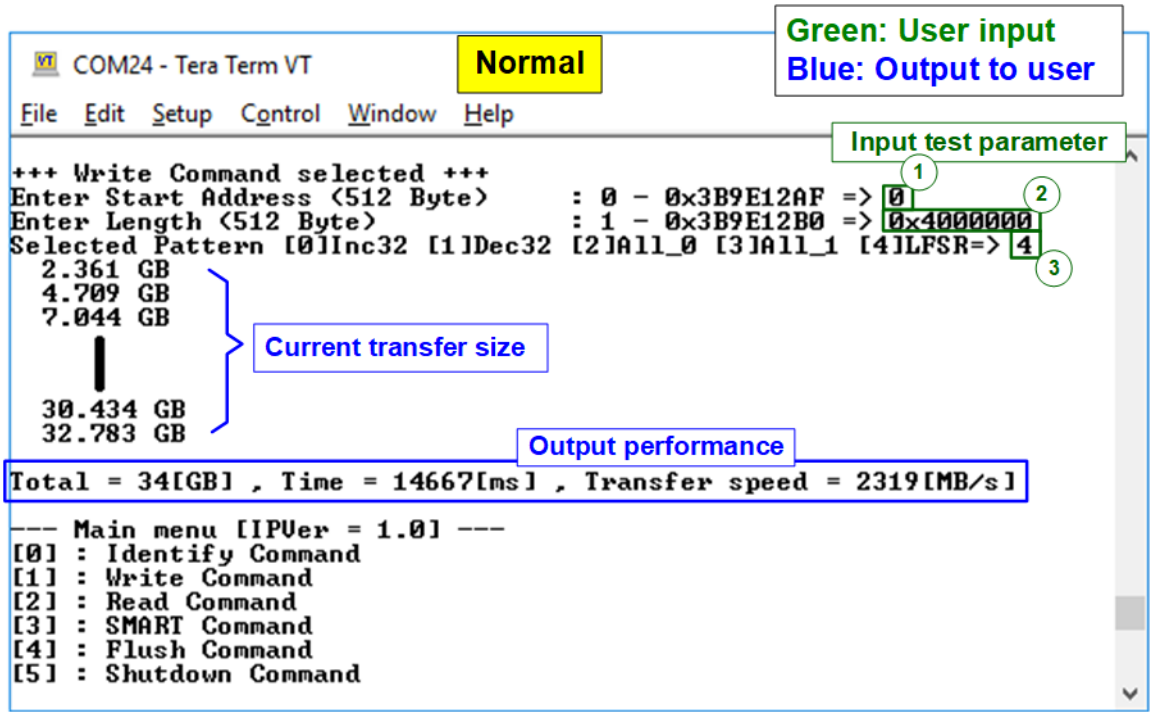


Figure 3-2 Input and test result when running Write command

User inputs three parameters as follows.

1) Start Address: Input start address to write SSD as 512-byte unit. The input is decimal unit when user inputs only digit number. User can add “0x” to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
2) Transfer Length: Input total transfer size as 512-byte unit. The input is decimal unit when user inputs only digit number. User can add “0x” to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
3) Test pattern: Select test data pattern for writing to SSD. There are five patterns, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

After all inputs are valid, the operation begins. During writing data, current transfer size is displayed on the console every second to show that system is still alive. Finally, total size, total time usage, and test speed are displayed on the console after finishing the operation.

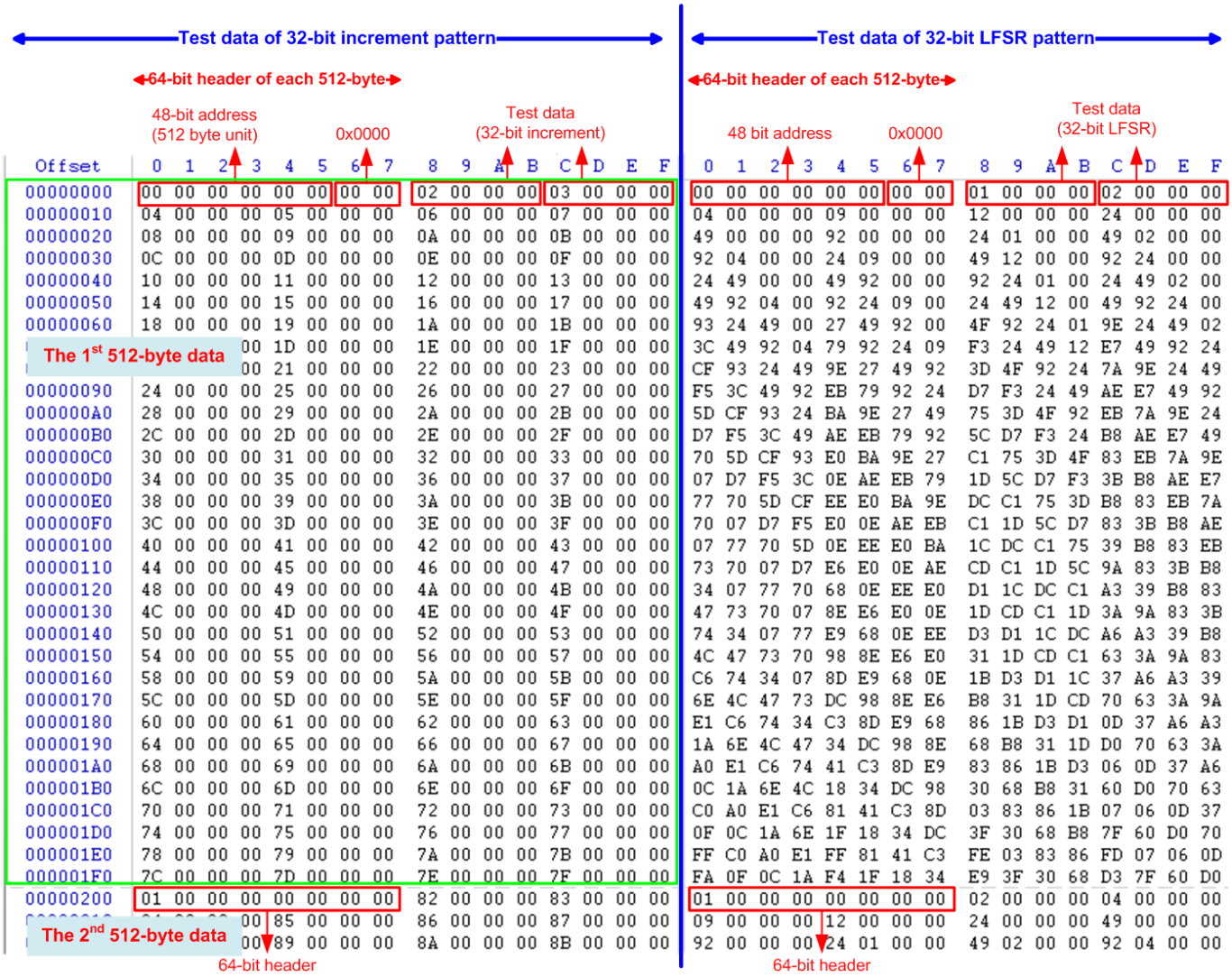


Figure 3-3 Example Test data of the 1st and 2nd 512 byte by using increment/LFSR pattern

Test data in SSD is split into 512-byte unit. For incremental, decremental, or LFSR pettern, each 512-byte data has unique 64-bit header which consists of 48-bit address (in 512-byte unit) and 16-bit zero value. The data after 64-bit header is the test pattern which is selected by user.

The left window of Figure 3-3 shows the example when using 32-bit incremental pattern while the right window shows the example when using 32-bit LFSR pattern.

When user runs Write or Read command with 4-Kbyte LBA SSD, there is the message displaying on the console to show the input limitation which must be aligned to 8 as shown in Figure 3-4. When the input does not align to 8, “Invalid input” is displayed and the operation is cancelled.

Figure 3-5 shows the example when the input is out of the recommended range for each parameter. The console displays “Invalid input” and then the operation is cancelled.

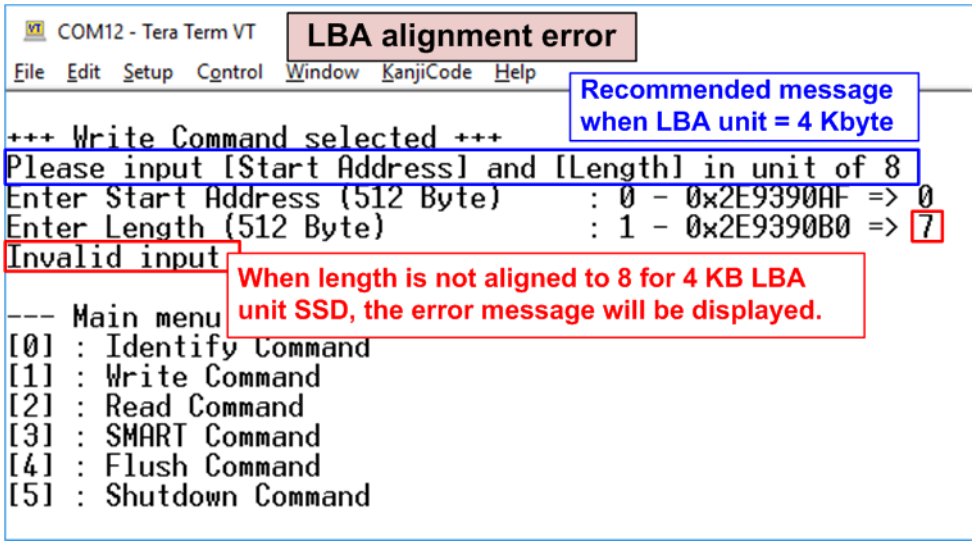


Figure 3-4 Error message when the input is unaligned for 4-Kbyte LBA SSD

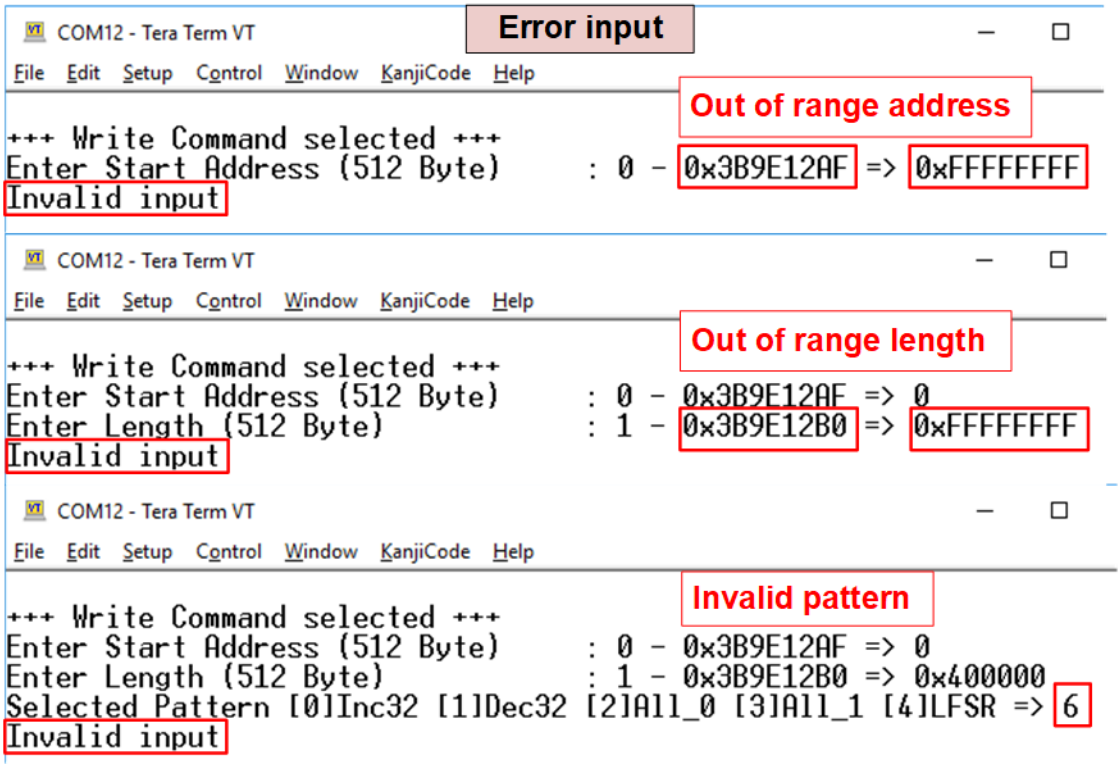


Figure 3-5 Error message from the invalid input

3.3 Read Command

Select ‘2’ to send Read command to NVMe SSD.

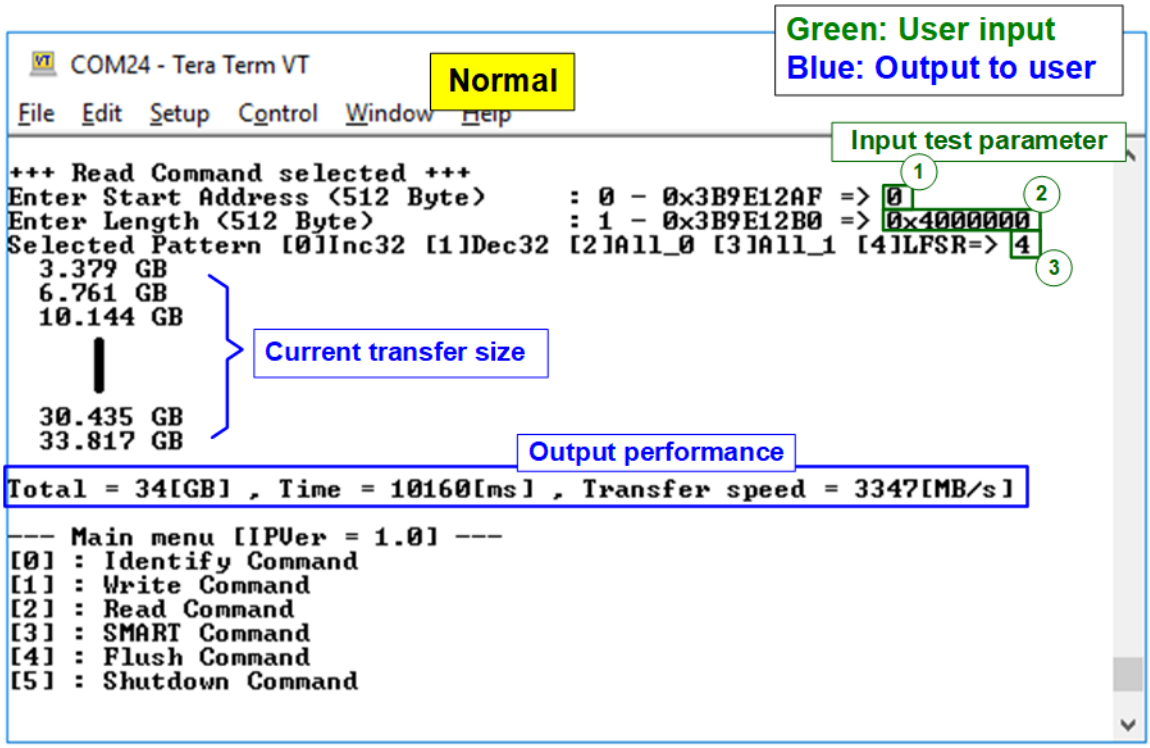


Figure 3-6 Input and test result when running Read Command

User inputs three parameters as follows.

1) Start Address: Input start address to read SSD as 512-byte unit. The input is decimal unit when user inputs only digit number. User can add “0x” to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
2) Transfer Length: Input total transfer size as 512-byte unit. The input is decimal unit when user inputs only digit number. User can add “0x” to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
3) Test pattern: Select test data pattern to verify data from SSD. Test pattern must be matched with the pattern using in Write Command menu. There are five patterns, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter

Similar to Write command menu, test system begins to read data from SSD when all inputs are valid. During reading data, current transfer size is displayed on the console every second to show that system is still alive. Total size, total time usage, and test speed are displayed after finishing the operation.

“Invalid input” is displayed when some inputs are invalid or unaligned to 8 (when connecting to 4-KB LBA SSD).

Figure 3-7 shows error message when data verification is failed. “Verify fail” is displayed with the information of the 1st failure data, i.e. the error byte address, the expected value, and the read value.

User can enter any keys to cancel the read operation or wait until finishing Read command. Similar to the normal condition, the output performance is displayed on the console when the user does not enter any keys to stop the operation.

After enter the key to cancel the operation, the read command operation still runs as the background process. It is recommended to power-off/on AB18/AB16 and then press “RESET” button to recover the error situation.

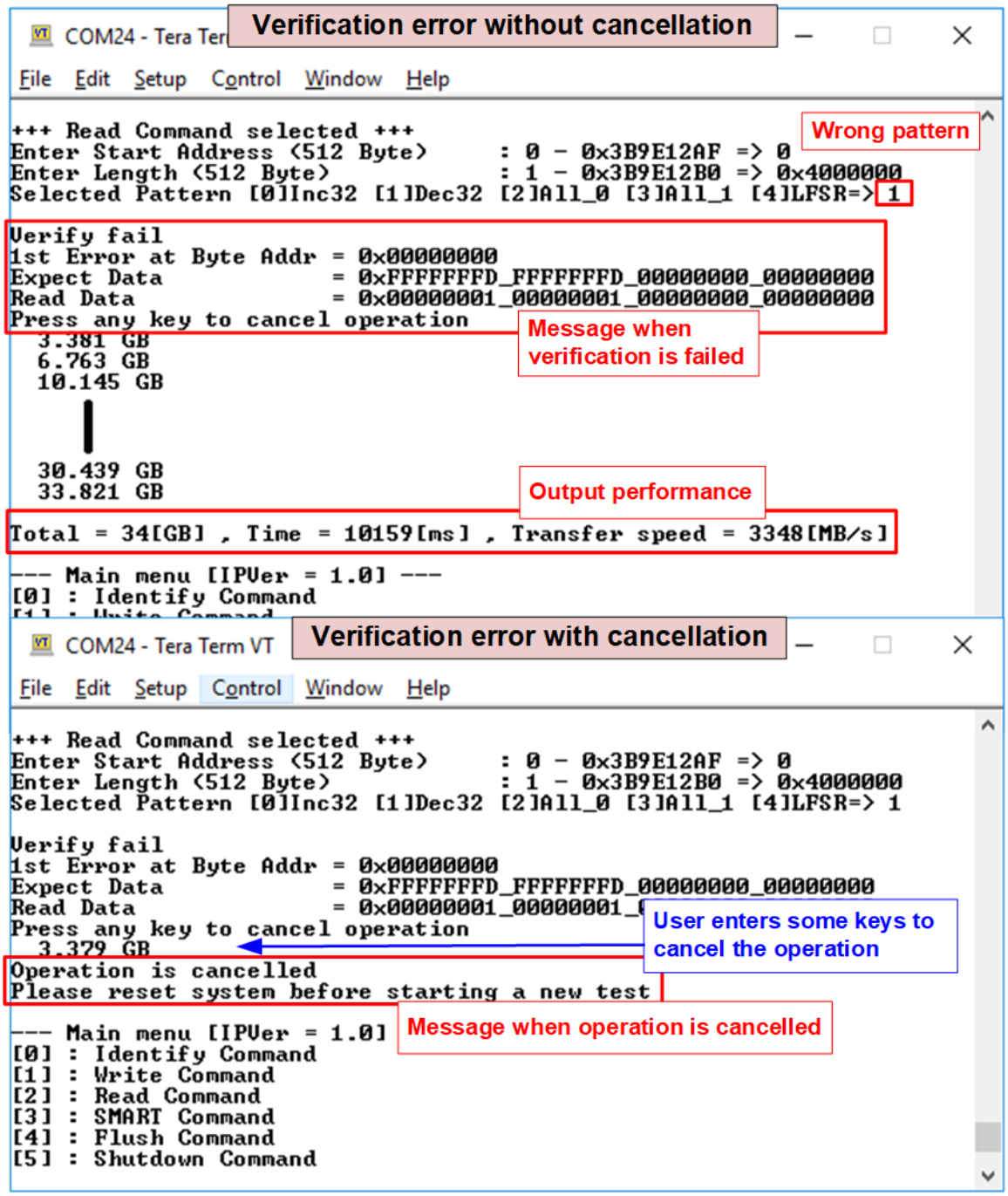


Figure 3-7 Data verification is failed

3.4 SMART Command

Select ‘3’ to send SMART command to NVMe SSD.

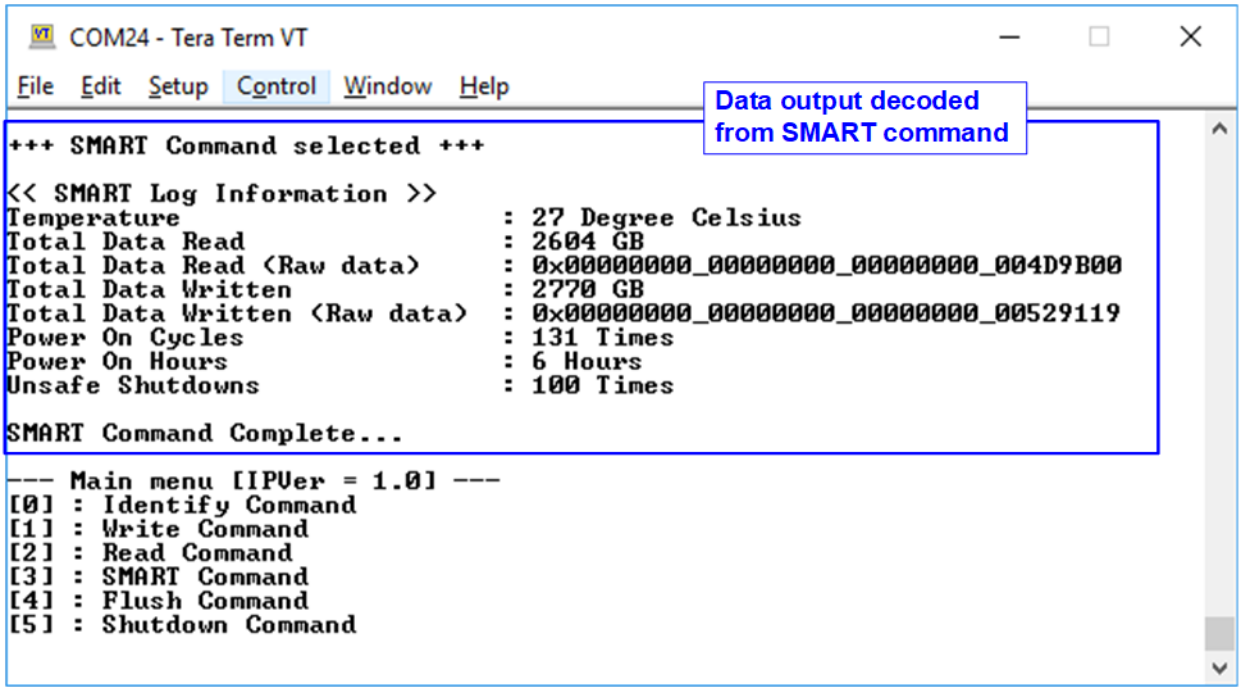


Figure 3-8 Test result when running SMART command

After finishing the operation, SMART/Health Information (output from SMART command) is be displayed as shown in Figure 3-8. The console shows six parameters, described as follows.

1) Temperature in °C unit.
2) Total Data Read decoded as GB/TB unit. Additionally, raw data without decoding is displayed in 128-bit hexadecimal unit. The unit size of raw data is 512,000 Byte.
3) Total Data Written decoded as GB/TB unit. Additionally, raw data without decoding is displayed in 128-bit hexadecimal unit. The unit size of raw data is 512,000 Byte.
4) Power On Cycles: Display the number of power cycles.
5) Power On Hours: Display the period of time in hours to show how long the SSD has been powered on.
6) Unsafe Shutdowns: Display the number of unsafe shutdowns of SSD

3.5 Flush Command

Select ‘4’ to send Flush command to NVMe SSD.

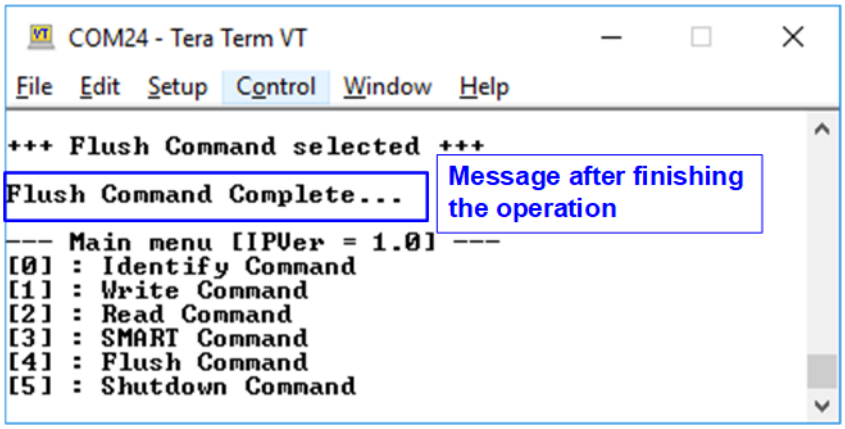


Figure 3-9 Test result when running Flush command

“Flush Command Complete” is displayed after finishing Flush operation.

3.6 Shutdown Command

Select ‘5’ to send Shutdown command to NVMe SSD.

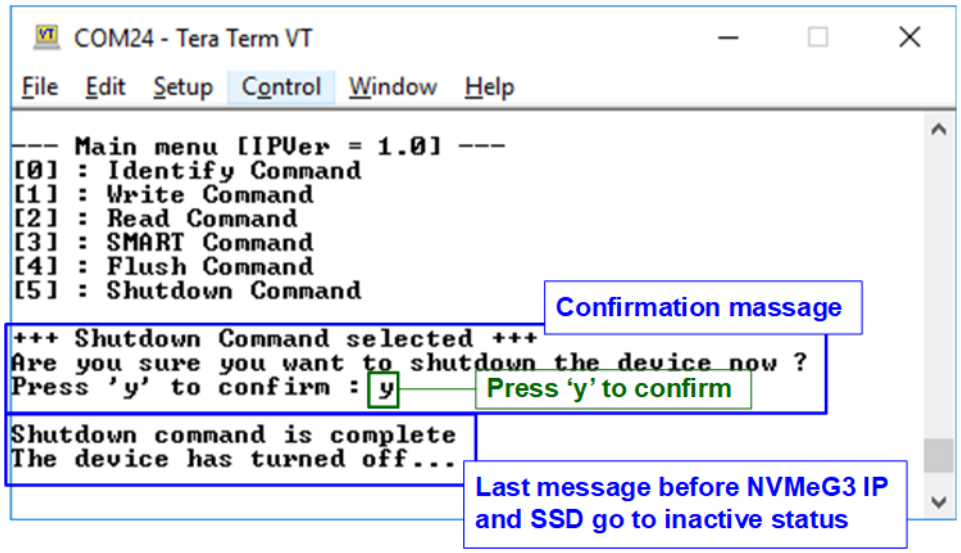


Figure 3-10 Shutdown Command with confirmation

The confirmation message is displayed on the console. User enters ‘y’ or ‘Y’ to continue the operation or enters other keys to cancel the operation.

After finishing Shutdown operation, “Shutdown command is complete” is displayed on the console as the last message. Main menu is not displayed anymore. User needs to power off/on test system to start new test operation.

4 Revision History

Revision	Date	Description
1.0	30-Aug-19	Initial version release
1.1	20-Apr-20	Remove power adapter cable from AB18