

NVMe IP Demo Instruction

Rev3.4 20-Apr-20

This document describes the instruction to run NVMe IP demo on FPGA development board by using the PCIe adapter board (AB18-PCIeX16/AB16-PCIeXOVR adapter board). The demo is designed to write/verify data with NVMe SSD. User controls the test operation through Serial console.

1 Environment Requirement

To run the demo on FPGA development board, please prepare following environment.

- 1) Supported FPGA Development board: ZC706, VC707, KCU105, ZCU106, and VCU118
- 2) PC installing Xilinx programmer software (Vivado) and Serial console software such as HyperTerminal and TeraTerm
- 3) The PCIe adapter board (AB18-PCIeX16/AB16-PCIeXOVR adapter board) provided by Design Gateway
https://dgway.com/ABseries_E.html
- 4) Xilinx power adapter for FPGA board
- 5) ATX power supply for PCIe adapter board
- 6) NVMe SSD connecting to B side (Device) of PCIe adapter board
- 7) One micro USB cable for programming FPGA, connecting between FPGA board and PC
- 8) One mini/micro USB cable for Serial console, connecting between FPGA board and PC

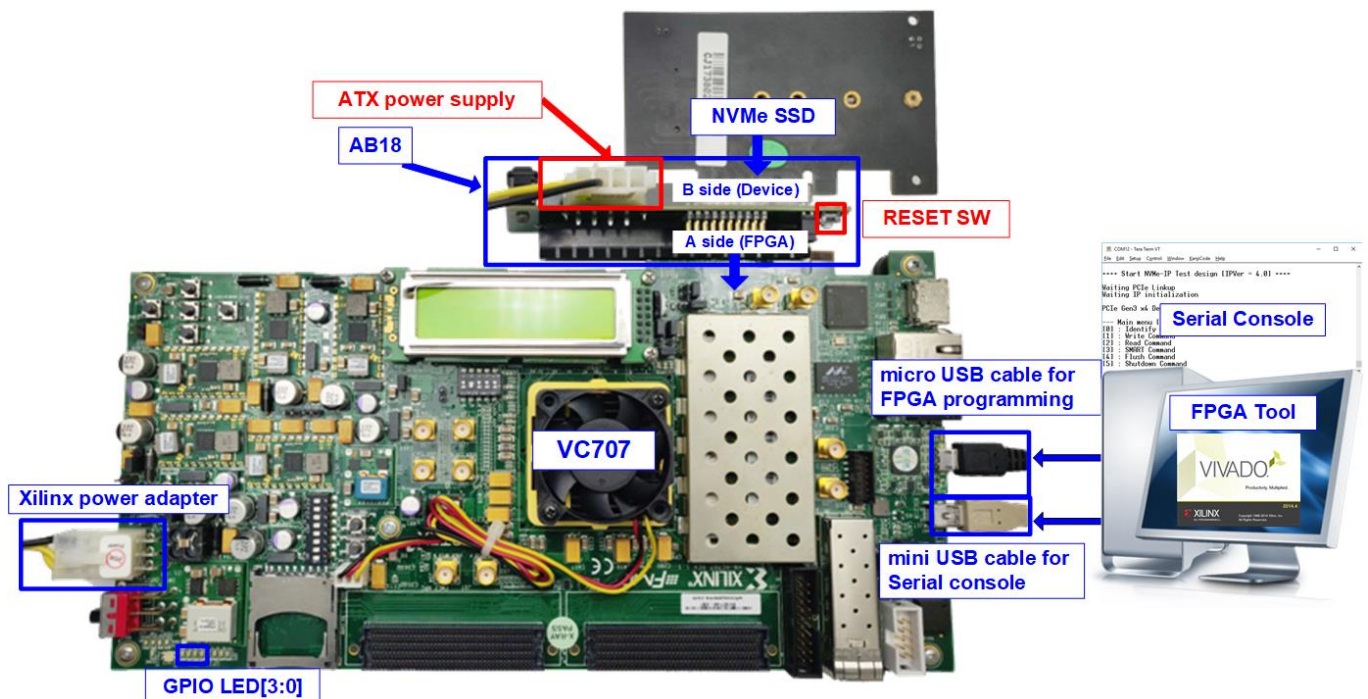


Figure 1-1 NVMe IP demo environment setup on VC707 (PCIe Gen2)

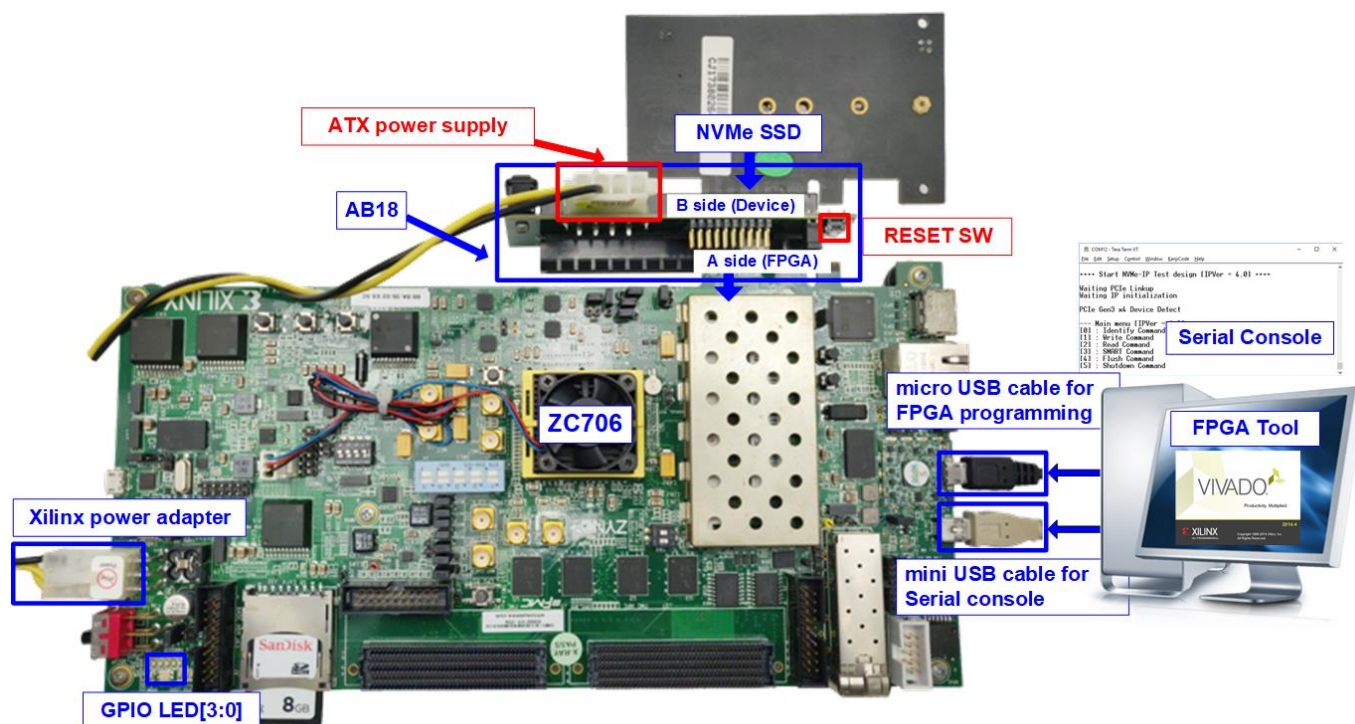


Figure 1-2 NVMe IP demo environment setup on ZC706 (PCIe Gen2)

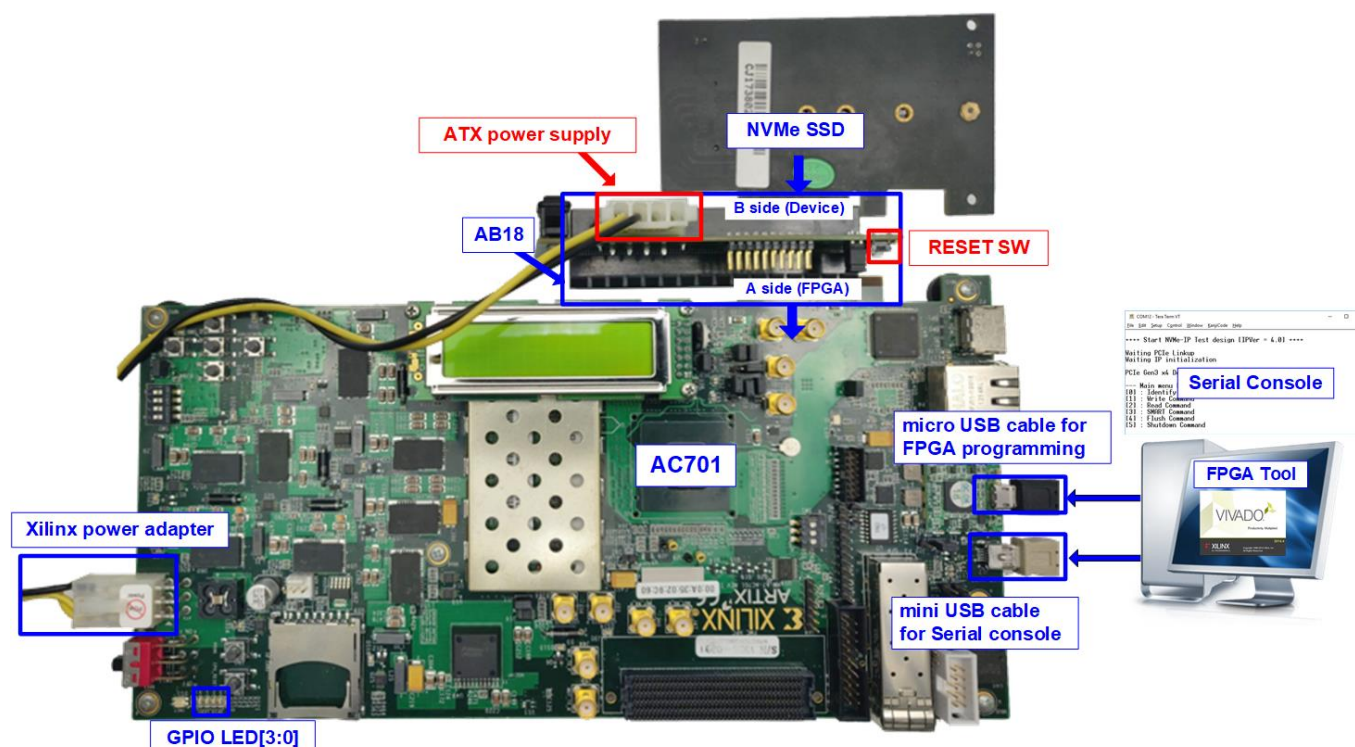


Figure 1-3 NVMe IP demo environment setup on AC701 (PCIe Gen2)

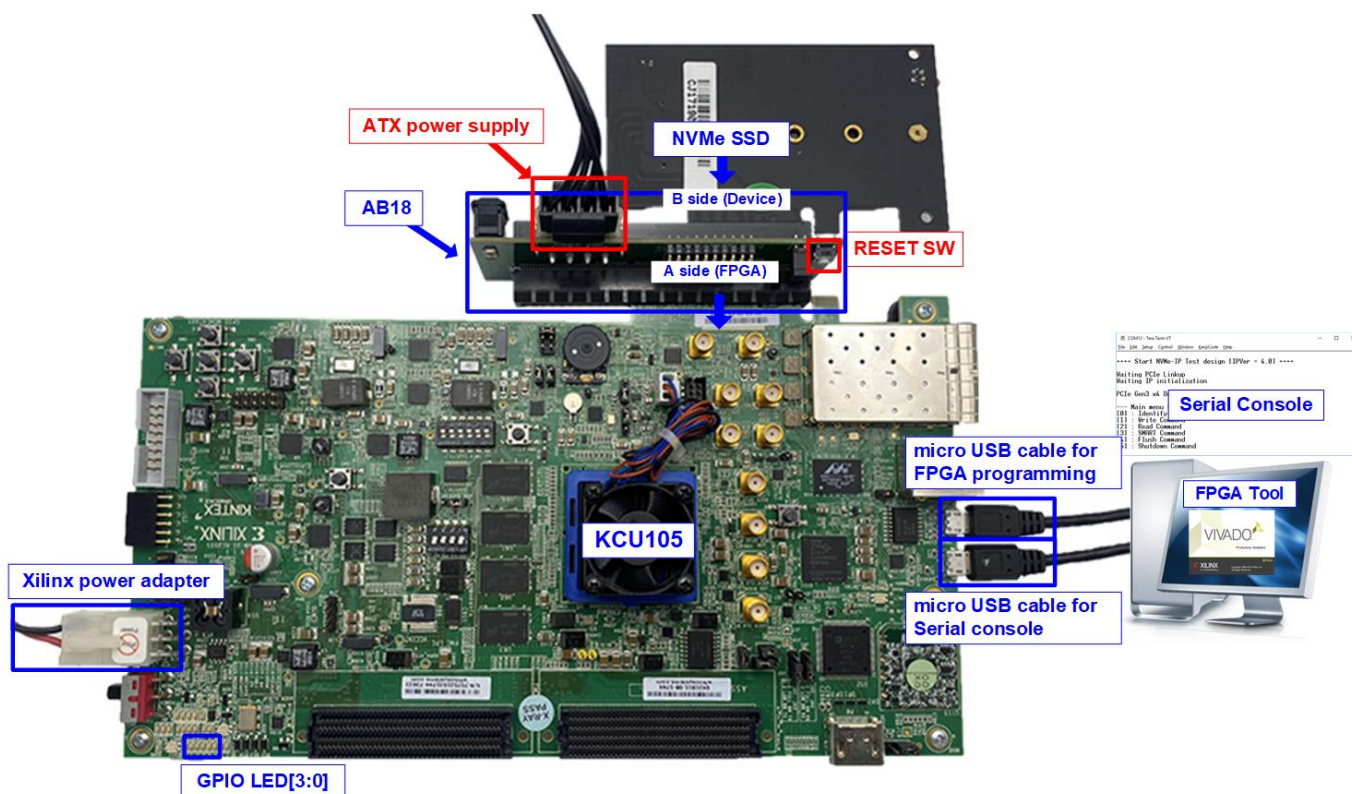


Figure 1-4 NVMe IP demo environment setup on KCU105 (PCIe Gen3)

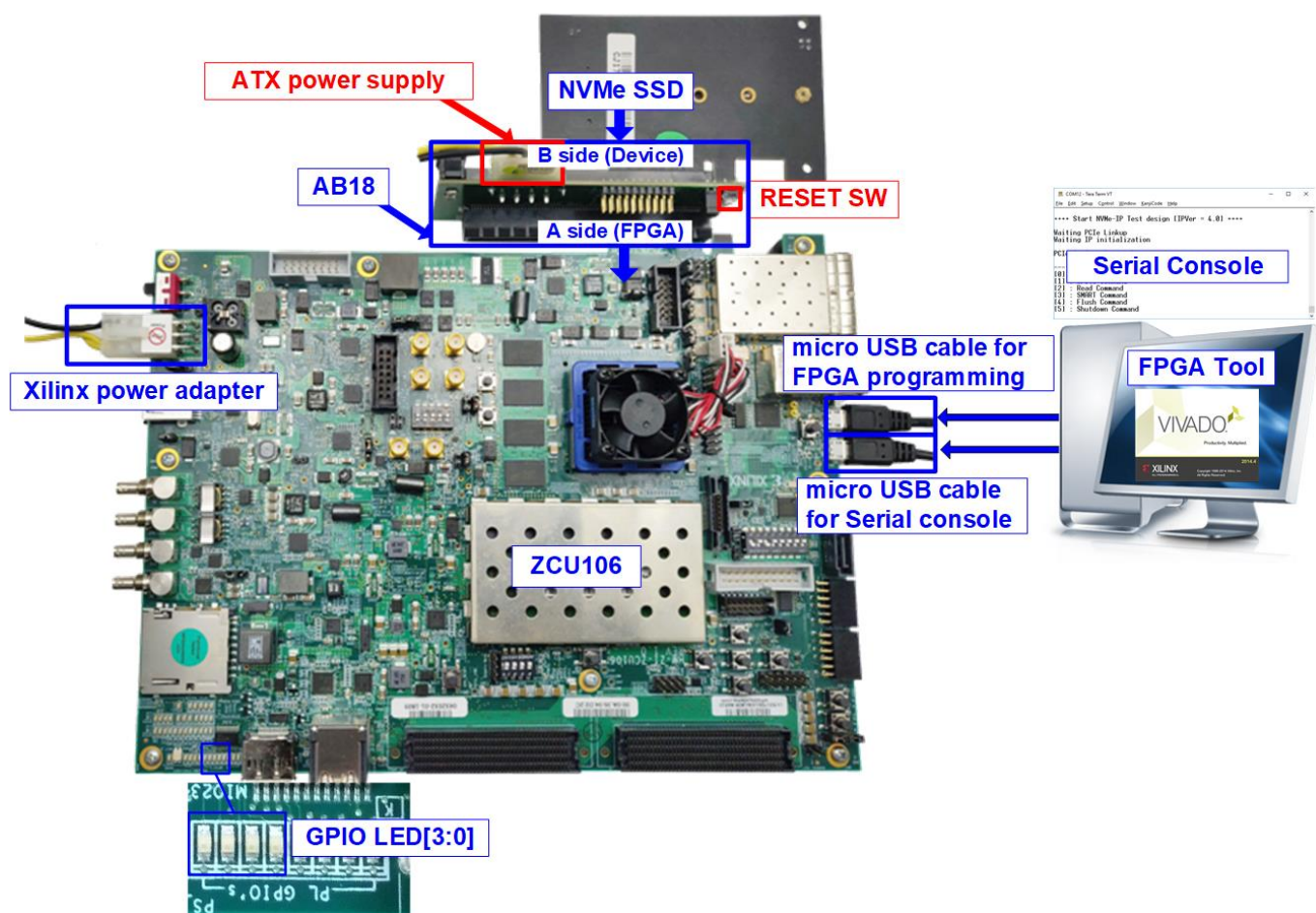


Figure 1-5 NVMe IP demo environment setup on ZCU106 (PCIe Gen3)

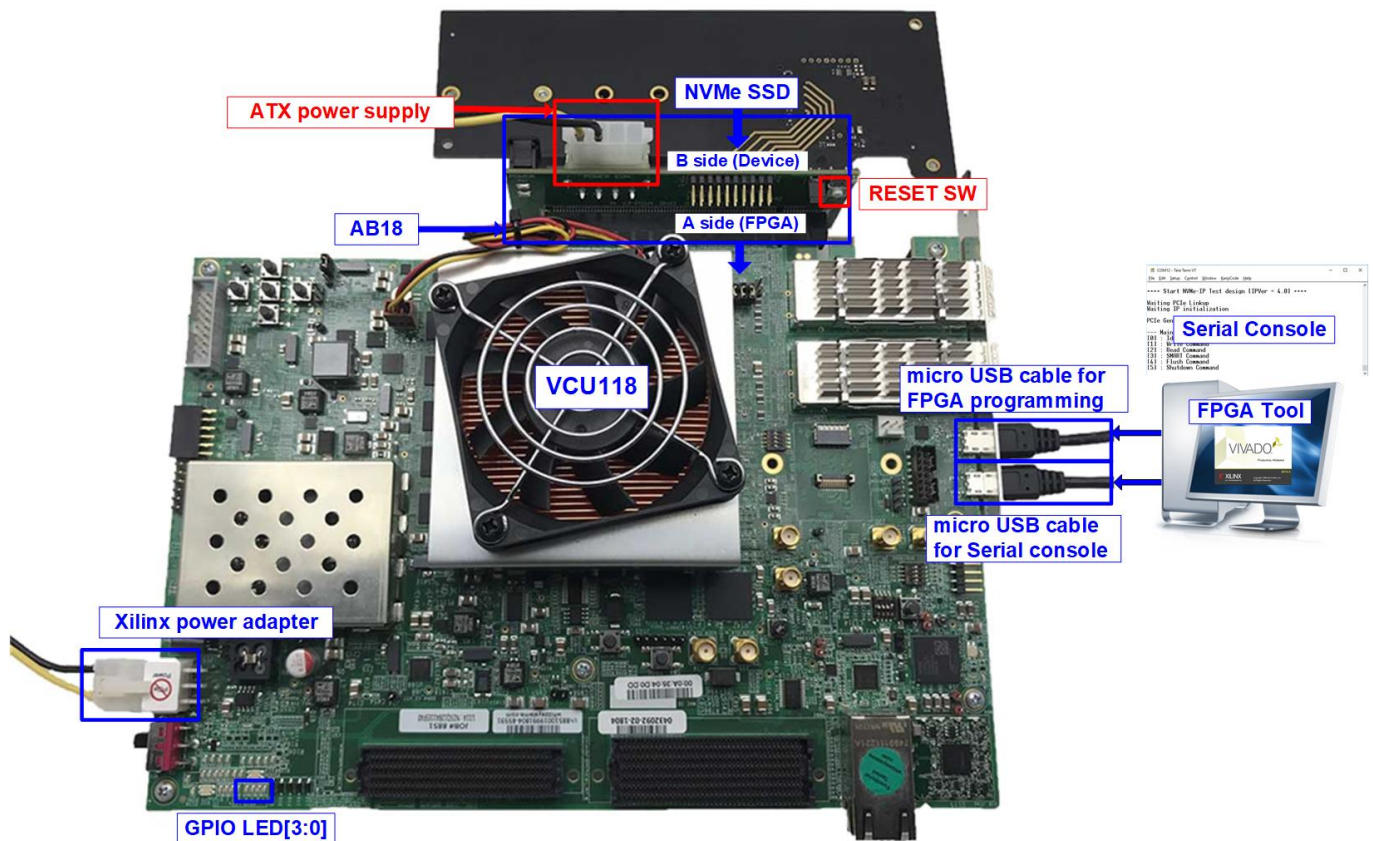


Figure 1-6 NVMe IP demo environment setup on VCU118 (PCIe Gen3)

2 Demo setup

- 1) Power off system.
- 2) DIP Switch setting for JTAG configuration on Zynq board.
 - a) For ZC706 board, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 2-1.

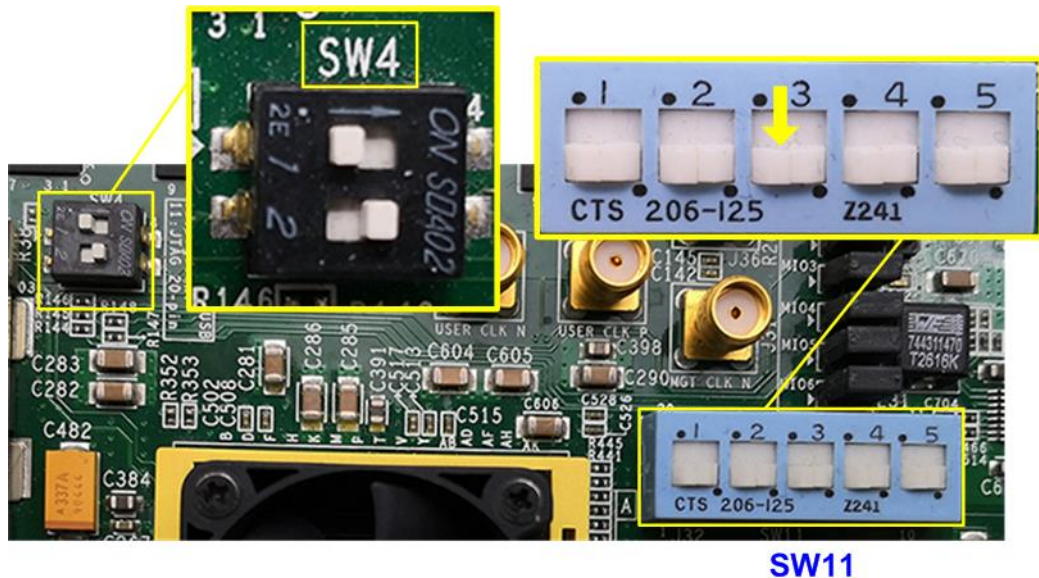


Figure 2-1 SW11 setting to configure PS from JTAG on ZC706

- b) For ZCU106 board, set SW6=all ON to configure PS from JTAG, as shown in Figure 2-2.

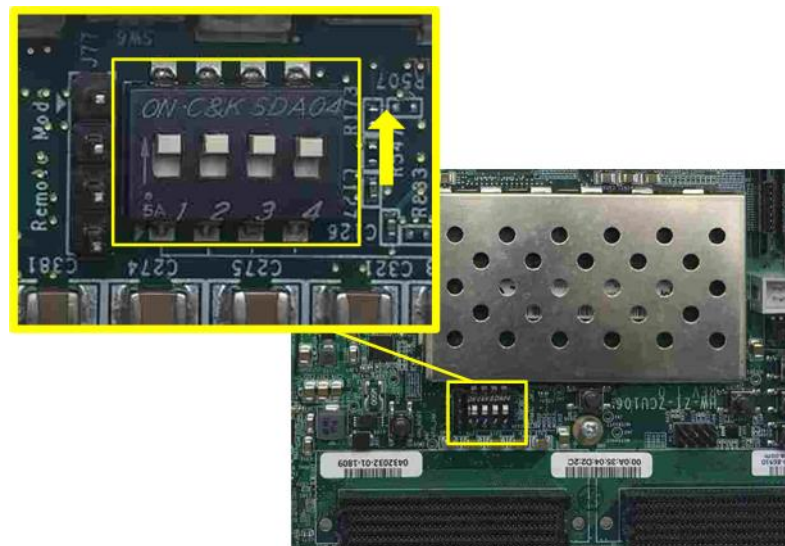


Figure 2-2 SW6 setting to configure PS from JTAG on ZCU106

- 3) Connect ATX power supply to AB18-PCIeX16 board and Xilinx power adapter to FPGA development board.

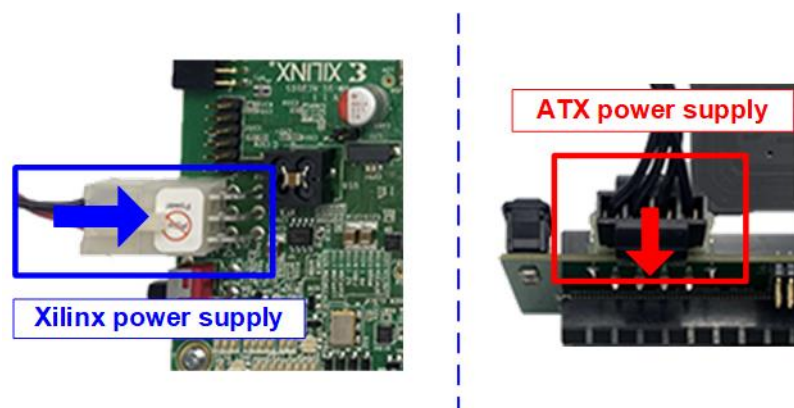


Figure 2-3 Power supply connection

- 4) Confirm that two mini jumpers are inserted at J5 connector on AB18. After that, connect FPGA Side (A-side) on AB18 to PCIe connector on FPGA board and connect NVMe PCIe SSD to device side (B-Side) on AB18, as shown in Figure 2-4.

Warning: Please confirm that the SSD is inserted in the correct side of AB18 (B-side, not A-side) before power on system.

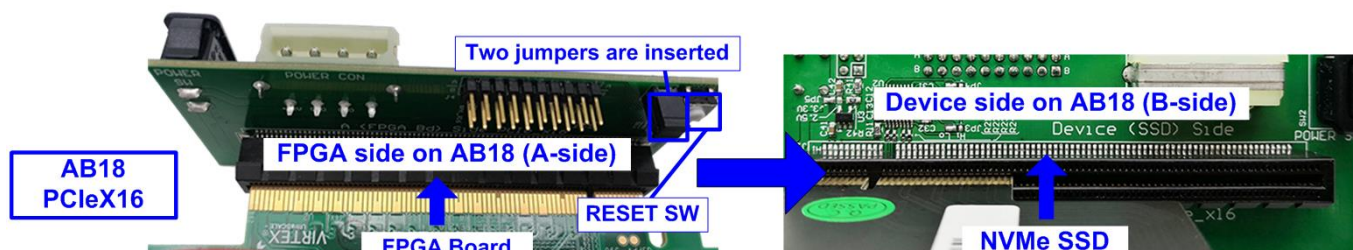


Figure 2-4 Connect Adapter board to NVMe SSD and FPGA board

- 5) Connect USB cables for JTAG programming and Serial console.
 - a) For AC701/VC707/ZC706, connect micro USB for JTAG and mini USB cable for Serial console.
 - b) For KCU105/ZCU106/VCU118, connect two micro USB cables for JTAG and Serial console.

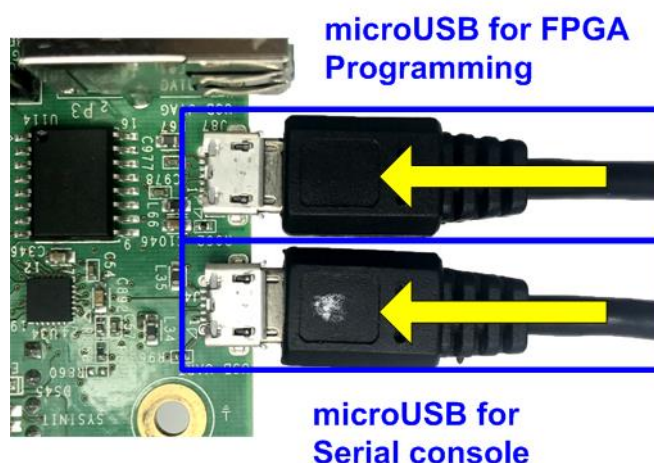


Figure 2-5 USB cable connection

- 6) Power on FPGA development board, ATX power supply, and AB18, as shown in Figure 2-6.

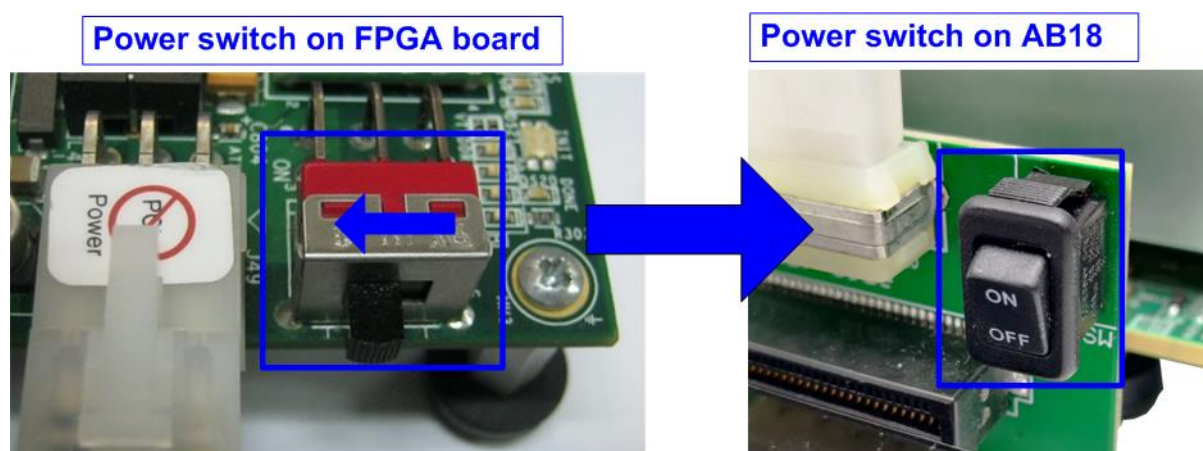


Figure 2-6 Turn on power switch on FPGA and adapter board

- 7) On PC, additional COM port is detected after connecting USB cables to FPGA board. On Ultrascale/Ultrascale+ board, there are more than one COM ports detected.

In case of KCU105 and VCU118, select Standard COM port.

In case of ZCU106, select the lowest number for ZCU106 board, as shown in Figure 2-7.

On Serial console, the setting is as follows. Baud rate=115,200, Data=8-bit, Non-Parity, and Stop = 1.

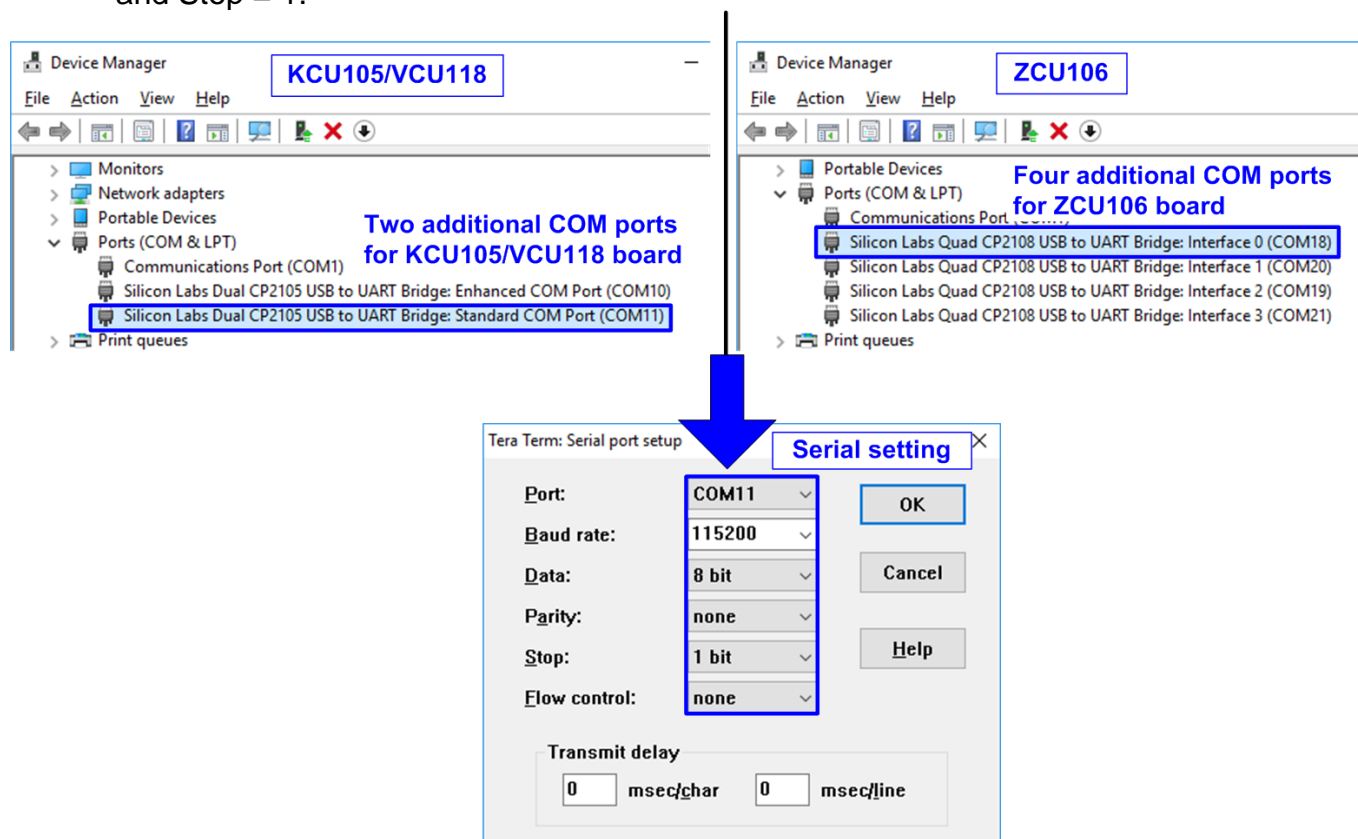


Figure 2-7 Select and set COM port

- 8) Download and program configuration file and firmware to FPGA board.
- a) For AC701/VC707/KCU105/VCU118, configure FPGA by using Vivado, as shown in Figure 2-8.

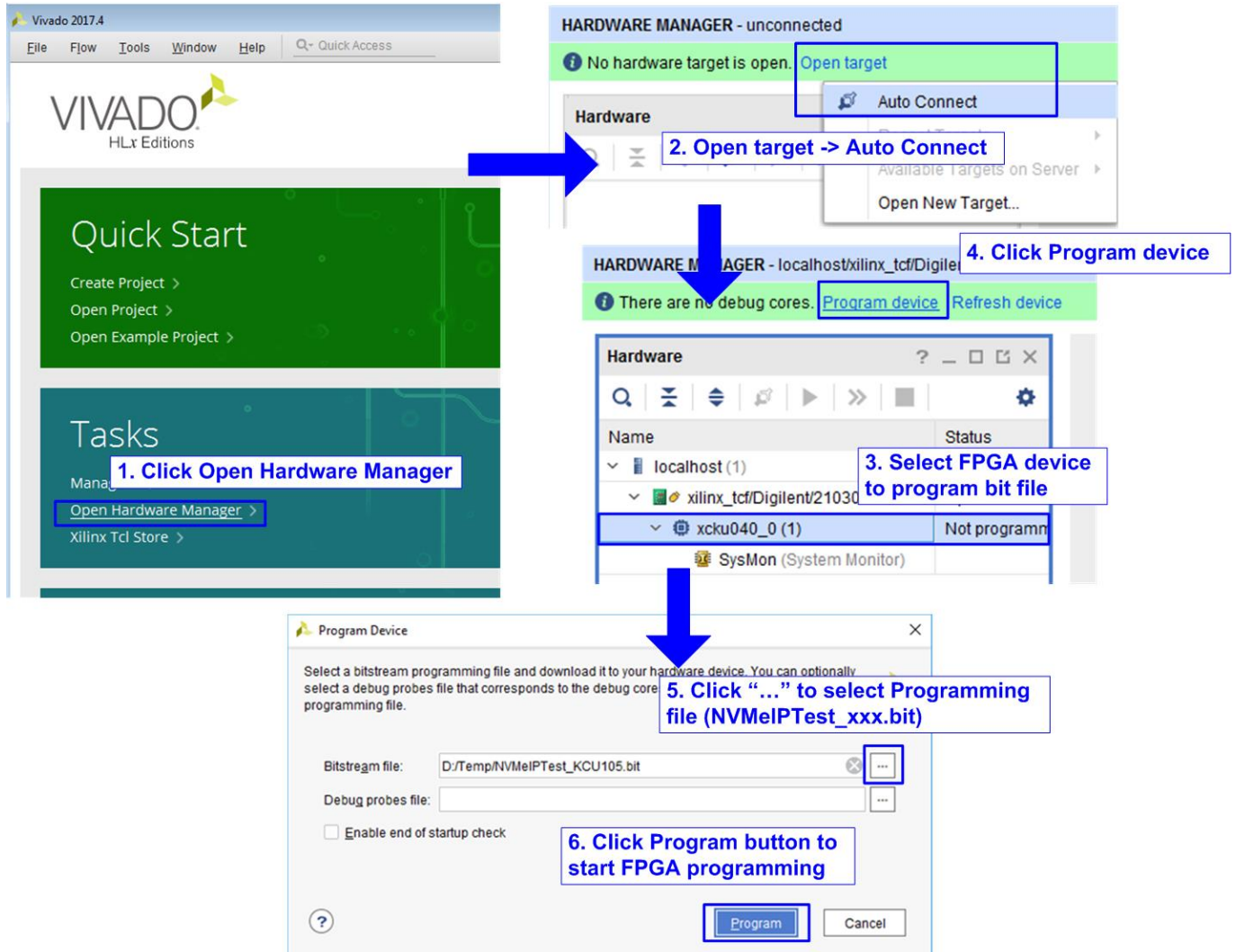


Figure 2-8 Program FPGA by Vivado

- b) For ZC706/ZCU106 board, open Vivado TCL shell and change directory to ready_for_download or directory that batch file is located. Next, type zc706_NVMeIPTest.bat or zcu106_NVMeIPTest.bat, as shown in Figure 2-9.

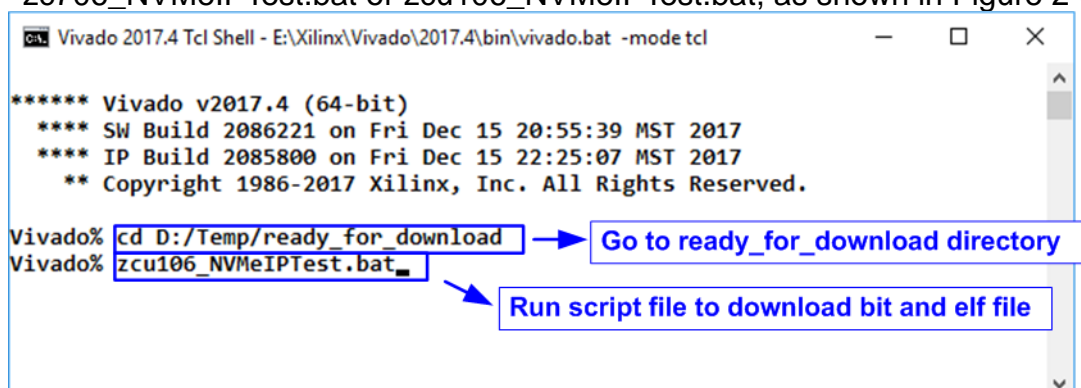


Figure 2-9 Command script to download demo file on Vivado TCL shell

9) Check LED status on FPGA board. The description of LED is as follows.

Table 2-1 LED Definition

GPIO LED	ON	OFF
0	Normal operation	Clock is not locked or reset button is pressed
1/R	System is busy	Idle status
2/C	IP Error detect	Normal operation
3/L	Data verification fail	Normal operation

10) After programming completely, LED[0] and LED[1] are ON during PCIe initialization process. Then, LED[1] changes to OFF after PCIe completes initialization process.

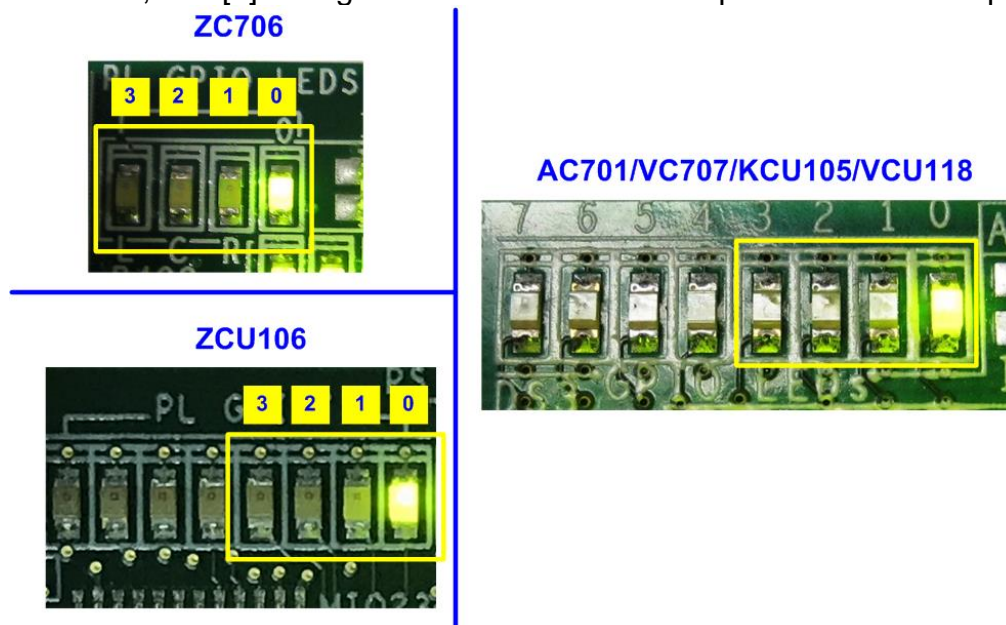
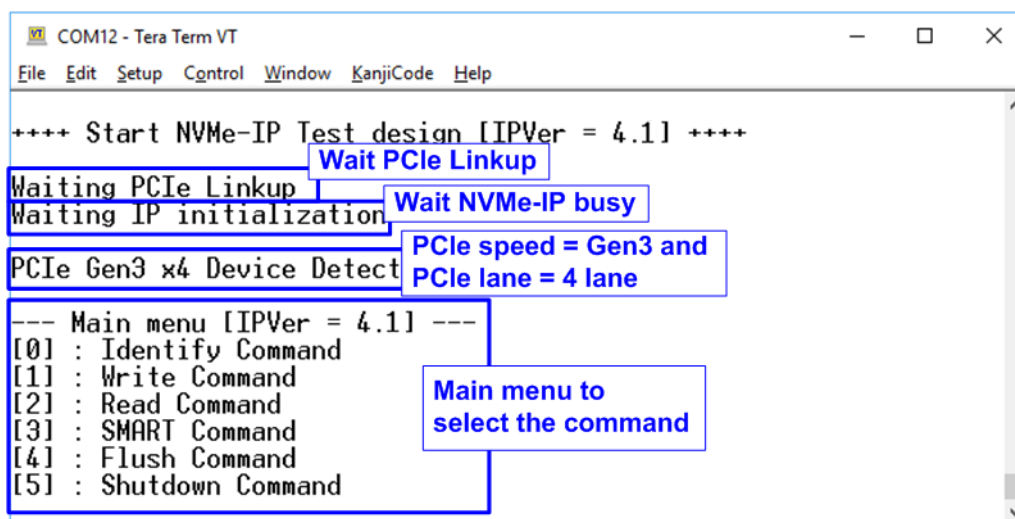


Figure 2-10 LED status after program configuration file and PCIe initialization complete

- 11) On the console, the message is displayed to show current status as follows.
 “Waiting PCIe Linkup” is displayed after finishing configuration.
 After PCIe is linkup, “Waiting IP initialization” is displayed.
 After finishing NVMe IP initialization, PCIe speed and number of PCIe lanes are displayed. Finally, main menu to run six commands is shown on the console.



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

++++ Start NVMe-IP Test design [IPVer = 4.1] ++++
Waiting PCIe Linkup
Waiting IP initialization
PCIe Gen3 x4 Device Detect
Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command
  
```

Figure 2-11 Main menu after IP finishes initialization

3 Test Menu

3.1 Identify Command

Select '0' to send Identify command to NVMe SSD.

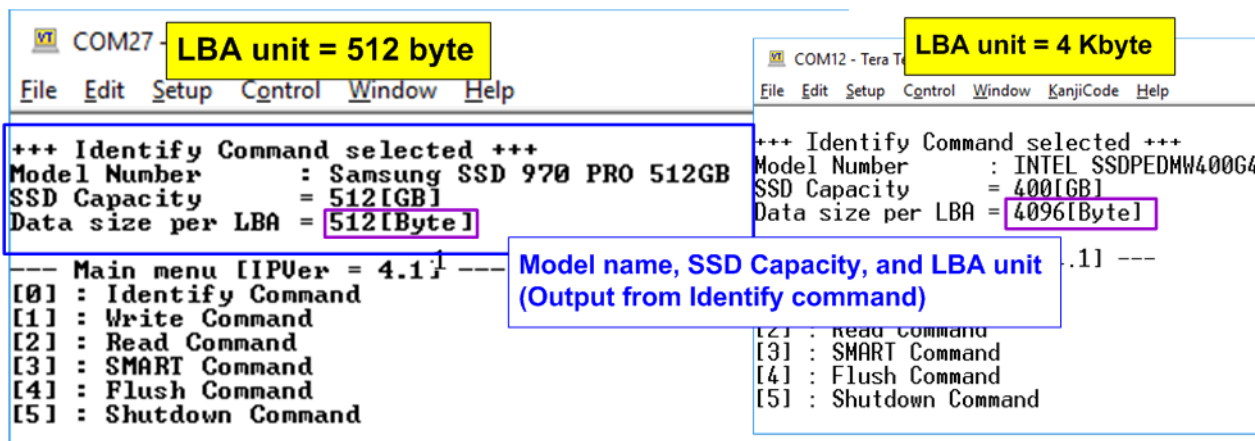


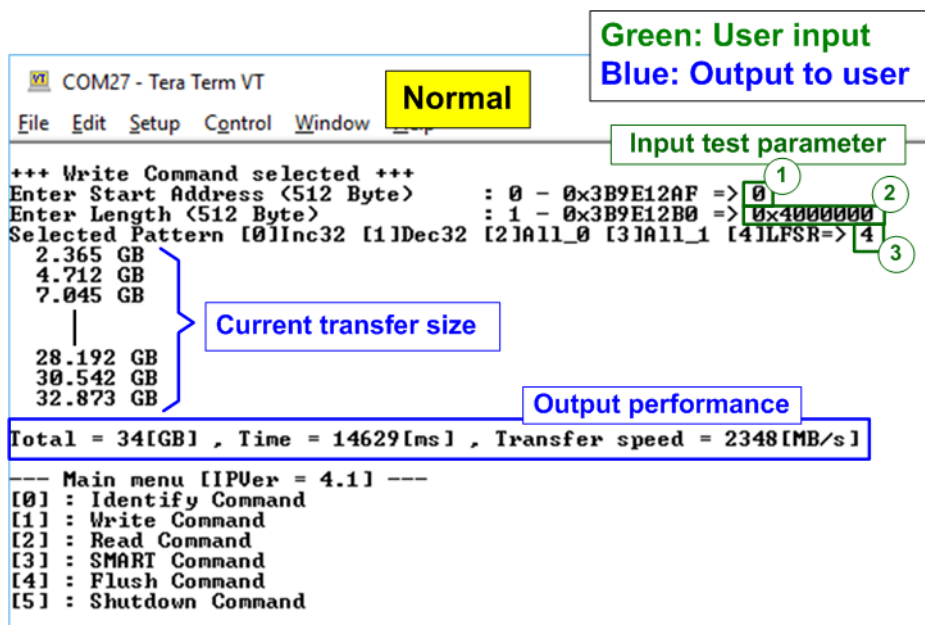
Figure 3-1 Test result when running Identify command

After finishing the operation, the SSD information output from Identify command is displayed. The console shows three values.

- 1) SSD model number: This value is decoded from Identify controller data.
- 2) SSD capacity: This value is signal output from NVMe-IP.
- 3) Data size per LBA: This value is signal output from NVMe-IP. Two values are supported, i.e. 512 byte and 4 Kbyte.

3.2 Write Command

Select '1' to send Write command to NVMe SSD.



```

COM27 - Tera Term VT
File Edit Setup Control Window
Normal

+++ Write Command selected +++
Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0
Enter Length (512 Byte) : 1 - 0x3B9E12B0 => 0x40000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 4

2.365 GB
4.712 GB
7.045 GB
|
28.192 GB
30.542 GB
32.873 GB

Total = 34[GB] , Time = 14629[ms] , Transfer speed = 2348[MB/s]

--- Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command
  
```

Green: User input
Blue: Output to user

Input test parameter

Current transfer size

Output performance

Figure 3-2 Test result when running Write command

User inputs three parameters as follows.

- 1) Start Address: Input start address to write SSD as 512-byte unit. The input is decimal unit when user enters only digit number. User can add "0x" to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
- 2) Transfer Length: Input total transfer size as 512-byte unit. The input is decimal unit when user enters only digit number. User can add "0x" to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
- 3) Test pattern: Select test data pattern for writing to SSD. There are five patterns, i.e. 32-bit incremental, 32-bit decremental, all-0, all-1, and 32-bit LFSR counter.

When all inputs are valid, the operation begins. During writing data, current transfer size is displayed on the console every second to show that system is still alive. Finally, total size, total time usage, and test speed are displayed on the console to be a test result.

Test data of 32-bit increment pattern																Test data of 32-bit LFSR pattern																			
←64-bit header of each 512-byte→																←64-bit header of each 512-byte→																			
		48-bit address (512 byte unit)								Test data (32-bit increment)										48 bit address								Test data (32-bit LFSR)							
Offset	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F			
00000000	00	00	00	00	00	00	00	00	02	00	00	00	03	00	00	00	00	00	00	00	00	00	00	00	01	00	00	00	02	00	00	00			
00000010	04	00	00	00	05	00	00	00	06	00	00	00	07	00	00	00	04	00	00	00	09	00	00	00	12	00	00	00	24	00	00	00			
00000020	08	00	00	00	09	00	00	00	0A	00	00	00	0B	00	00	00	49	00	00	00	92	00	00	00	24	01	00	00	49	02	00	00			
00000030	0C	00	00	00	0D	00	00	00	0E	00	00	00	0F	00	00	00	92	04	00	00	24	09	00	00	49	12	00	00	92	24	00	00			
00000040	10	00	00	00	11	00	00	00	12	00	00	00	13	00	00	00	24	49	00	00	49	92	00	00	92	24	01	00	24	49	02	00			
00000050	14	00	00	00	15	00	00	00	16	00	00	00	17	00	00	00	49	92	04	00	92	24	09	00	24	49	12	00	49	92	24	00			
00000060	18	00	00	00	19	00	00	00	1A	00	00	00	1B	00	00	00	93	24	49	00	27	49	92	00	4F	92	24	01	9E	24	49	02			
The 1 st 512-byte data																																			
00000090	24	00	00	00	25	00	00	00	26	00	00	00	27	00	00	00	CF	93	24	49	9E	27	49	92	3D	4F	92	24	7A	9E	24	49			
000000A0	28	00	00	00	29	00	00	00	2A	00	00	00	2B	00	00	00	5D	CF	93	24	BA	9E	27	49	75	3D	4F	92	EB	7A	9E	24			
000000B0	2C	00	00	00	2D	00	00	00	2E	00	00	00	2F	00	00	00	D7	F5	3C	49	AE	EB	79	92	5C	D7	F3	24	B8	AE	E7	49			
000000C0	30	00	00	00	31	00	00	00	32	00	00	00	33	00	00	00	70	5D	CF	93	E0	BA	9E	27	C1	75	3D	4F	83	EB	7A	9E			
000000D0	34	00	00	00	35	00	00	00	36	00	00	00	37	00	00	00	07	D7	F5	3C	0E	AE	EB	79	1D	5C	D7	F3	3B	B8	AE	E7			
000000E0	38	00	00	00	39	00	00	00	3A	00	00	00	3B	00	00	00	77	70	5D	CF	EE	E0	BA	9E	DC	C1	75	3D	B8	83	EB	7A			
000000F0	3C	00	00	00	3D	00	00	00	3E	00	00	00	3F	00	00	00	70	07	D7	F5	E0	0E	AE	EB	C1	1D	5C	D7	83	3B	B8	AE			
00000100	40	00	00	00	41	00	00	00	42	00	00	00	43	00	00	00	07	77	70	5D	0E	EE	E0	BA	1C	DC	C1	75	39	B8	83	EB			
00000110	44	00	00	00	45	00	00	00	46	00	00	00	47	00	00	00	73	70	07	D7	E6	E0	0E	AE	CD	C1	1D	5C	9A	83	3B	B8			
00000120	48	00	00	00	49	00	00	00	4A	00	00	00	4B	00	00	00	34	07	77	70	68	0E	EE	E0	D1	1C	DC	C1	A3	39	B8	83			
00000130	4C	00	00	00	4D	00	00	00	4E	00	00	00	4F	00	00	00	47	73	70	07	8E	E6	E0	0E	1D	CD	C1	1D	3A	9A	83	3B			
00000140	50	00	00	00	51	00	00	00	52	00	00	00	53	00	00	00	74	34	07	77	E9	68	0E	EE	D3	D1	1C	DC	A6	A3	39	B8			
00000150	54	00	00	00	55	00	00	00	56	00	00	00	57	00	00	00	4C	47	73	70	98	8E	E6	E0	31	1D	CD	C1	63	3A	9A	83			
00000160	58	00	00	00	59	00	00	00	5A	00	00	00	5B	00	00	00	C6	74	34	07	8D	E9	68	0E	1B	D3	D1	1C	37	A6	A3	39			
00000170	5C	00	00	00	5D	00	00	00	5E	00	00	00	5F	00	00	00	6E	4C	47	73	DC	98	8E	E6	B8	31	1D	CD	70	63	3A	9A			
00000180	60	00	00	00	61	00	00	00	62	00	00	00	63	00	00	00	E1	C6	74	34	C3	8D	E9	68	86	1B	D3	D1	0D	37	A6	A3			
00000190	64	00	00	00	65	00	00	00	66	00	00	00	67	00	00	00	1A	6E	4C	47	34	DC	98	8E	68	B8	31	1D	D0	70	63	3A			
000001A0	68	00	00	00	69	00	00	00	6A	00	00	00	6B	00	00	00	A0	E1	C6	74	41	C3	8D	E9	83	86	1B	D3	06	0D	37	A6			
000001B0	6C	00	00	00	6D	00	00	00	6E	00	00	00	6F	00	00	00	0C	1A	6E	4C	18	34	DC	98	30	68	B8	31	60	D0	70	63			
000001C0	70	00	00	00	71	00	00	00	72	00	00	00	73	00	00	00	C0	A0	E1	C6	81	41	C3	8D	03	83	86	1B	07	06	0D	37			
000001D0	74	00	00	00	75	00	00	00	76	00	00	00	77	00	00	00	0F	0C	1A	6E	1F	18	34	DC	3F	30	68	B8	7F	60	D0	70			
000001E0	78	00	00	00	79	00	00	00	7A	00	00	00	7B	00	00	00	FF	C0	A0	E1	FF	81	41	C3	FE	03	83	86	FD	07	06	0D			
000001F0	7C	00	00	00	7D	00	00	00	7E	00	00	00	7F	00	00	00	FA	0F	0C	1A	F4	1F	18	34	E9	3F	30	68	D3	7F	60	D0			
00000200	01	00	00	00	00	00	00	00	82	00	00	00	83	00	00	00	01	00	00	00	00	00	00	00	02	00	00	00	04	00	00	00			
The 2 nd 512-byte data																																			
00000210	04	00	00	00	05	00	00	00	86	00	00	00	87	00	00	00	09	00	00	00	12	00	00	00	24	00	00	00	49	00	00	00			
00000220	08	00	00	00	09	00	00	00	8A	00	00	00	8B	00	00	00	92	00	00	00	24	01	00	00	49	02	00	00	92	04	00	00			

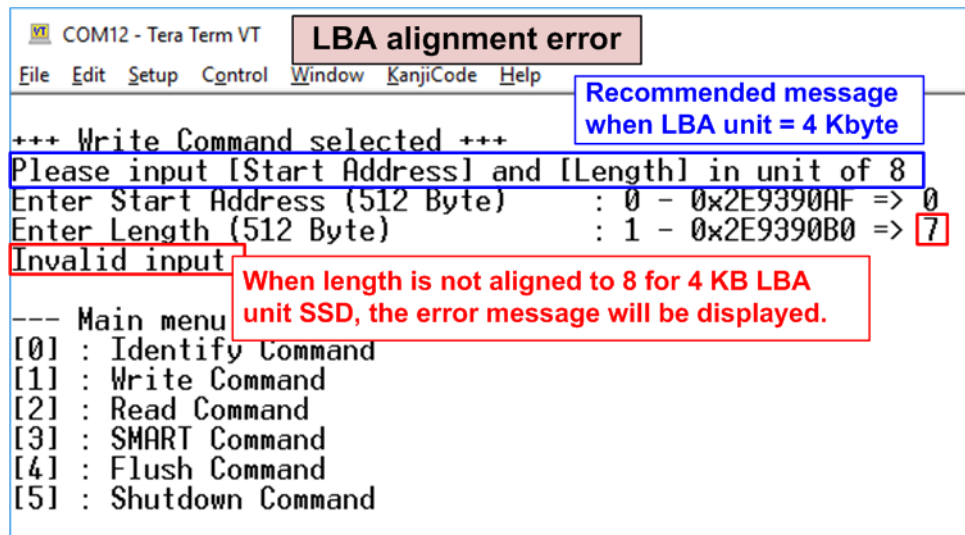
Figure 3-3 Example Test data of the 1st and 2nd 512 byte by using increment/LFSR pattern

Test data in SSD is split into 512-byte unit. For incremental, decremental, or LFSR pattern, each 512-byte data has unique 64-bit header consisting of 48-bit address (in 512-byte unit) and 16-bit zero value. The data after 64-bit header is the test pattern which is selected by user.

The left window of Figure 3-3 shows the example when using 32-bit incremental pattern while the right window shows the example when using 32 bit LFSR pattern. The unique header is not included when running all-0 or all-1 pattern.

When user runs Write or Read command with 4-Kbyte LBA SSD, there is the message displaying on the console to show the input limitation which must be aligned to 8, as shown in Figure 3-4. When the input does not align to 8, "Invalid input" is displayed and the operation is cancelled.

Also, Figure 3-5 shows the example when the input is out of the recommended range for each parameter. The console displays "Invalid input" and then the operation is cancelled.



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

+++ Write Command selected +++
Please input [Start Address] and [Length] in unit of 8
Enter Start Address (512 Byte) : 0 - 0x2E9390AF => 0
Enter Length (512 Byte) : 1 - 0x2E9390B0 => 7
Invalid input

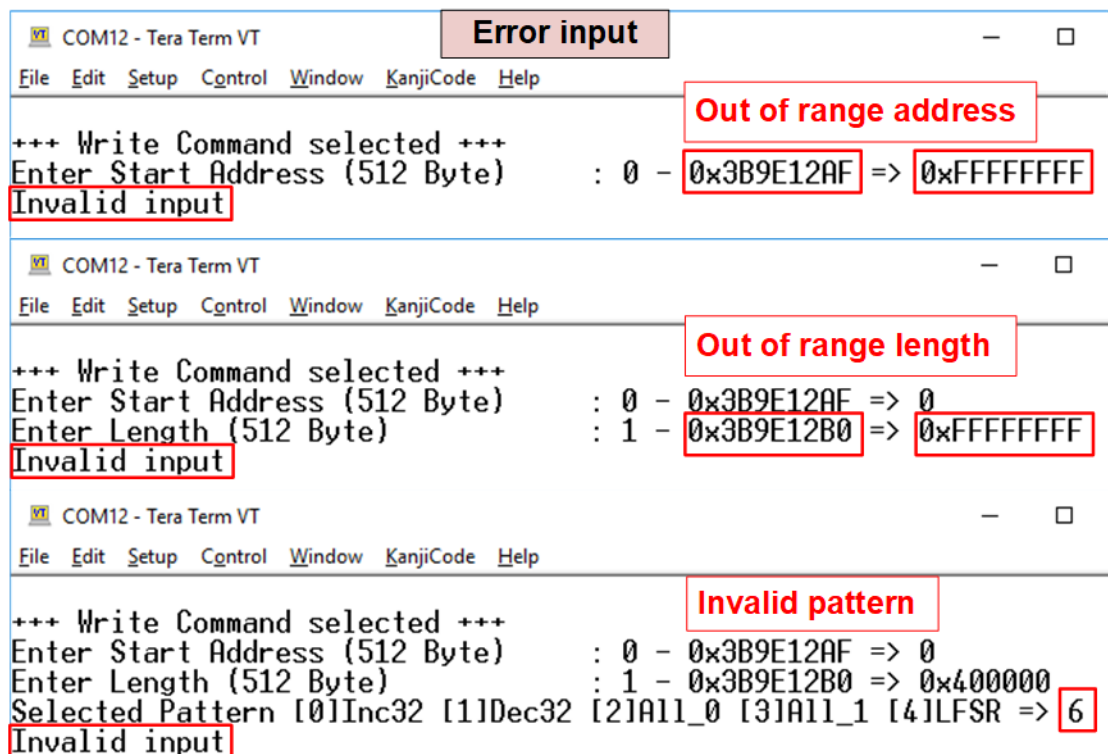
--- Main menu
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command
  
```

LBA alignment error

Recommended message when LBA unit = 4 Kbyte

When length is not aligned to 8 for 4 KB LBA unit SSD, the error message will be displayed.

Figure 3-4 Error message when the input is unaligned for SSD with 4KB LBA unit



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

+++ Write Command selected +++
Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0xFFFFFFFF
Invalid input

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

+++ Write Command selected +++
Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0
Enter Length (512 Byte) : 1 - 0x3B9E12B0 => 0xFFFFFFFF
Invalid input

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

+++ Write Command selected +++
Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0
Enter Length (512 Byte) : 1 - 0x3B9E12B0 => 0x400000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LSR => 6
Invalid input
  
```

Error input

Out of range address

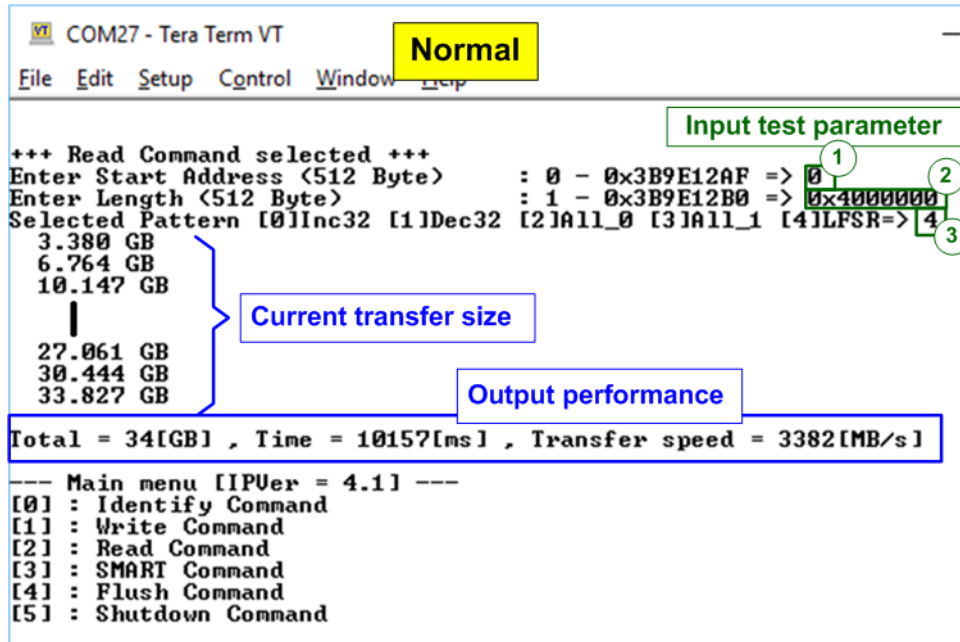
Out of range length

Invalid pattern

Figure 3-5 Error message from the invalid input

3.3 Read Command

Select '2' to send Read command to NVMe SSD.



```

COM27 - Tera Term VT
File Edit Setup Control Window Help

+++ Read Command selected +++
Enter Start Address <512 Byte> : 0 - 0x3B9E12AF => 0
Enter Length <512 Byte> : 1 - 0x3B9E12B0 => 0x40000000
Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 4

3.380 GB
6.764 GB
10.147 GB
27.061 GB
30.444 GB
33.827 GB

Total = 34[GB] , Time = 10157[ms] , Transfer speed = 3382[MB/s]

--- Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command

```

Figure 3-6 Input and result of Read Command menu

User inputs three parameters as follows.

- 1) Start Address: Input start address to read SSD as 512-byte unit. The input is decimal unit when user enters only digit number. User can add "0x" to be prefix for hexadecimal unit. When LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
- 2) Transfer Length: Input total transfer size as 512-byte unit. The input is decimal unit when user enters only digit number. User can add "0x" to be prefix for hexadecimal unit. If LBA unit of SSD is 4 Kbyte, this input must be aligned to 8.
- 3) Test pattern: Select test data pattern to verify data from SSD. Test pattern must be matched with the pattern using in Write Command menu. There are five patterns, i.e. 32-bit incremental, 32-bit decremental, all-0, all-1, and 32-bit LFSR counter

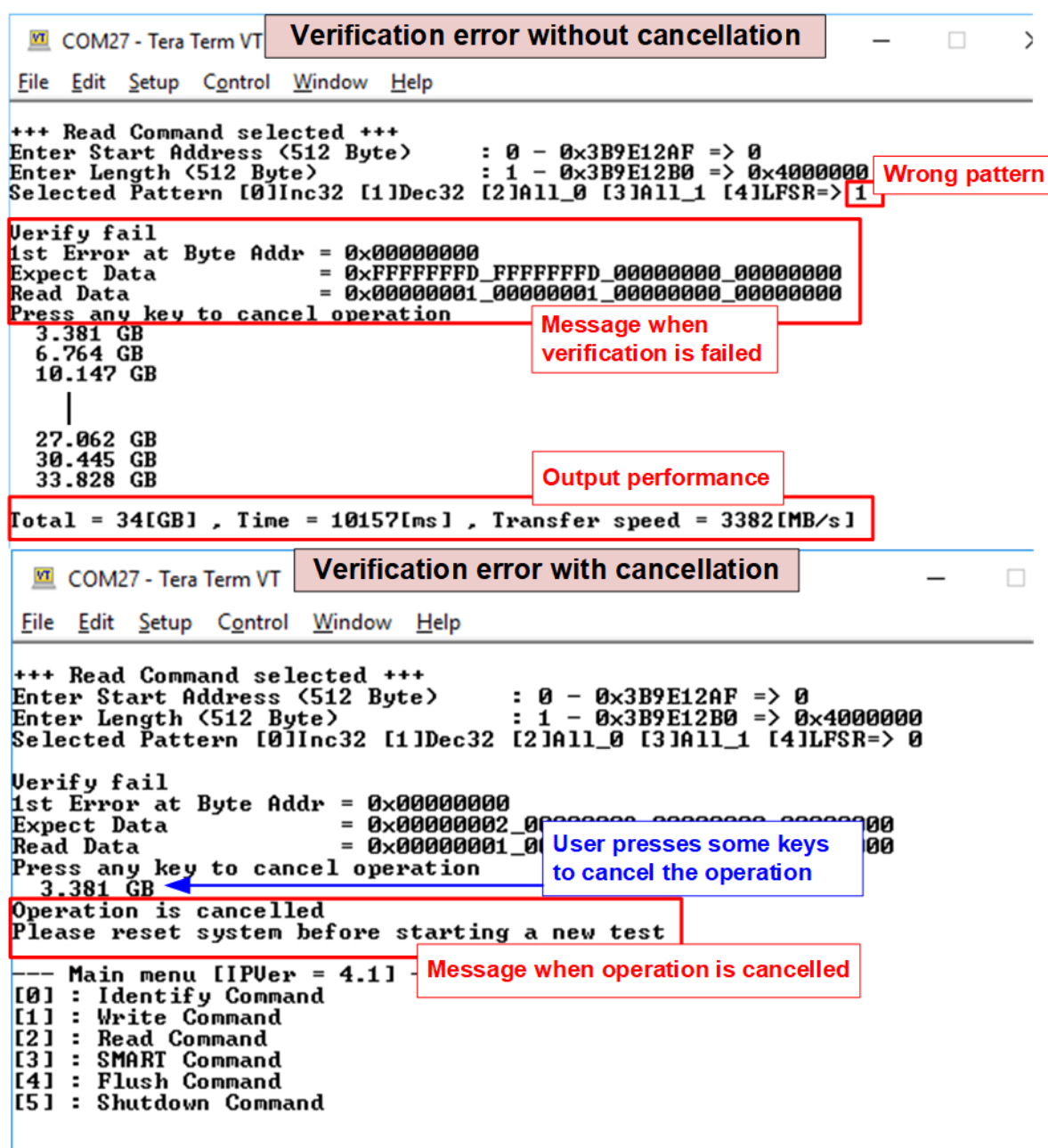
Similar to Write command menu, test system reads data from SSD when all inputs are valid. During reading data, current transfer size is displayed on the console every second to show that system is still alive. Total size, total time usage, and test speed are displayed after finishing the operation.

"Invalid input" is displayed when some inputs are invalid or unaligned to 8 (when connecting to 4-KB LBA SSD).

Figure 3-7 shows error message when data verification is failed. “Verify fail” is displayed with the information of the 1st failure data, i.e. the error byte address, the expected value, and the read value.

User can press any key(s) to cancel read operation or wait until finishing Read command. Similar to the normal condition, the output performance is displayed on the console when the user does not enter any key(s) to stop the operation.

When cancelling the operation, the read command still runs as the background process. It is recommended to power-off/on AB18, and then press “RESET” button to restart system.



The screenshot displays two windows from the Tera Term VT application, both titled "COM27 - Tera Term VT".

Top Window: Verification error without cancellation

- Menu: File Edit Setup Control Window Help
- Content:
 - +++ Read Command selected +++
 - Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0
 - Enter Length (512 Byte) : 1 - 0x3B9E12B0 => 0x4000000
 - Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 1
 - Verify fail
 - 1st Error at Byte Addr = 0x00000000
 - Expect Data = 0xFFFFFFFF_FFFFFFFD_00000000_00000000
 - Read Data = 0x00000001_00000001_00000000_00000000
 - Press any key to cancel operation
 - 3.381 GB
 - 6.764 GB
 - 10.147 GB
 - |
 - 27.062 GB
 - 30.445 GB
 - 33.828 GB
 - Total = 34[GB] , Time = 10157[ms] , Transfer speed = 3382[MB/s]
- Annotations:
 - "Wrong pattern" points to the Selected Pattern line.
 - "Message when verification is failed" points to the "Verify fail" section.
 - "Output performance" points to the transfer speed line.

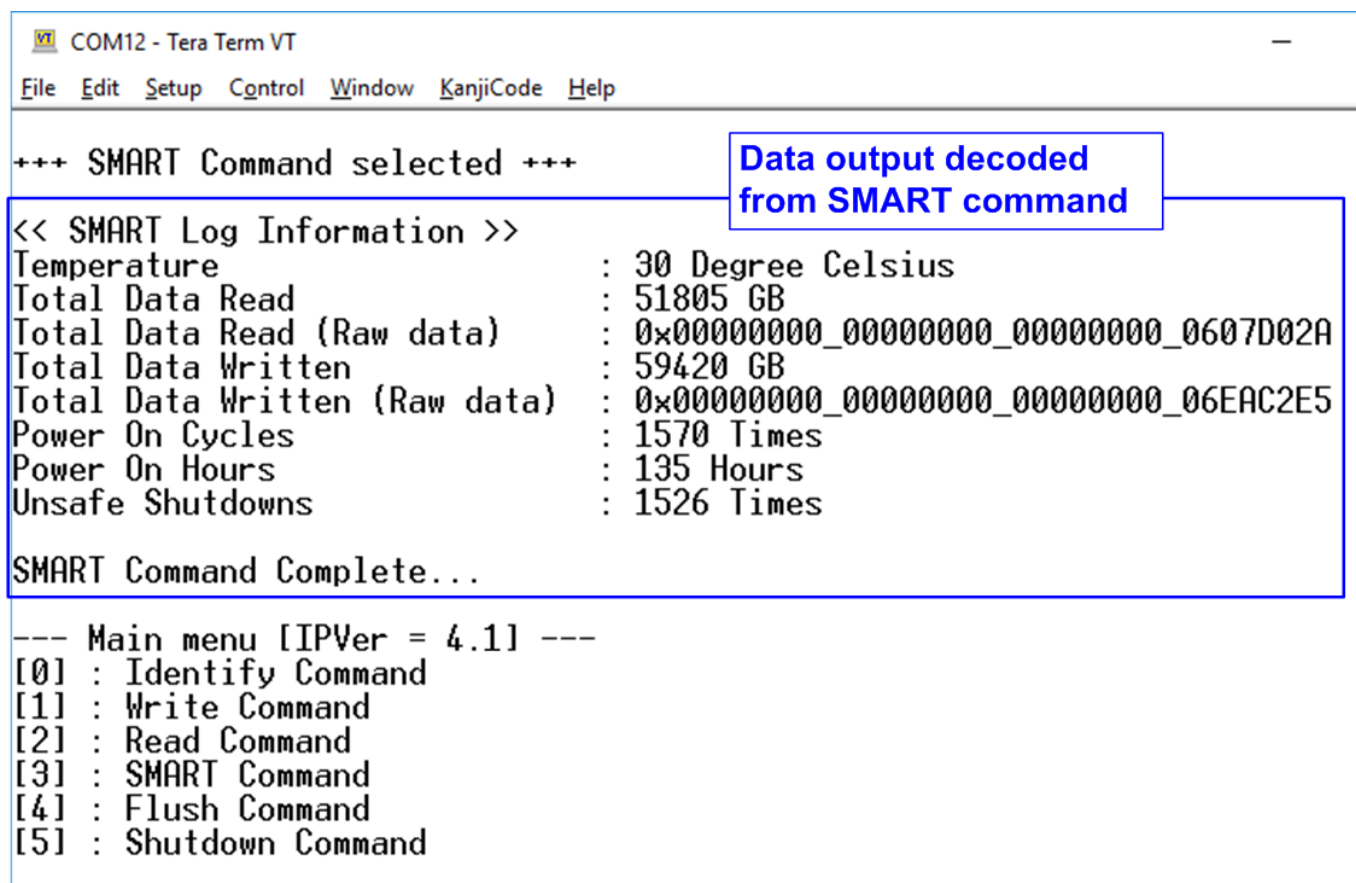
Bottom Window: Verification error with cancellation

- Menu: File Edit Setup Control Window Help
- Content:
 - +++ Read Command selected +++
 - Enter Start Address (512 Byte) : 0 - 0x3B9E12AF => 0
 - Enter Length (512 Byte) : 1 - 0x3B9E12B0 => 0x4000000
 - Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=> 0
 - Verify fail
 - 1st Error at Byte Addr = 0x00000000
 - Expect Data = 0x00000002_00000000_00000000_00000000
 - Read Data = 0x00000001_00000000_00000000_00000000
 - Press any key to cancel operation
 - 3.381 GB
 - Operation is cancelled
 - Please reset system before starting a new test
 - Main menu [IPVer = 4.1] ---
 - [0] : Identify Command
 - [1] : Write Command
 - [2] : Read Command
 - [3] : SMART Command
 - [4] : Flush Command
 - [5] : Shutdown Command
- Annotations:
 - "User presses some keys to cancel the operation" points to the "Press any key to cancel operation" line.
 - "Message when operation is cancelled" points to the "Operation is cancelled" line.

Figure 3-7 Data verification is failed

3.4 SMART Command

Select '3' to send SMART command to NVMe SSD.



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

+++ SMART Command selected +++

<< SMART Log Information >>
Temperature                : 30 Degree Celsius
Total Data Read             : 51805 GB
Total Data Read (Raw data)  : 0x00000000_00000000_00000000_0607D02A
Total Data Written          : 59420 GB
Total Data Written (Raw data) : 0x00000000_00000000_00000000_06EAC2E5
Power On Cycles             : 1570 Times
Power On Hours              : 135 Hours
Unsafe Shutdowns            : 1526 Times

SMART Command Complete...

--- Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command
  
```

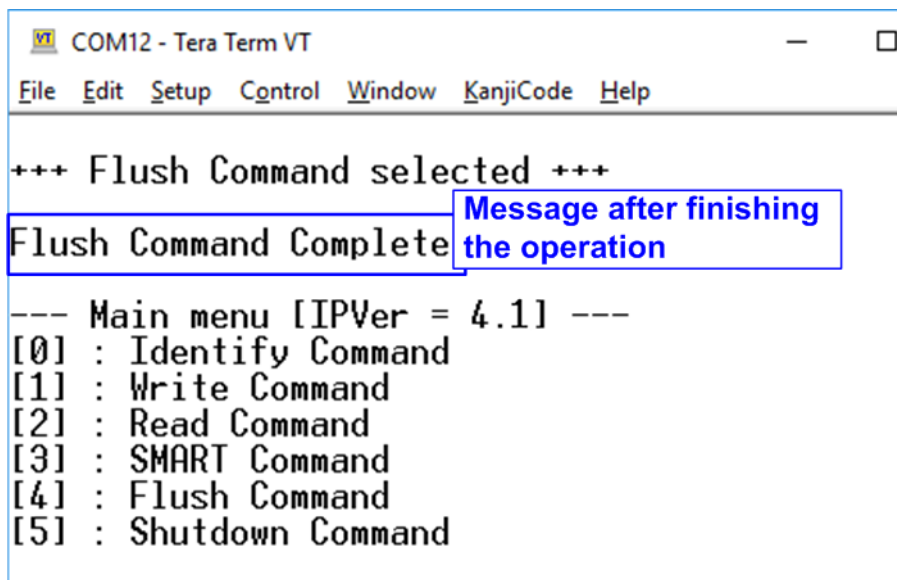
Figure 3-8 Test result when running SMART command

When finishing the operation, SMART/Health Information (output from SMART command) is displayed as shown in Figure 3-8. The console shows six parameters, described as follows.

- 1) Temperature in °C unit.
- 2) Total Data Read decoded as GB/TB unit. Additionally, raw data without decoding is displayed in 128-bit hexadecimal unit. The unit size of raw data is 512,000 byte.
- 3) Total Data Written decoded as GB/TB unit. Additionally, raw data without decoding is displayed in 128-bit hexadecimal unit. The unit size of raw data is 512,000 byte.
- 4) Power On Cycles: Display the number of power cycles.
- 5) Power On Hours: Display period of time in hours to show how long the SSD has been powered on.
- 6) Unsafe Shutdowns: Display the number of unsafe shutdowns of SSD

3.5 Flush Command

Select '4' to send Flush command to NVMe SSD.



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

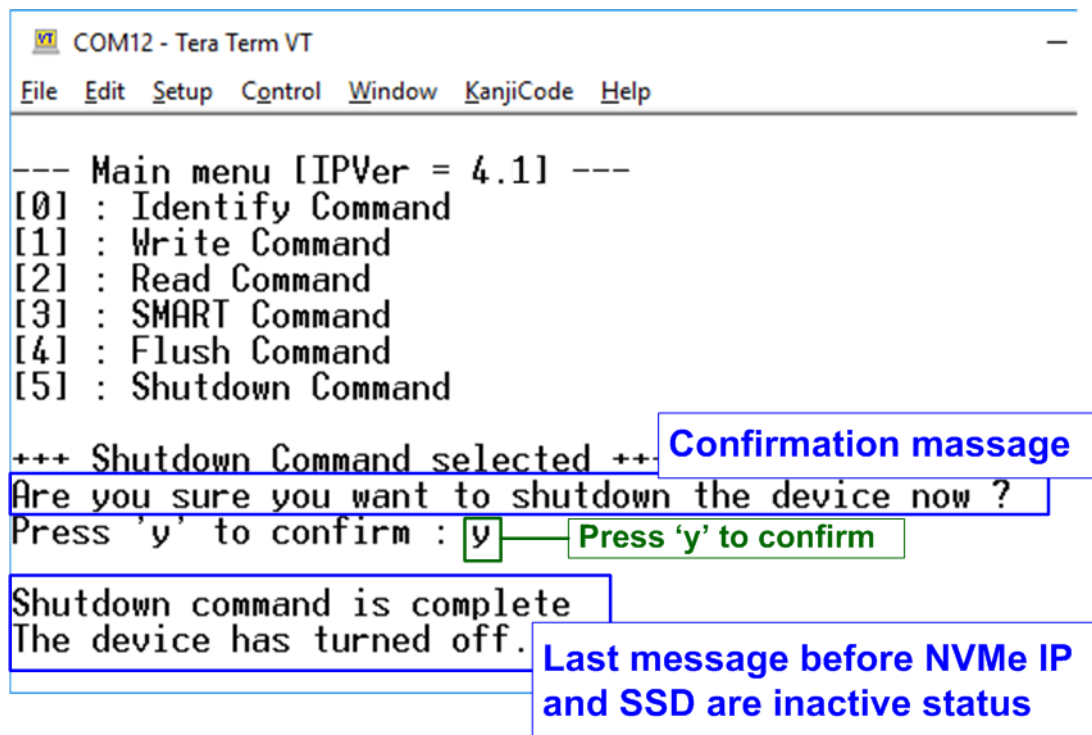
+++ Flush Command selected +++
Flush Command Complete
--- Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command
  
```

Figure 3-9 Test result when running Flush command

“Flush Command Complete” is displayed after finishing Flush operation.

3.6 Shutdown Command

Select '5' to send Shutdown command to NVMe SSD.



```

COM12 - Tera Term VT
File Edit Setup Control Window KanjiCode Help

--- Main menu [IPVer = 4.1] ---
[0] : Identify Command
[1] : Write Command
[2] : Read Command
[3] : SMART Command
[4] : Flush Command
[5] : Shutdown Command

+++ Shutdown Command selected ++
Are you sure you want to shutdown the device now ?
Press 'y' to confirm : y
Shutdown command is complete
The device has turned off.
  
```

Confirmation message

Press 'y' to confirm

Last message before NVMe IP and SSD are inactive status

Figure 3-10 Shutdown Command with confirmation

The confirmation message is displayed on the console. User inputs 'y' or 'Y' to confirm the operation or inputs other keys to cancel the operation.

After finishing Shutdown operation, "Shutdown command is complete" is displayed on the console as the last message. Main menu is not displayed anymore. User needs to power off/on test system to start new test operation.

4 Revision History

Revision	Date	Description
1.0	2-Jun-16	Initial version release
1.1	17-Jun-16	Support KCU105 board
1.2	5-Sep-16	Support ZC706 board
1.3	9-Sep-16	Support KC705 board
1.4	29-Sep-16	Support Zynq Mini-ITX board
1.5	28-Oct-16	Support VC709 board
1.6	14-Dec-16	Update performance result of new buffer system
2.0	8-Jun-17	New NVMe IP version
2.1	27-Jul-17	Add LFSR pattern
2.2	30-Nov-17	Support ZCU106 board
2.3	13-Mar-18	Add numbers of lane message
3.0	19-Jul-18	Support Shutdown, SMART, and Flush command
3.1	23-Nov-18	Support AC701 board
3.2	3-May-19	Support VCU118 board
3.3	28-Jan-20	Update board demo by using AB18
3.4	20-Apr-20	Remove power adapter cable from AB18