NVMe-IP for PLDA PCIe by AB17 Demo Instruction

Rev1.0 9-Oct-18

This document describes the instruction to run NVMe-IP demo on FPGA development board by using AB17-M2FMC board. The demo is designed to write/verify data with M.2 NVMe SSD. User controls test operation through Serial console.

1 Environment Requirement

To run the demo on FPGA development board, please prepare following environment.

1) FPGA Development board: ZCU102
2) PC installing Xilinx programmer software (Vivado) and Serial console software such as HyperTerminal
3) AB17-M2FMC board, provided by Design Gateway
4) Xilinx Power adapter for FPGA board
5) M.2 NVMe SSD, inserting to Drive#1 M.2 connector on AB17
6) Two micro USB cables for programming FPGA and Serial console, connecting between FPGA board and PC

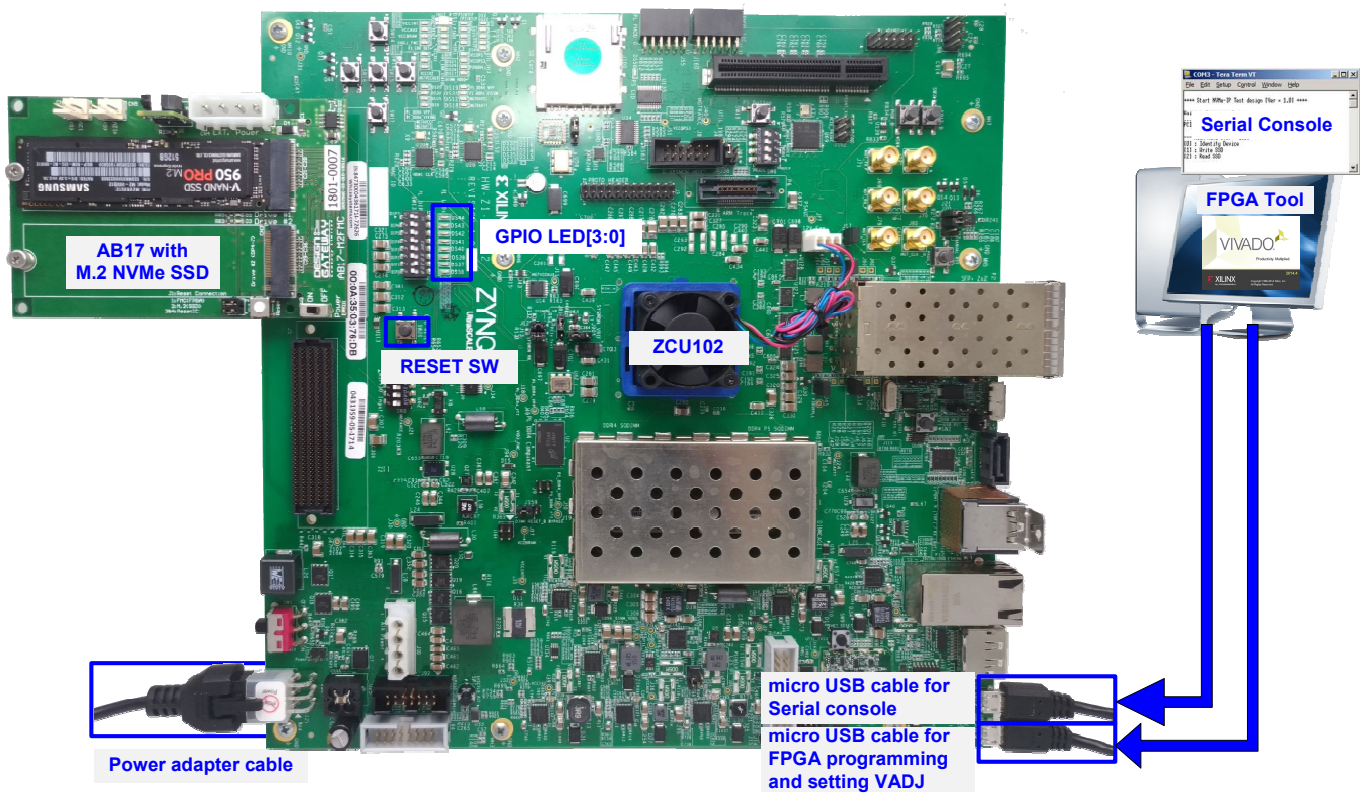

Figure 1-1 NVMe-IP for PLDA PCIe demo by AB17 setup on ZCU102

2 Demo setup

1) Power off system.
2) Connect M.2 NVMe SSD to Drive#1 M.2 connector on AB17-M2FMC, as shown in Figure 2-1.

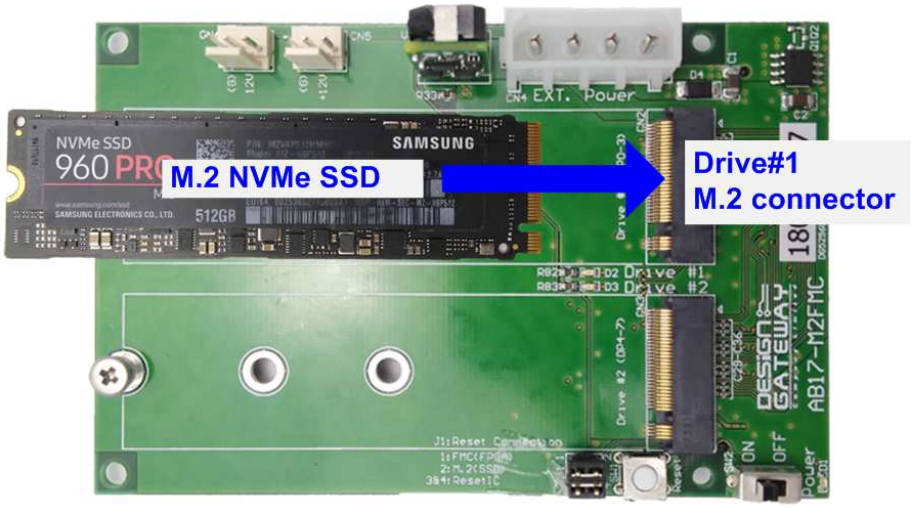

Figure 2-1 Connect M.2 NVMe to AB17

3) Connect AB17-M2FMC to HPC1 connector (J4) for ZCU102 as shown in Figure 2-2.

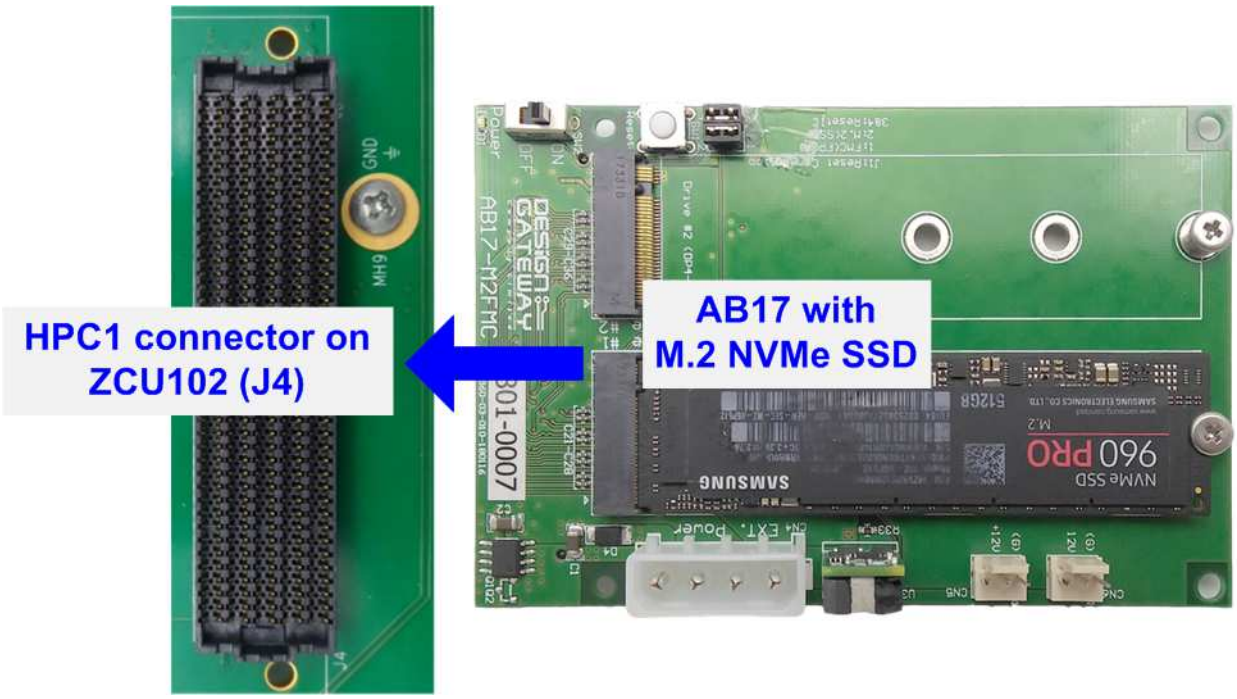

Figure 2-2 Connect AB17 to FPGA board

4) Connect two micro USB cables between FPGA board and PC for FPGA programming and Serial console.

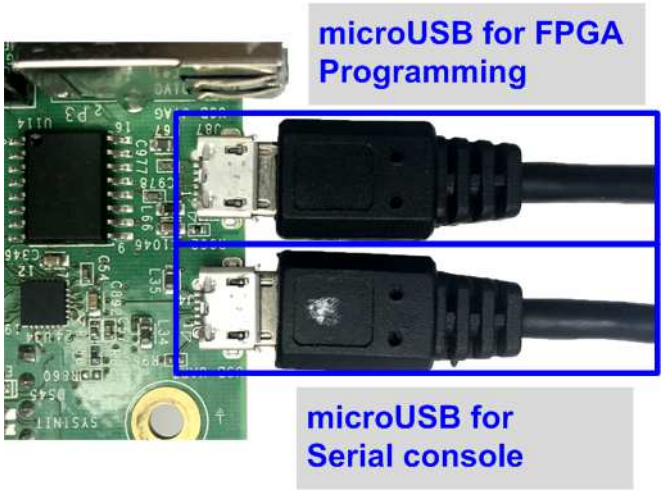

Figure 2-3 USB cable connection

5) Turn on power switch on AB17-M2FMC and FPGA development board, as shown in Figure 2-4.

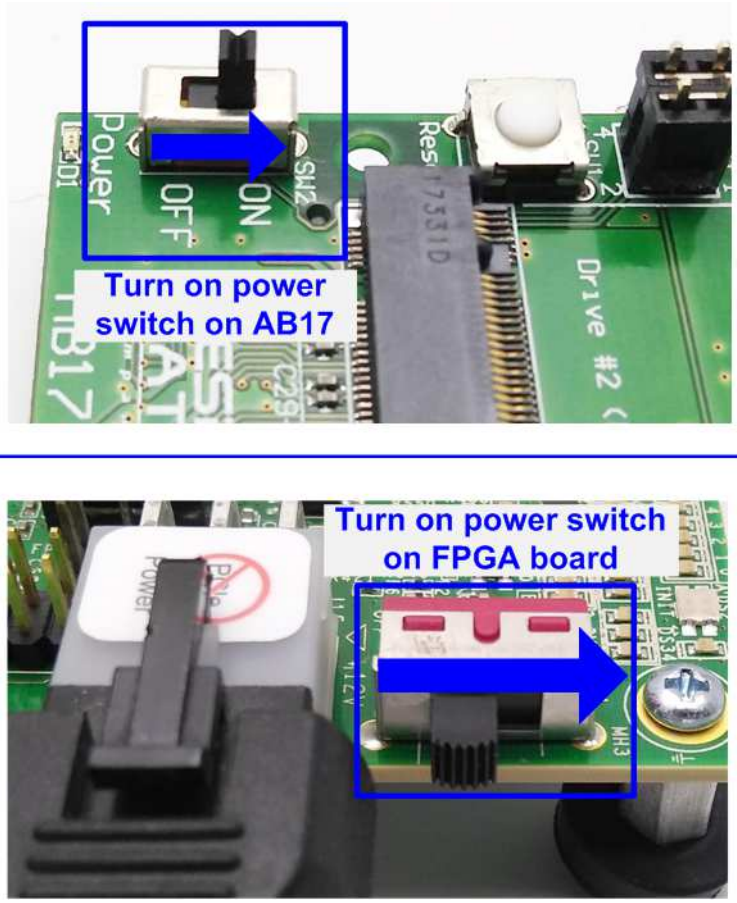

Figure 2-4 Turn on power switch

6) Open Serial console. When connecting ZCU102 board to PC, there are four COM ports displayed on Device Manager. Use COM port number of Interface0 (COM15 in Figure 2-5) for Serial console.

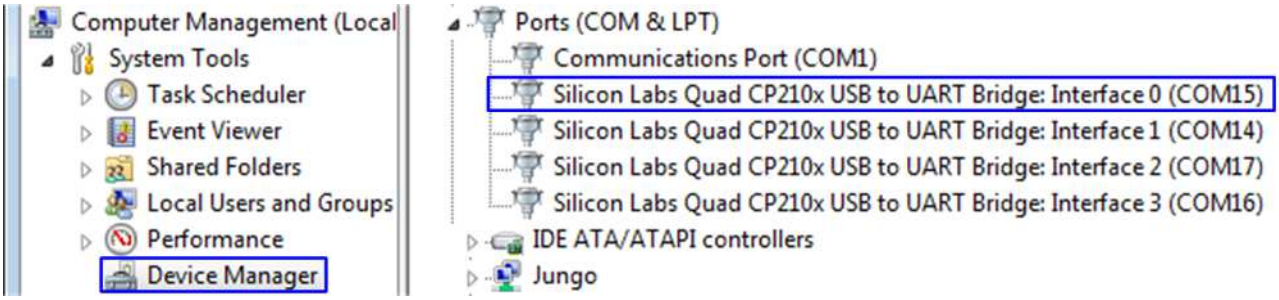

Figure 2-5 Two COM ports from FPGA connection

7) Download and program configuration file and firmware to FPGA board. Open Vivado TCL shell and change directory to download folder which includes demo configuration file. Type “NVMeXR1IPTest_zcu102.bat”, as shown in Figure 2-6.

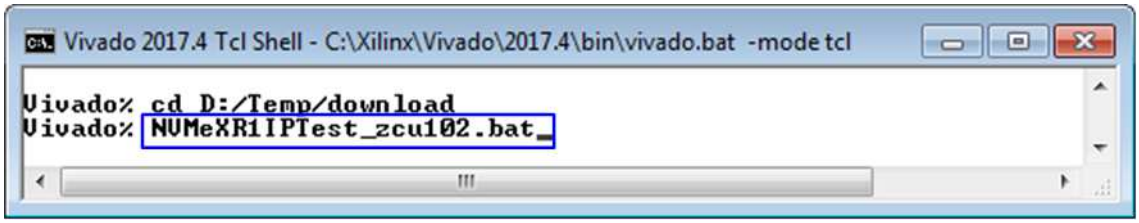

Figure 2-6 Programmed by Vivado

8) Check LED status on FPGA board. The description of LED is as follows.

GPIO LED	ON	OFF
0	Normal operation	SSD is not good status or reset button is pressed
1	System is busy	Idle status
2	IP Error detect	Normal operation
3	Data verification fail	Normal operation

Table 2-1 LED Definition

9) After programming completely, LED[0] and LED[1] are ON during PCIe initialization process. Then, LED[1] changes to OFF after PCIe completes initialization process and system is ready to receive command from user. After that, main menu is displayed, as shown in Figure 2-8.

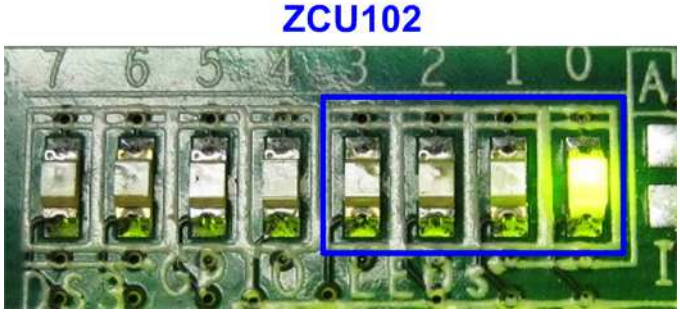

Figure 2-7 LED status after program configuration file and PCIe initialization complete

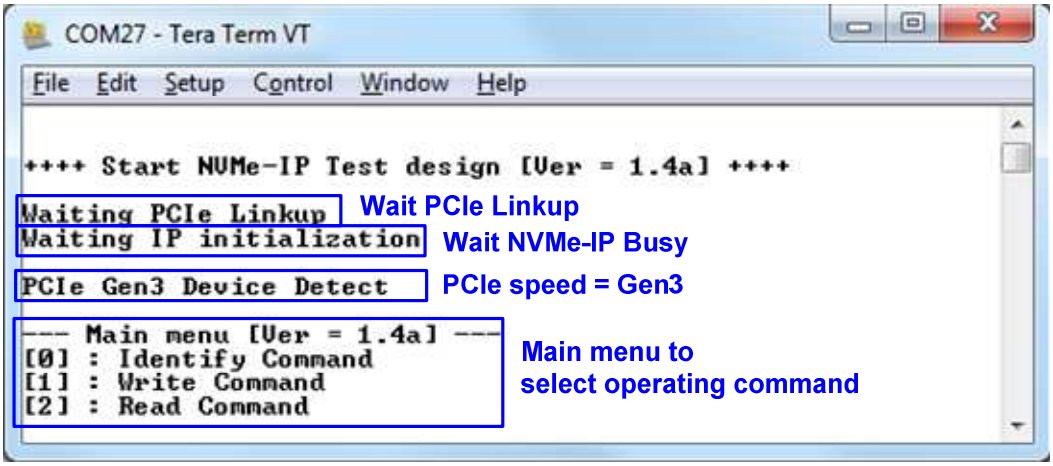

Figure 2-8 Main menu after program configuration file and PCIe initialization complete

3 Test Menu

3.1 Identify Command

Select '0' to send Identify command to NVMe SSD. When operation is completed, SSD information is displayed on the console, i.e.
1) SSD model number
2) SSD capacity which is output from NVMe-IP.

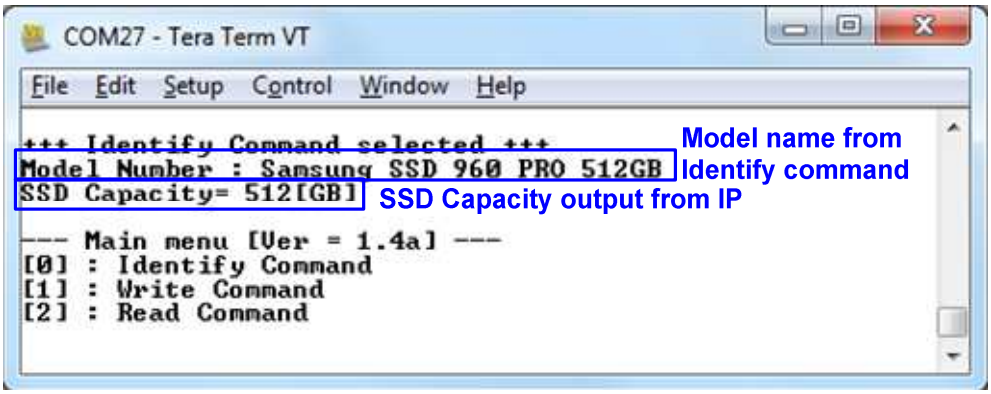

Figure 3-1 Result from Identify Device menu

3.2 Write Command

Select '1' to send Write command to NVMe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
3) Test pattern: Select test pattern of test data for writing to SSD. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, current transfer size is displayed on the console to show that system still run. Finally, test performance, total size, and total time usage are displayed on the console as test result.

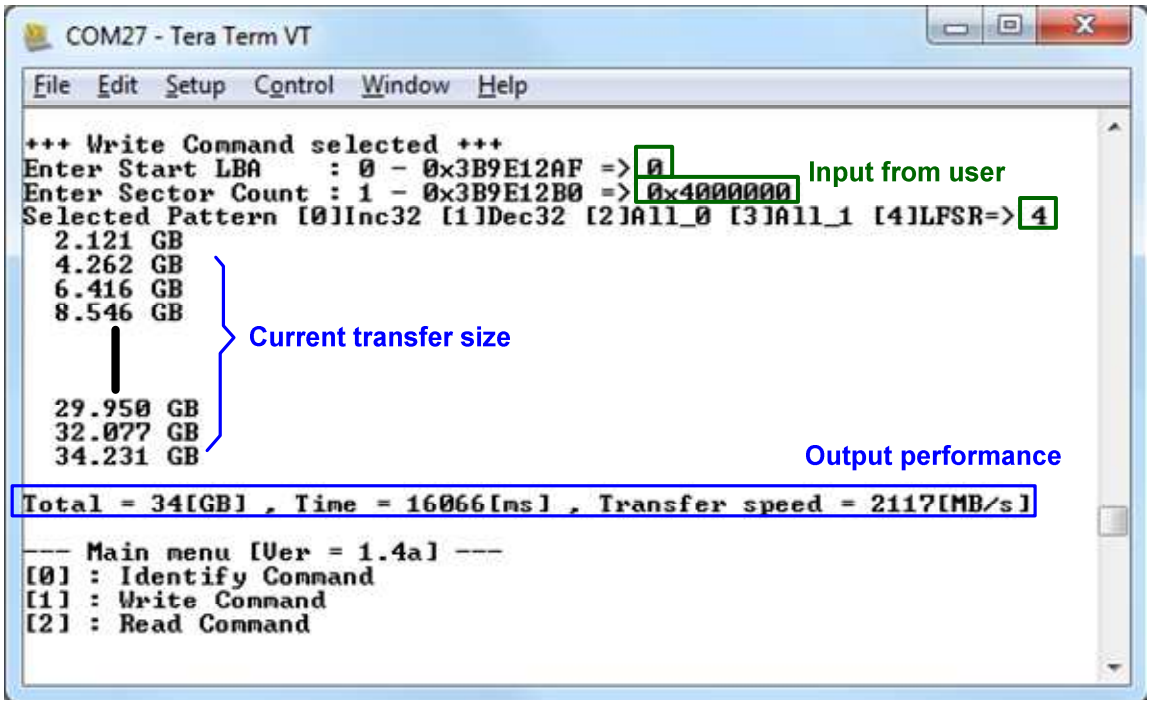

Figure 3-2 Input and result of Write Command menu

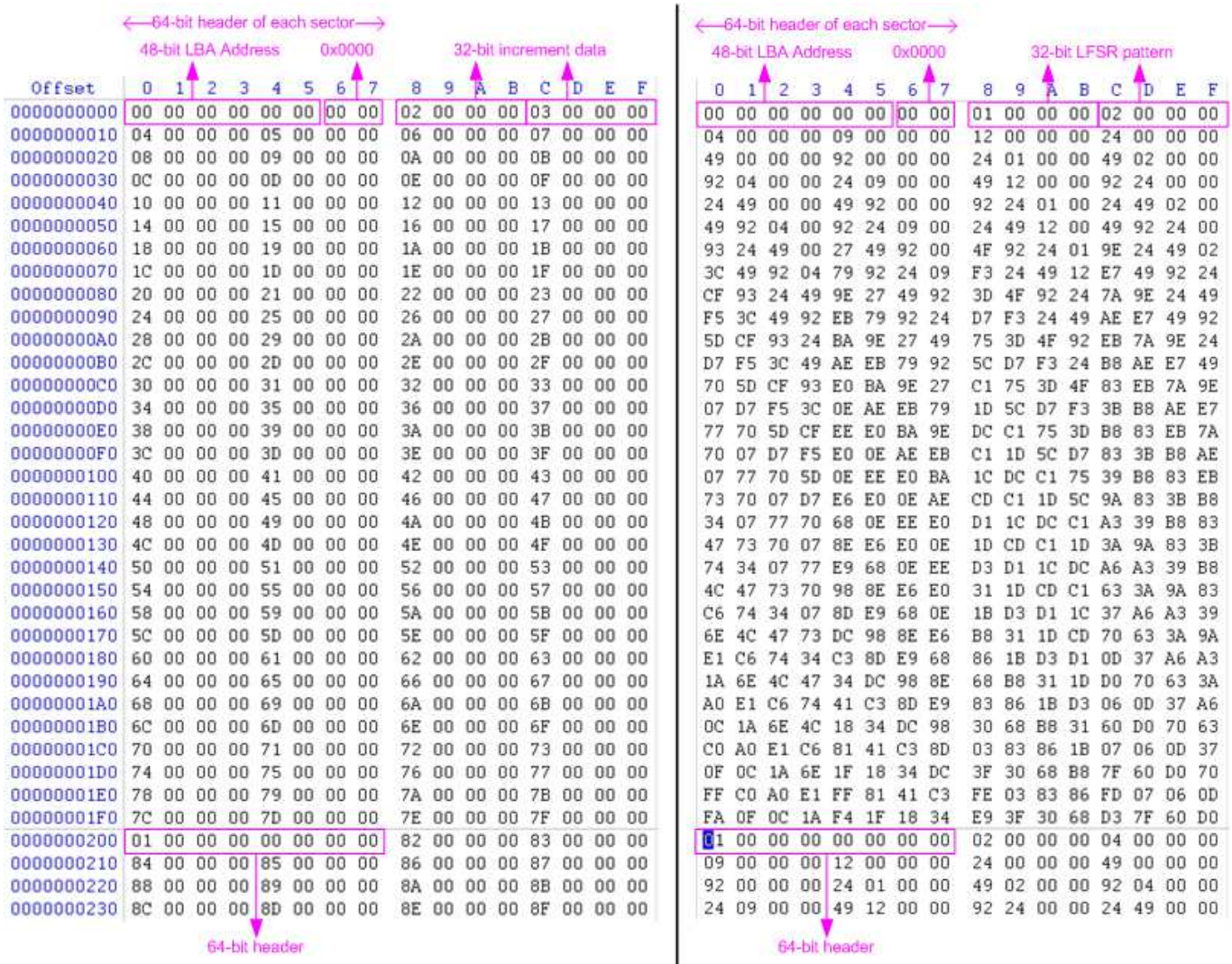

Figure 3-3 Example Test data in sector#0/#1 by increment/LFSR pattern

Test data of each sector has different 64-bit header. 64-bit header consists of 48-bit LBA address and 16-bit zero value. 48-bit LBA address is unique value for each sector. The data after 64-bit header is the test pattern which is selected by user. The example of test pattern is shown in Figure 3-3. 32-bit increment pattern is shown in left window while 32-bit LFSR pattern is shown in right window.

Figure 3-4 – Figure 3-6 show the error message when user input is invalid. “Invalid input” message is displayed on the console and then returns to main menu to receive new command.

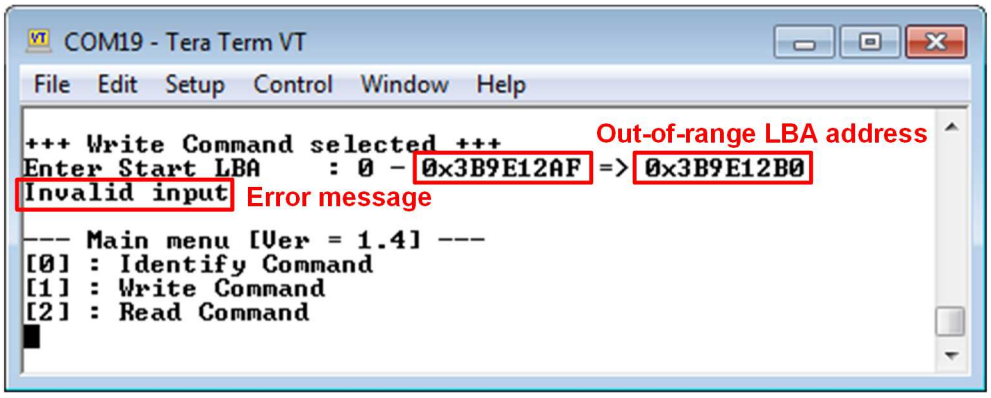

Figure 3-4 Invalid Start LBA input

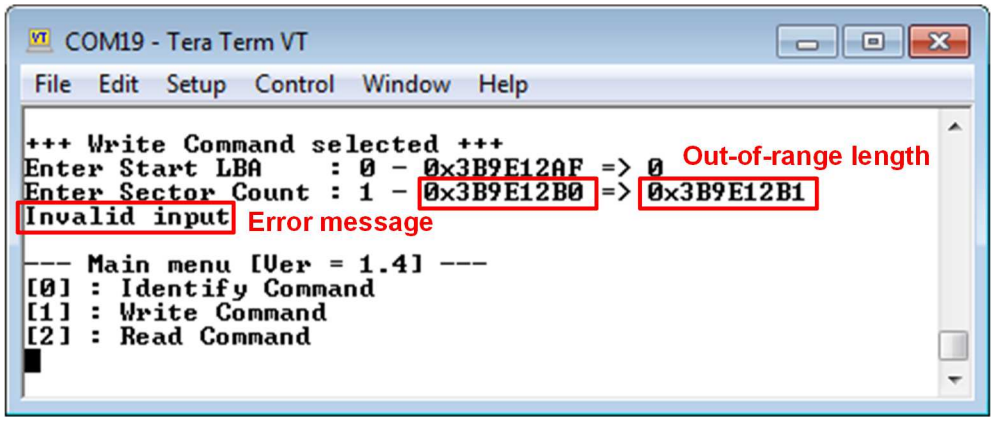

Figure 3-5 Invalid Sector count input

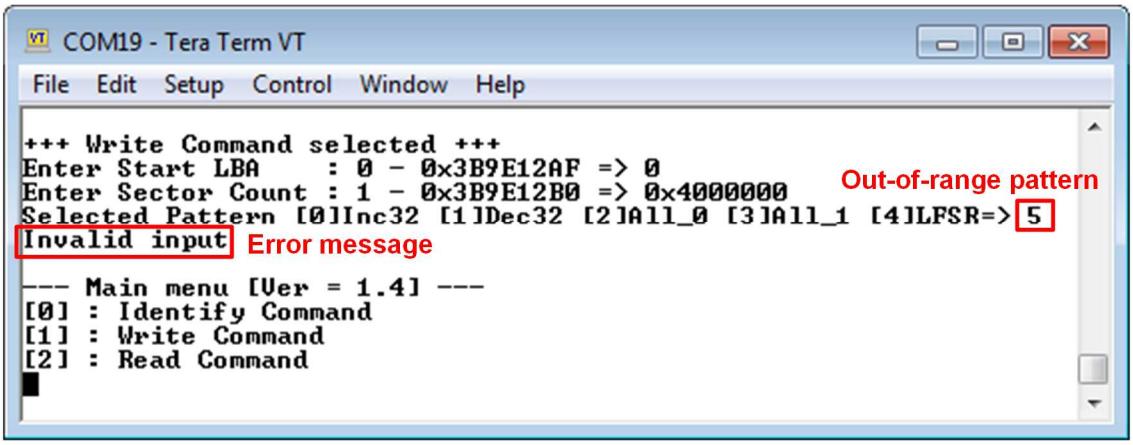

Figure 3-6 Invalid Test pattern input

3.3 Read Command

Select '2' to send Read command to NVMe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with the test pattern using in Write Command menu. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

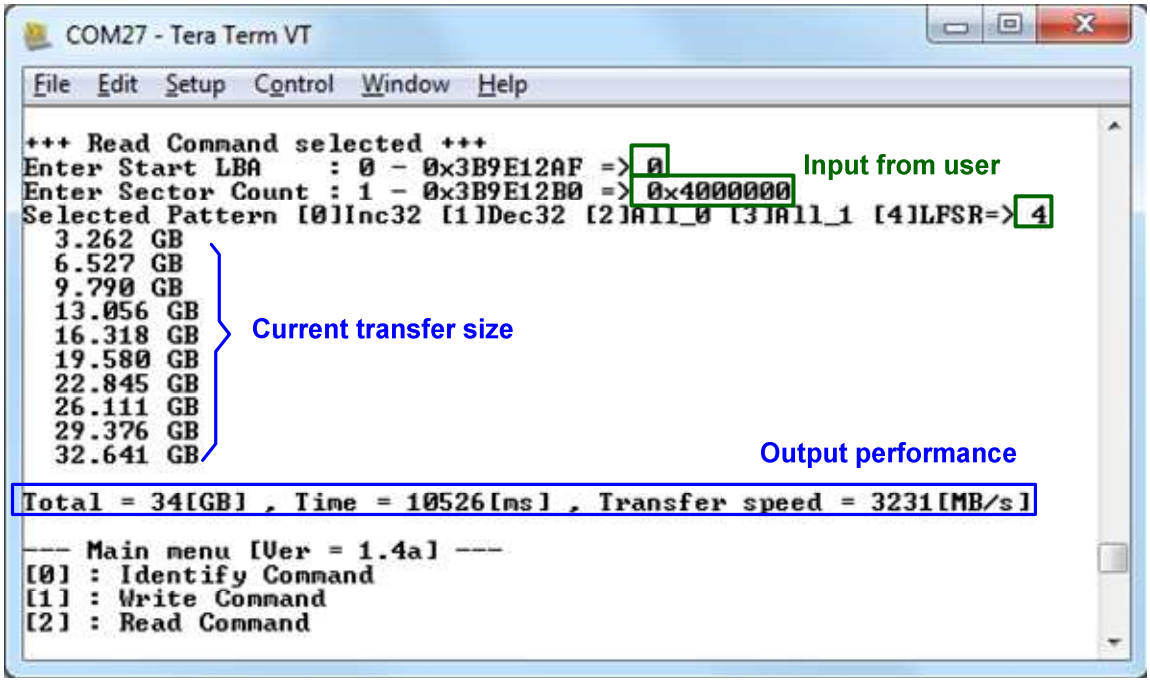

Figure 3-7 Input and result of Read Command menu

Similar to Write Command menu, if all inputs are valid, test system will read data from SSD. Test performance, total size, and total time usage are displayed after end of transfer. "Invalid input" will be displayed if some inputs are out-of-range.

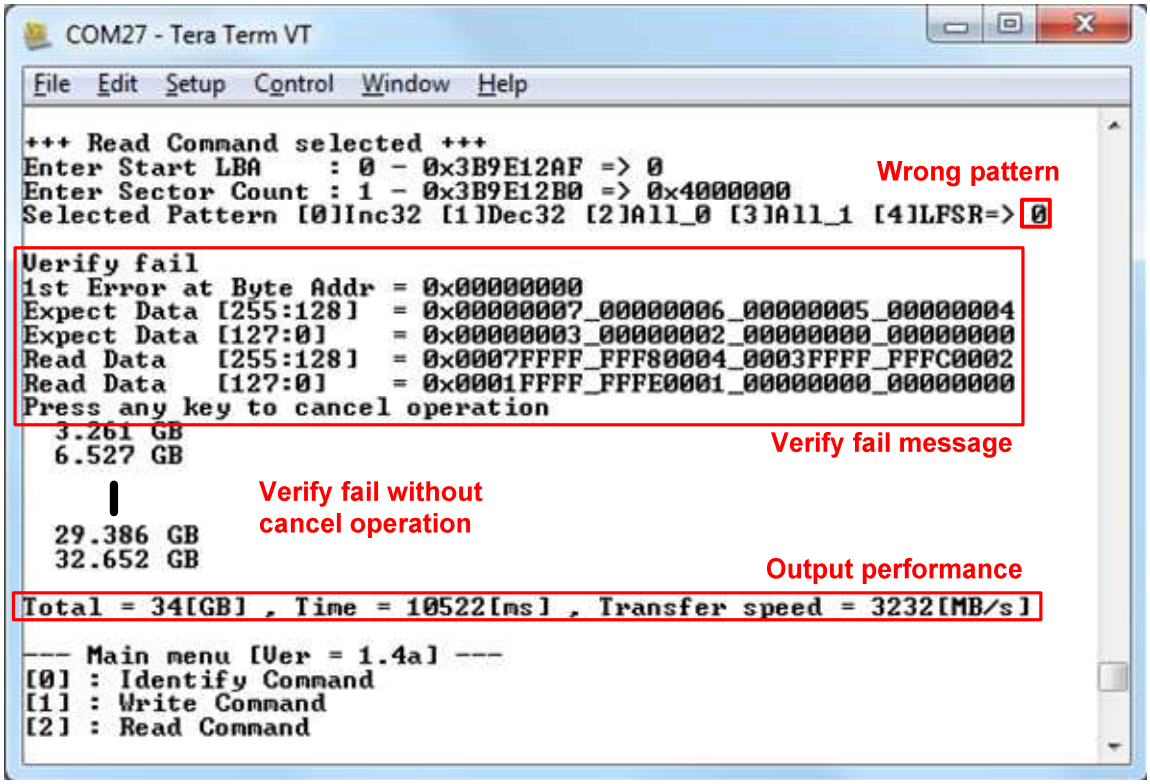

Figure 3-8 Data verification is failed but wait until read complete

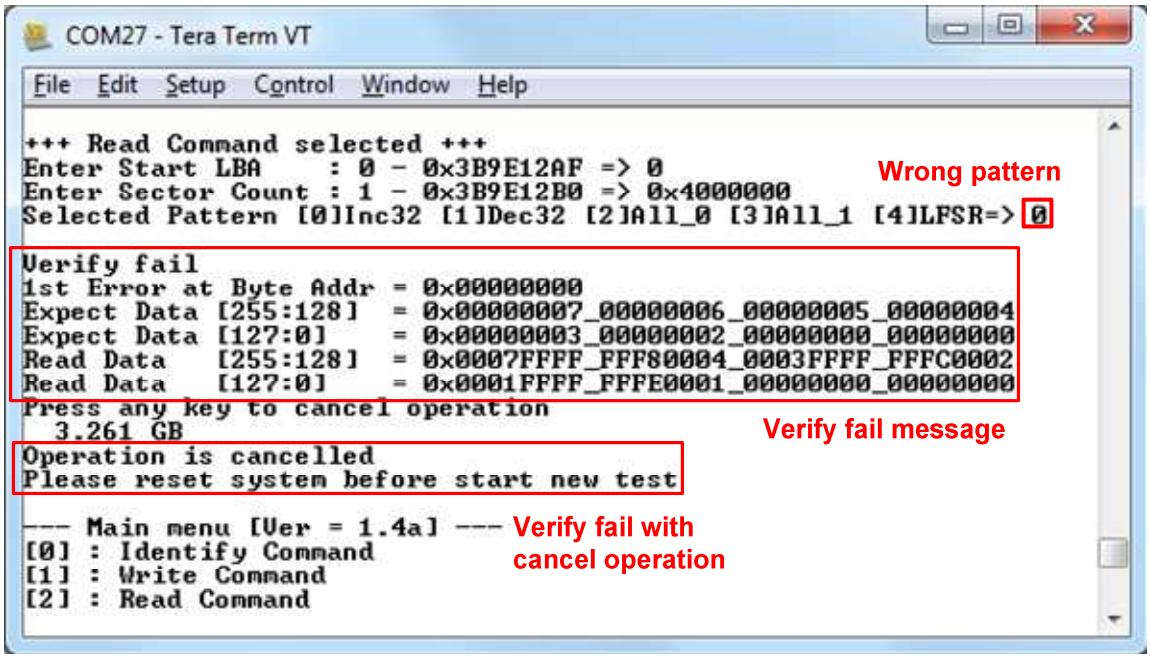

Figure 3-9 Data verification is failed and press any key to cancel operation

Figure 3-8 and Figure 3-9 show error message when data verification is failed. “Verify fail” is displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete.
If read process is completed, output performance from read process will be displayed.

In case of cancel operation, the previous command does not complete in good sequence. It is recommended to power-off/on all AB17 and press “RESET” button to restart system.

4 Revision History

Revision	Date	Description
1.0	9-Oct-18	Initial version release