

# NVMe-IP for PLDA PCIe (PCIe Switch) Demo Instruction

<u>Rev1.0 30-Jan-19</u>

This document describes the instruction to run NVMe-IP for PLDA demo on FPGA development board by connecting SSD through PCIe switch instead of directly connection with SSD. FMC-PCIe adapter card and PCIe switch card with M.2 connector are applied in the demo. The demo is designed to write/verify data one SSD through PCIe switch. Though 4 M.2 NVMe SSD are connected to PCIe switch card, user could select to operate with one SSD. User controls test operation and selects active SSD through Serial console.

# **1** Environment Requirement

To run the demo on FPGA development board, please prepare following environment.

- 1) FPGA Development board: ZCU102
- 2) PC installing Xilinx programmer software (Vivado) and Serial console software such as HyperTerminal
- 3) Xilinx Power adapter for FPGA board
- 4) FMC to PCIe card
- 5) ATX power supply for FMC-to-PCIe card
- a) PCIe switch card with M.2 connector + M.2 NVMe SSD connecting to PCIe switch
   b) PCIe NVMe SSD or PCIe-M.2 adapter card with M.2 SSD
- 7) Two micro USB cables for programming FPGA and Serial console, connecting between FPGA board and PC

Note:

[1] FMC to PCIe adapter card: HTG-FMC-PCIE board

http://www.hitechglobal.com/fmcmodules/fmc\_pciexpress.htm

[2] PCIe switch card with M.2 connector: Quattro 400 M.2 NVMe SSD Adapter http://www.aplicata.com/guattro-400/





# Figure 1-1 NVMe-IP for PLDA PCIe (PCIe Switch) demo on ZCU102



# 2 Demo setup

- 1) Power off system.
- 2) Connect FMC-to-PCIe card to HPC1 connector (J4) on ZCU102, as shown in Figure 2-1.



Figure 2-1 Connect FMC to PCIe board to FPGA board

 Connect ATX power cable to J4 on FMC-to-PCIe card and select power source of FMC (S2) to Ext (external power), as shown in Figure 2-2





4) Connect at least 1 NVMe SSD to PCIe switch card. In the example, four SSDs are connected to show different device number usage from different connector. As shown in Figure 2-3, each connector is defined as different device number depending on PCIe switch schematic. The details of device number for each M.2 connector on reference board are shown in Figure 2-3. After that, install heat sink to cool down NVMe SSD on PCIe switch card.



Figure 2-3 Connect NVMe SSD to PCIe switch



5) Connect PCIe switch card to PCIe female connector on FMC-to-PCIe card.



Figure 2-4 Connect PCIe switch card to FMC-to-PCIe card

6) Connect two micro USB cables between FPGA board and PC for FPGA programming and Serial console, as shown in Figure 2-5.





7) Turn on ATX power supply for FMC-to-PCIe card power and FPGA development board, as shown in Figure 2-6.



Figure 2-6 Turn on power switch

8) Open Serial console. When connecting ZCU102 board to PC, there are four COM ports displayed on Device Manager. Use COM port number of Interface0 (COM15 in Figure 2-7) for Serial console.



 Download and program configuration file and firmware to FPGA board. Open Vivado TCL shell and change directory to download folder which includes demo configuration file. Type "NVMeXR1IPTest\_zcu102.bat", as shown in Figure 2-8.



Figure 2-8 Programmed by Vivado

10)Check LED status on FPGA board. The description of LED is as follows.

GPIO LED	ON	OFF					
0	Normal operation	SSD is not good status or reset button is pressed					
1	System is busy	Idle status					
2	IP Error detect	Normal operation					
3	Data verification fail	Normal operation					
Table 2-1 LED Definition							



- 11)After programming complete, LED[0] and LED[1] are ON during PCIe initialization process. NVMe SSD could be connected to FMC-to-PCIe card by two methods. First method is connecting to FMC-to-PCIe card directly. Second method is connecting to FMC-to-PCIe card through PCIe switch card.
  - a) When NVMe SSD is connected to FMC-to-PCIe card directly, the step is as follows.
    - (1) "Waiting PCIe Linkkup" and "PCIe Genx Device Detect" are displayed to the console.
    - (2) User inputs '0' to select the connection to be direct connection.
    - (3) "Complete PCIe initialization" is displayed when IP completes the initialization sequence.
    - (4) LED[1] changes to OFF and Main menu is displayed to receive command from user.



Figure 2-9 Direct NVMe SSD initialization



Figure 2-10 LED status after complete initialization sequence



- b) When NVMe SSD is connected to PCIe switch card, so FMC-to-PCIe card detects PCIe switch firstly, not NVMe SSD. The step to complete initialization sequence is as follows.
  - (1) "Waiting PCIe Linkup" is displayed.
  - (2) User needs to press S1 on FMC-to-PCIe card (PCIe RESET) to reset PCIe switch and SSD.
  - (3) "PCIe GenX Device Detect" is displayed.
  - (4) User inputs '1' and selects device number to test. Figure 2-3 shows device number position of each M.2 slot on PCIe switch card.
  - (5) "Complete PCIe initialization" is displayed when IP completes the initialization sequence.
  - (6) LED[1] changes to OFF and Main menu is displayed to receive command from user.



Figure 2-11 NVMe SSD through PCIe switch initialization



## 3 Test Menu

#### 3.1 Identify Command

Select '0' to send Identify command to NVMe SSD. When operation is completed, SSD information is displayed on the console, i.e.

- 1) SSD model number
- 2) SSD capacity which is output from NVMe-IP.

📒 COM27 - Tera Term VT	
<u>File Edit Setup Control Window H</u> elp	
+++ Identify Command selected +++ Model Number : Samsung SSD 960 PRO 51 SSD Capacity= 512[GB] Capacity (output Main menu [Ver = 1.5] [0] : Identify Command [1] : Write Command	Model name [2GB] (decoded from Identify data) from IP)
[2] : Read Command [9] : Re-Initial System	-

Figure 3-1 Result from Identify Device menu



#### 3.2 Write Command

Select '1' to send Write command to NVMe SSD. Three inputs are required for this menu.

- 1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
- 2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
- 3) Test pattern: Select test pattern to write test data to SSD. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, current transfer size is displayed on the console to show that system still run. Finally, test performance, total size, and total time usage are displayed on the console as test result.



Figure 3-2 Input and result of Write Command menu



<=64-bit header of each sector→									-	64-b	it hea	ader	of ea	ich s	ecto	$\rightarrow$																	
	48-bit LBA Address 0x0000 32-bit increment data								4	8-bit	LBA	Addr	ess		0x0	000			32-Ь	it LF	SR p	atte	'n										
Offset	0	1	2	3	4	5	6	7	8	9	A	В	C	D	E	F	<b>[</b> ]	0	1	2	3	4	5	6	7	8	9	A	в	C	D	E	F
0000000000	00	00	00	00	00	00	00	00	02	00	00	00	03	00	00	00		00	00	00	00	00	00	00	00	01	00	00	00	02	00	00	00
0000000010	04	00	00	00	05	00	00	00	06	00	00	00	07	00	00	00		04	00	00	00	09	00	00	00	12	00	00	00	24	00	00	00
0000000020	08	00	00	00	09	00	00	00	0A	00	00	00	0B	00	00	00		49	00	00	00	92	00	00	00	24	01	00	00	49	02	00	00
0000000030	0C	00	00	00	OD	00	00	00	0E	00	00	00	OF	00	00	00	11	92	04	00	00	24	09	00	00	49	12	00	00	92	24	00	00
0000000040	10	00	00	00	11	00	00	00	12	00	00	00	13	00	00	00	11	24	49	00	00	49	92	00	00	92	24	01	00	24	49	02	00
0000000050	14	00	00	00	15	00	00	00	16	00	00	00	17	00	00	00	11	49	92	0.4	00	92	24	09	00	24	49	12	00	49	92	24	00
0000000060	18	00	00	00	19	00	00	00	1A	00	00	00	1B	00	00	00	11	93	24	49	00	27	49	92	00	4F	92	24	01	9E	24	49	02
0000000070	1C	00	00	00	1D	00	00	00	1E	00	00	00	1F	00	00	00	11	30	49	92	04	79	92	24	09	FЗ	24	49	12	E7	49	92	2.4
0000000080	20	00	00	00	21	00	00	00	22	00	00	00	23	00	00	00	11	CF	93	24	49	9E	27	49	92	ЗD	4F	92	24	7A	9E	24	49
0000000090	24	00	00	00	25	00	00	00	26	00	00	00	27	00	00	00	11	F5	3C	49	92	EB	79	92	24	D7	F3	24	49	AE	E7	49	92
00000000A0	28	00	00	00	29	00	00	00	2A	00	00	00	2B	00	00	00	11	5D	CF	93	24	BA	9E	27	49	75	3D	4F	92	EB	7A	9E	24
00000000B0	2C	00	00	00	2D	00	00	00	2E	00	00	00	2F	00	00	00	11	D7	F5	3C	49	AE	EB	79	92	5C	D7	F3	24	B8	ΑE	E7	49
00000000000	30	00	00	00	31	00	00	00	32	00	00	00	33	00	00	00	11	70	5D	CF	93	EO	BA	9E	27	C1	75	3D	4F	83	EB	7A	9E
0000000000	34	00	00	00	35	00	00	00	36	00	00	00	37	00	00	00	11	07	D7	F5	3C	OE	AE	EB	79	1D	5C	D7	FЗ	3B	B8	AE	E7
00000000E0	38	00	00	00	39	00	00	00	ЗÀ	00	00	00	ЗB	00	00	00	11	77	70	5D	CF	EE	EO	BA	9E	DC	C1	75	ЗD	B8	83	EB	7A
00000000F0	3C	00	00	00	3D	00	00	00	3E	00	00	00	ЗF	00	00	00	11	70	07	D7	F5	EO	OE	AE	EB	C1	1D	5C	D7	83	3B	B8	AE
0000000100	40	00	00	00	41	00	00	00	42	00	00	00	43	00	00	00	11	07	77	70	5D	0E	EE	EO	BA	1C	DC	C1	75	39	B8	83	EB
0000000110	44	00	00	00	45	00	00	00	46	00	00	00	47	00	00	00	11	73	70	07	D7	E6	EO	OE	ÀΕ	CD	C1	1D	5C	9A	83	3B	B8
0000000120	48	00	00	00	49	00	00	00	4A	00	00	00	4B	00	00	00	11	34	07	77	70	68	0E	EE	EO	D1	1C	DC	C1	A3	39	B8	83
0000000130	4C	00	00	00	4D	00	00	00	4E	00	00	00	4F	00	00	00	11	47	73	70	07	8E	E6	EO	0E	1D	CD	C1	1D	ЗA	9A	83	ЗB
0000000140	50	00	00	00	51	00	00	00	52	00	00	00	53	00	00	00	11	74	34	07	77	E9	68	OE	EE	D3	D1	1C	DC	A6	A3	39	B8
0000000150	54	00	00	00	55	00	00	00	56	00	00	00	57	00	00	00	11	40	47	73	70	98	8E	E6	EO	31	1D	CD	C1	63	3A	9A	83
0000000160	58	00	00	00	59	00	00	00	5A	00	00	00	5B	00	00	00	11	C6	74	34	07	8D	E9	68	0E	1B	D3	D1	1C	37	A6	A3	39
0000000170	5C	00	00	00	SD	00	00	00	5E	00	00	00	SF	00	00	00	11	6E	4C	47	73	DC	98	8E	E6	B8	31	1D	CD	70	63	ЗA	9A
0000000180	60	00	00	00	61	00	00	00	62	00	00	00	63	00	00	00	11	E1	C6	74	34	C3	8D	E9	68	86	1B	D3	D1	0D	37	A6	A3
0000000190	64	00	00	00	65	00	00	00	66	00	00	00	67	00	00	00	11	1A	6E	4C	47	34	DC	98	8E	68	88	31	1D	DO	70	63	ЗĂ
00000001A0	68	00	00	00	69	00	00	00	6A	00	00	00	6B	00	00	00	11	AO	E1	C6	74	41	C3	8D	E9	83	86	1B	DЗ	06	OD	37	Å6
00000001B0	6C	00	00	00	6D	00	00	00	6E	00	00	00	6F	00	00	00	11	0C	1A	6E	4C	18	34	DC	98	30	68	B8	31	60	DO	70	63
00000001C0	70	00	00	00	71	00	00	00	72	00	00	00	73	00	00	00	11	CO	AO	E1	C6	81	41	C3	8D	03	83	86	1B	07	06	OD	37
00000001D0	74	00	00	00	75	00	00	00	76	00	00	00	77	00	00	00	11	OF	0C	1A	6E	1F	18	34	DC	3F	30	68	B8	7F	60	DO	70
00000001E0	78	00	00	00	79	00	00	00	7A	00	00	00	7B	00	00	00	11	FF	CO	AO	E1	FF	81	41	C3	FE	03	83	86	FD	07	06	OD
00000001F0	7C	00	00	00	7D	00	00	00	7E	00	00	00	7F	00	00	00		FA	OF	0C	1A	F4	1F	18	34	E9	3F	30	68	D3	7F	60	DO
0000000200	01	00	00	00	00	00	00	00	82	00	00	00	83	00	00	00		1	00	00	00	00	00	00	00	02	00	00	00	04	00	00	00
0000000210	84	00	00	00	85	00	00	00	86	00	00	00	87	00	00	00		09	00	00	00	12	00	00	00	24	00	00	00	49	00	00	00
0000000220	88	00	00	00	89	00	00	00	8A	00	00	00	88	00	00	00		92	00	00	00	24	01	00	00	49	02	00	00	92	04	00	00
0000000230	8C	00	00	00	8D	00	00	00	8E	00	00	00	8F	00	00	00	ч.	24	09	00	00	49	12	00	00	92	24	00	00	24	49	00	00
			64	-bit	head	ler_														6	-bit	head	er										

### Figure 3-3 Example Test data in sector#0/#1 by increment/LFSR pattern

Test data of each sector has different 64-bit header. 64-bit header consists of 48-bit LBA address and 16-bit zero value. 48-bit LBA address is unique value for each sector. The data after 64-bit header is the test pattern which is selected by user. The example of test pattern is shown in Figure 3-3. 32-bit increment pattern is shown in the left window while 32-bit LFSR pattern is shown in the right window.



Figure 3-4 – Figure 3-6 show the error message when user input is invalid. "Invalid input" message is displayed on the console and then returns to main menu to receive new command.

COM19 - Tera Term VT
File Edit Setup Control Window Help
+++ Write Command selected +++ Out-of-range LBA address
Enter Start LBA : Ø - Øx3B9E12AF => Øx3B9E12BØ
Invalid input Error message
--- Main menu [Ver = 1.5] ---[Ø] : Identify Command
[11] : Write Command
[21] : Read Command
[22] : Read Command
[9] : Re-Initial System

Figure 3-4 Invalid Start LBA input



Figure 3-5 Invalid Sector count input

🧧 COM19 - Tera Tern	n VT			- • •
File Edit Setup (	Control Window	Help		
+++ Write Comma Enter Start LBA Enter Sector Co Selected Patter Invalid input E Main menu [ [0] : Identify [1] : Write Com [2] : Read Comm [9] : Re-Initia	nd selected + : 0 - 0x3 unt : 1 - 0x3 n [0]Inc32 [1 rror message Ver = 1.5] Command mand and 1 System	+++ B9E12AF => B9E12BØ => IDec32 [2]A	0 0x4000000 111_0 [3]A11_	Out-of-range pattern _1 [4]LFSR=>5

Figure 3-6 Invalid Test pattern input



#### 3.3 Read Command

Select '2' to send Read command to NVMe SSD. Three inputs are required for this menu.

- 1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
- 2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
- 3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with the test pattern using in Write Command menu. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

🕘 COM27 - Tera Term VT	X
<u>File Edit Setup Control Window H</u> elp	
<pre>+++ Read Command selected +++ Enter Start LBA : 0 - 0x3B9E12AF =&gt; 0 Input from user Enter Sector Count : 1 - 0x3B9E12B0 =&gt; 0x4000000 Selected Pattern [0]Inc32 [1]Dec32 [2]All_0 [3]All_1 [4]LFSR=&gt; 4 3.262 GB 6.527 GB 9.790 GB 13.056 GB 16.318 GB 19.580 GB 22.845 GB 26.111 GB</pre>	*
32.641 GB Output performance	
Total = 34[GB] , Time = 10526[ms] , Transfer speed = 3231[MB/s]	
Main menu [Ver = 1.5] [0] : Identify Command [1] : Write Command [2] : Read Command [9] : Re-Initial System	•

Figure 3-7 Input and result of Read Command menu

Similar to Write Command menu, if all inputs are valid, test system will read data from SSD. Test performance, total size, and total time usage are displayed after end of transfer. "Invalid input" will be displayed if some inputs are out-of-range.





Figure 3-8 Data verification is failed but wait until read complete



Figure 3-9 Data verification is failed and press any key to cancel operation

Figure 3-8 and Figure 3-9 show error message when data verification is failed. "Verify fail" is displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete.

If read process is completed, output performance from read process will be displayed.

In case of cancel operation, the previous command does not complete in good sequence. It is recommended to run menu [9] to restart system.



#### 3.4 Re-initialize System

Select '9' to re-initialize system. This menu is applied to reset system or change device number on PCIe switch. The step to re-initialize is as follows.

1) The step to reset system is displayed on the console.



2) User press FPGA RESET on FPGA board and PCIe RESET on FMC-to-PCIe card, as shown in Figure 3-11.





Figure 3-11 Press Reset SW



3) Press any keys to start PCIe initialization. The sequence after this step is same as Figure 2-11.

💐 COM27 - Tera Term VT <u>File Edit Setup Control Window</u> Help +++ Re-Initialize System selected +++ Press any key after press reset both FMC-PCIe card and FPGA board Waiting PCIe Linkup Waiting IP initialization Select PCIe Switch PCIe Gen3 Device Detect Select PCIe Switch Select PCIe device mode [0]Direct NUMe [1]Through PCIe Switch=>1 Input device no. of NUMe SSD: 0 - 31 =>10 Select new device no. Start PCIe initialization Complete PCIe initialization Main menu [Ver = 1.5] -User sends new command to test [0] : Identify Command new SSD, connected to different [1] : Write Command [2] : Read Command channel on PCIe switch card . [9] : Re-Initialize System

Figure 3-12 Re-Initialize process



dg\_nvmeip\_pldapcie\_sw\_instruction\_en.doc **4 Revision History** 

Revision	Date	Description
1.0	30-Jan-19	Initial version release