NVMe-IP for PLDA PCIe (PCIe Switch) Demo Instruction

Rev1.0 30-Jan-19

This document describes the instruction to run NVMe-IP for PLDA demo on FPGA development board by connecting SSD through PCIe switch instead of directly connection with SSD. FMC-PCIe adapter card and PCIe switch card with M.2 connector are applied in the demo. The demo is designed to write/verify data one SSD through PCIe switch. Though 4 M.2 NVMe SSD are connected to PCIe switch card, user could select to operate with one SSD. User controls test operation and selects active SSD through Serial console.

1 Environment Requirement

To run the demo on FPGA development board, please prepare following environment.

1) FPGA Development board: ZCU102
2) PC installing Xilinx programmer software (Vivado) and Serial console software such as HyperTerminal
3) Xilinx Power adapter for FPGA board
4) FMC to PCIe card
5) ATX power supply for FMC-to-PCIe card
6) a) PCIe switch card with M.2 connector + M.2 NVMe SSD connecting to PCIe switch
   b) PCIe NVMe SSD or PCIe-M.2 adapter card with M.2 SSD
7) Two micro USB cables for programming FPGA and Serial console, connecting between FPGA board and PC

Note:
[1] FMC to PCIe adapter card: HTG-FMC-PCIE board
http://www.hitechglobal.com/fmcmodules/fmc_pciexpress.htm
[2] PCIe switch card with M.2 connector: Quattro 400 M.2 NVMe SSD Adapter
http://www.aplicata.com/quattro-400/

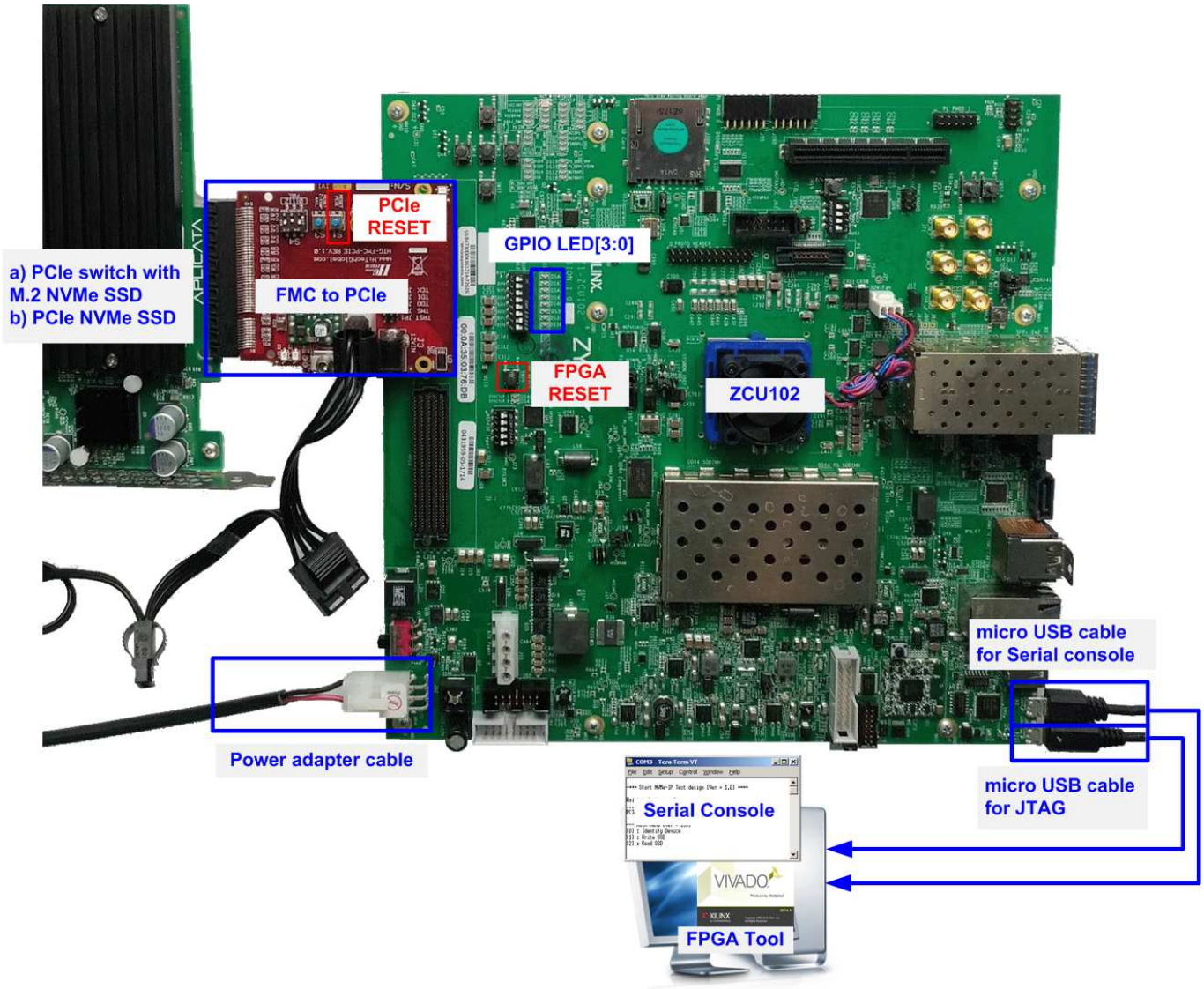

Figure 1-1 NVMe-IP for PLDA PCIe (PCIe Switch) demo on ZCU102

2 Demo setup

1) Power off system.
2) Connect FMC-to-PCIe card to HPC1 connector (J4) on ZCU102, as shown in Figure 2-1.

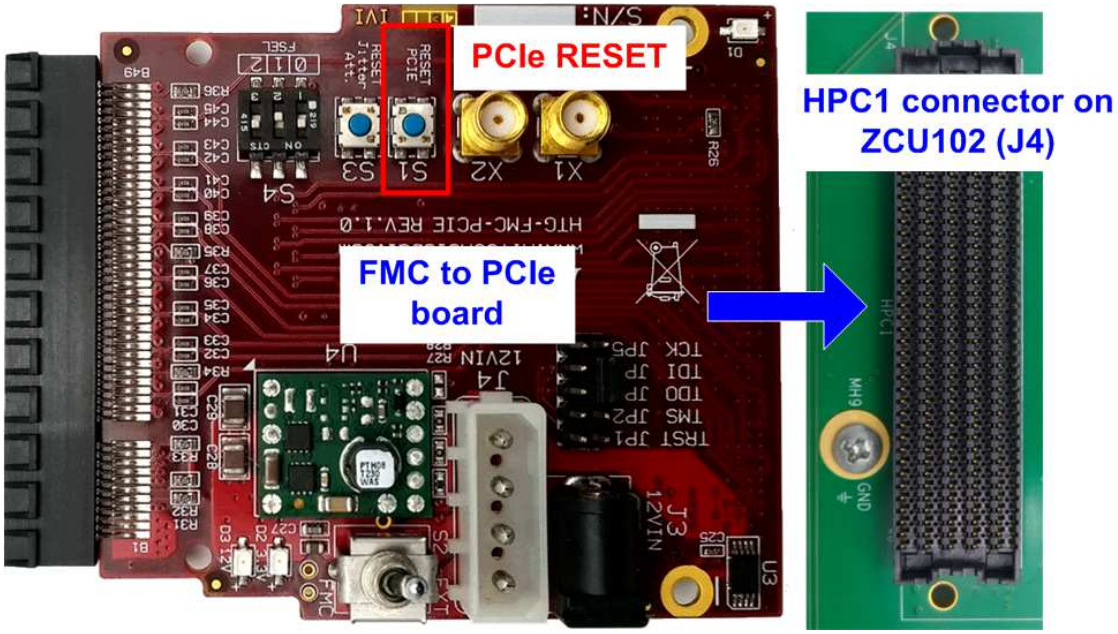

Figure 2-1 Connect FMC to PCIe board to FPGA board

3) Connect ATX power cable to J4 on FMC-to-PCIe card and select power source of FMC (S2) to Ext (external power), as shown in Figure 2-2

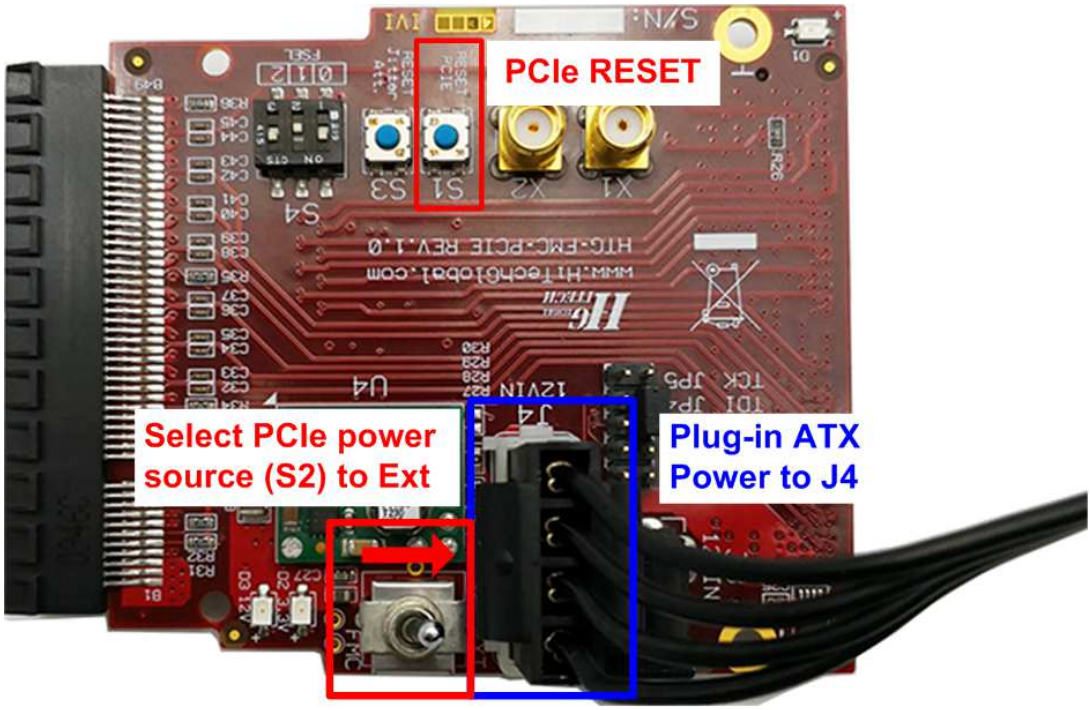

Figure 2-2 Set up power on FMC-to-PCIe card

4) Connect at least 1 NVMe SSD to PCIe switch card. In the example, four SSDs are connected to show different device number usage from different connector. As shown in Figure 2-3, each connector is defined as different device number depending on PCIe switch schematic. The details of device number for each M.2 connector on reference board are shown in Figure 2-3. After that, install heat sink to cool down NVMe SSD on PCIe switch card.

Figure 2-3 Connect NVMe SSD to PCIe switch

5) Connect PCIe switch card to PCIe female connector on FMC-to-PCIe card.

Figure 2-4 Connect PCIe switch card to FMC-to-PCIe card

6) Connect two micro USB cables between FPGA board and PC for FPGA programming and Serial console, as shown in Figure 2-5.

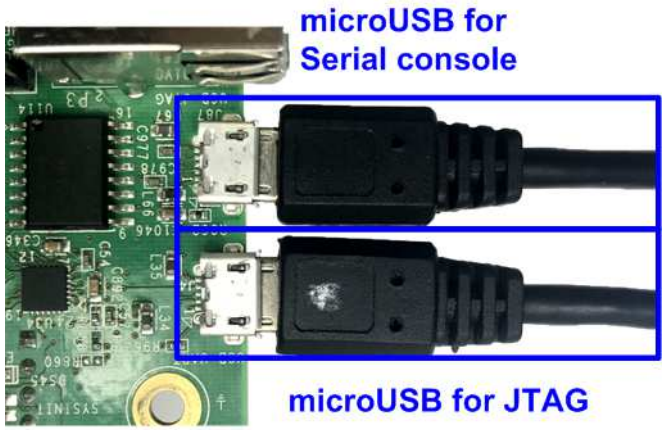

Figure 2-5 USB cable connection

7) Turn on ATX power supply for FMC-to-PCIe card power and FPGA development board, as shown in Figure 2-6.

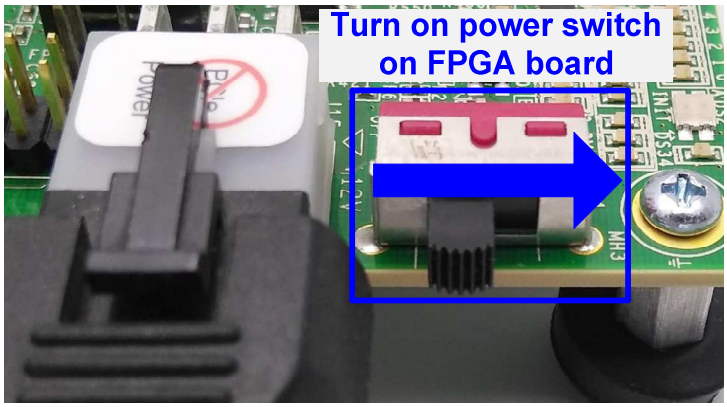

Figure 2-6 Turn on power switch

8) Open Serial console. When connecting ZCU102 board to PC, there are four COM ports displayed on Device Manager. Use COM port number of Interface0 (COM15 in Figure 2-7) for Serial console.

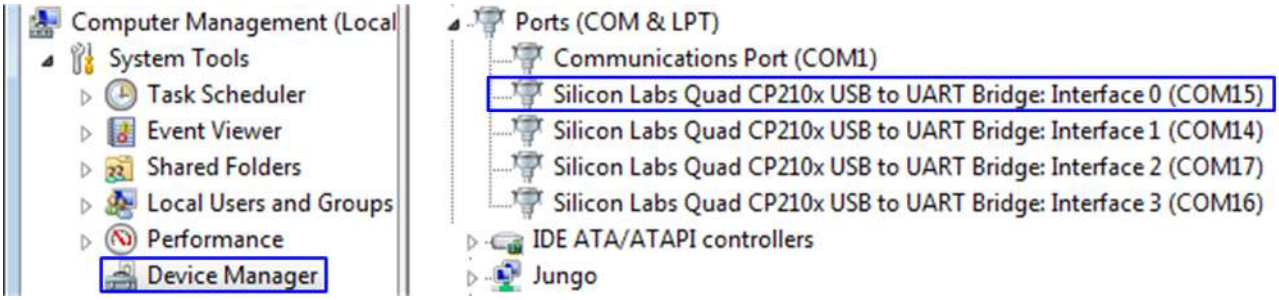

Figure 2-7 Two COM ports from FPGA connection

9) Download and program configuration file and firmware to FPGA board. Open Vivado TCL shell and change directory to download folder which includes demo configuration file. Type “NVMeXR1IPTest_zcu102.bat”, as shown in Figure 2-8.

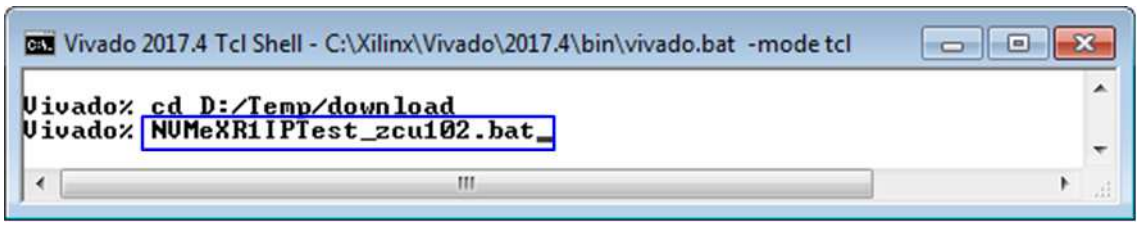

Figure 2-8 Programmed by Vivado

10) Check LED status on FPGA board. The description of LED is as follows.

GPIO LED	ON	OFF
0	Normal operation	SSD is not good status or reset button is pressed
1	System is busy	Idle status
2	IP Error detect	Normal operation
3	Data verification fail	Normal operation

Table 2-1 LED Definition

11) After programming complete, LED[0] and LED[1] are ON during PCIe initialization process. NVMe SSD could be connected to FMC-to-PCIe card by two methods. First method is connecting to FMC-to-PCIe card directly. Second method is connecting to FMC-to-PCIe card through PCIe switch card.

a) When NVMe SSD is connected to FMC-to-PCIe card directly, the step is as follows.
   (1) "Waiting PCIe Linkkup" and "PCIe Genx Device Detect" are displayed to the console.
   (2) User inputs '0' to select the connection to be direct connection.
   (3) "Complete PCIe initialization" is displayed when IP completes the initialization sequence.
   (4) LED[1] changes to OFF and Main menu is displayed to receive command from user.

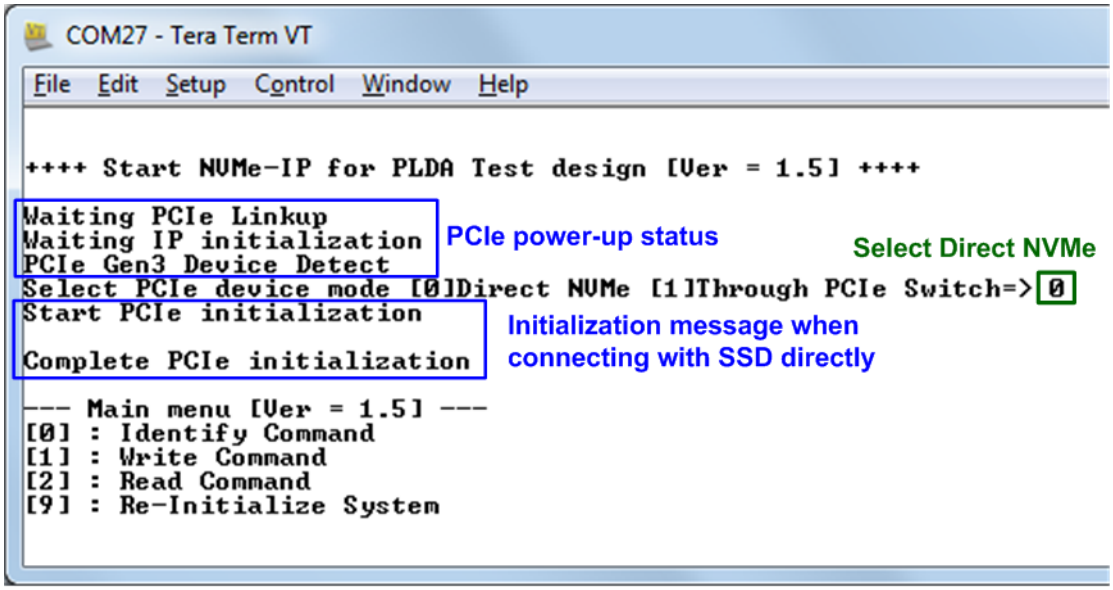

Figure 2-9 Direct NVMe SSD initialization

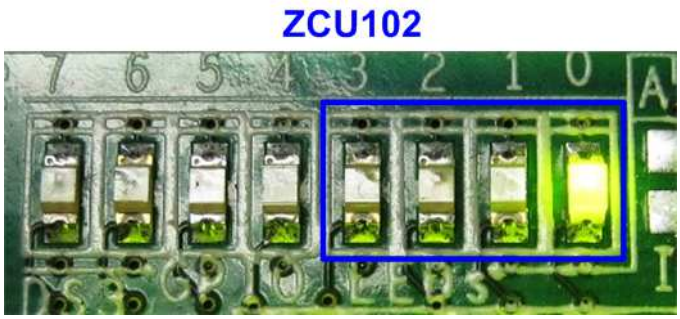

Figure 2-10 LED status after complete initialization sequence

b) When NVMe SSD is connected to PCIe switch card, so FMC-to-PCIe card detects PCIe switch firstly, not NVMe SSD. The step to complete initialization sequence is as follows.
   (1) "Waiting PCIe Linkup" is displayed.
   (2) User needs to press S1 on FMC-to-PCIe card (PCIe RESET) to reset PCIe switch and SSD.
   (3) "PCIe GenX Device Detect" is displayed.
   (4) User inputs '1' and selects device number to test. Figure 2-3 shows device number position of each M.2 slot on PCIe switch card.
   (5) "Complete PCIe initialization" is displayed when IP completes the initialization sequence.
   (6) LED[1] changes to OFF and Main menu is displayed to receive command from user.

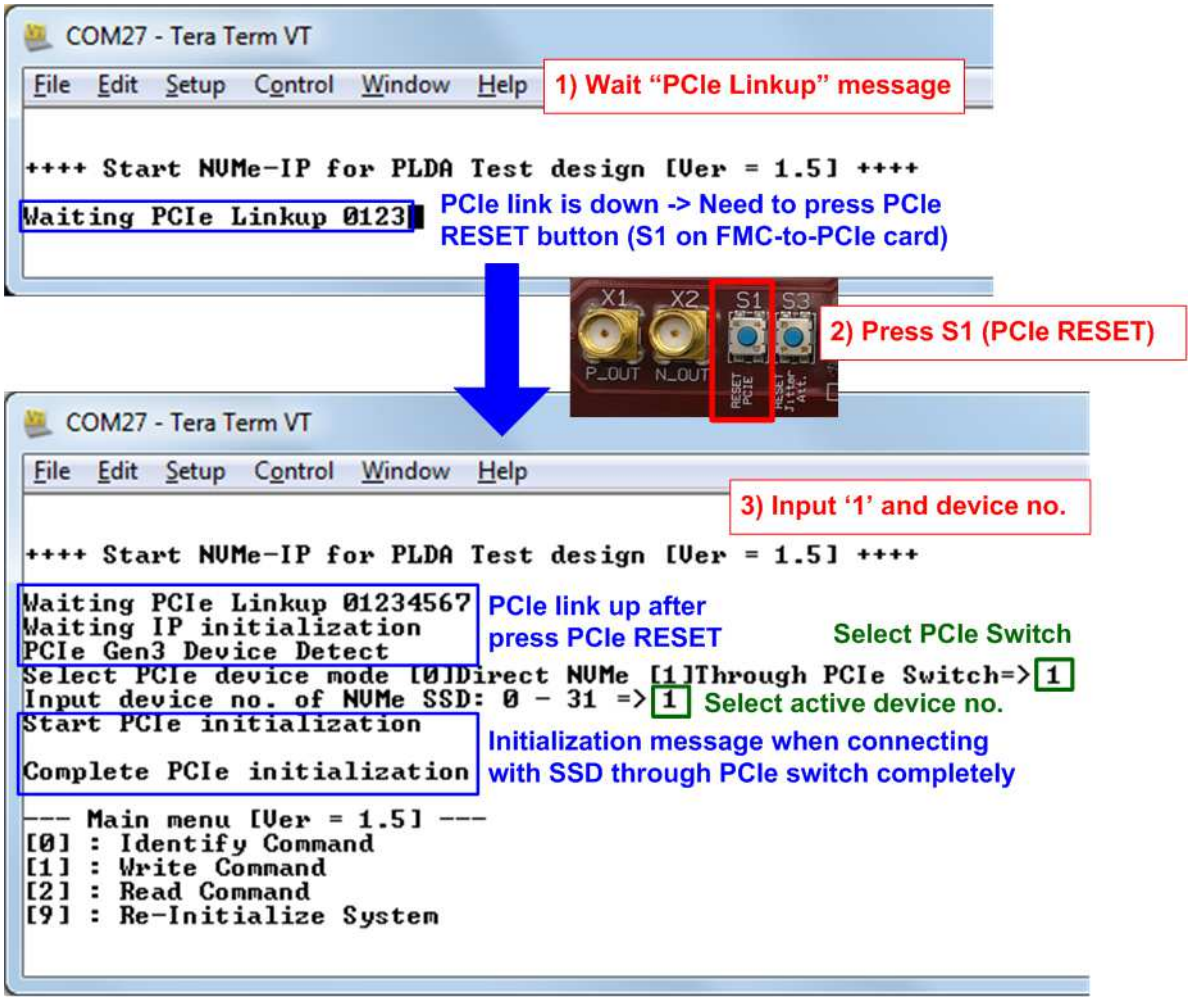

Figure 2-11 NVMe SSD through PCIe switch initialization

3 Test Menu

3.1 Identify Command

Select '0' to send Identify command to NVMe SSD. When operation is completed, SSD information is displayed on the console, i.e.
1) SSD model number
2) SSD capacity which is output from NVMe-IP.

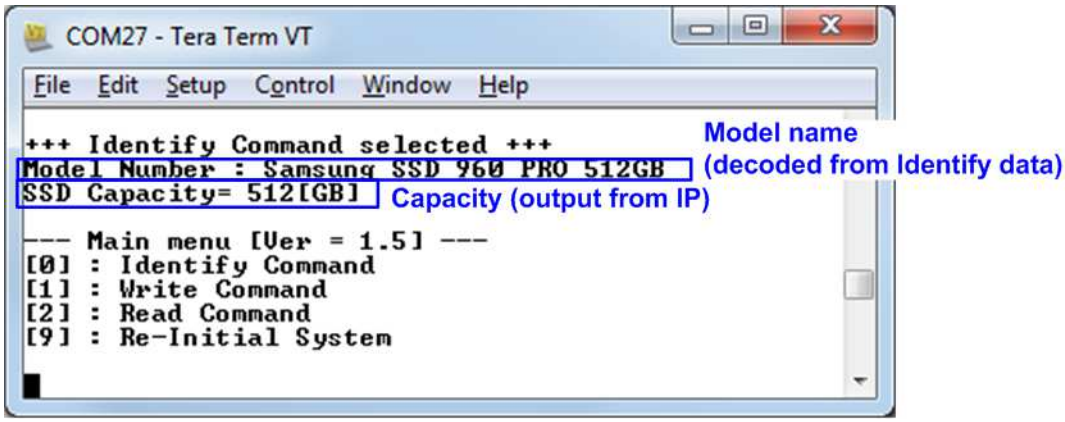

Figure 3-1 Result from Identify Device menu

3.2 Write Command

Select '1' to send Write command to NVMe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
3) Test pattern: Select test pattern to write test data to SSD. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, current transfer size is displayed on the console to show that system still run. Finally, test performance, total size, and total time usage are displayed on the console as test result.

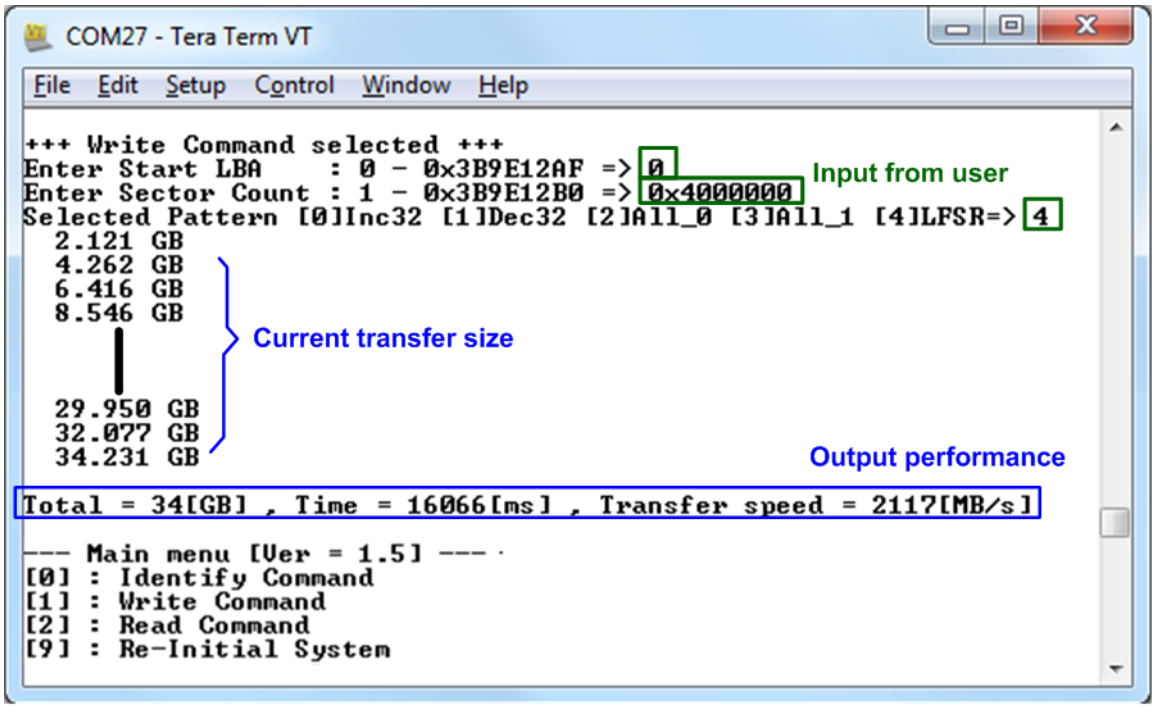

Figure 3-2 Input and result of Write Command menu

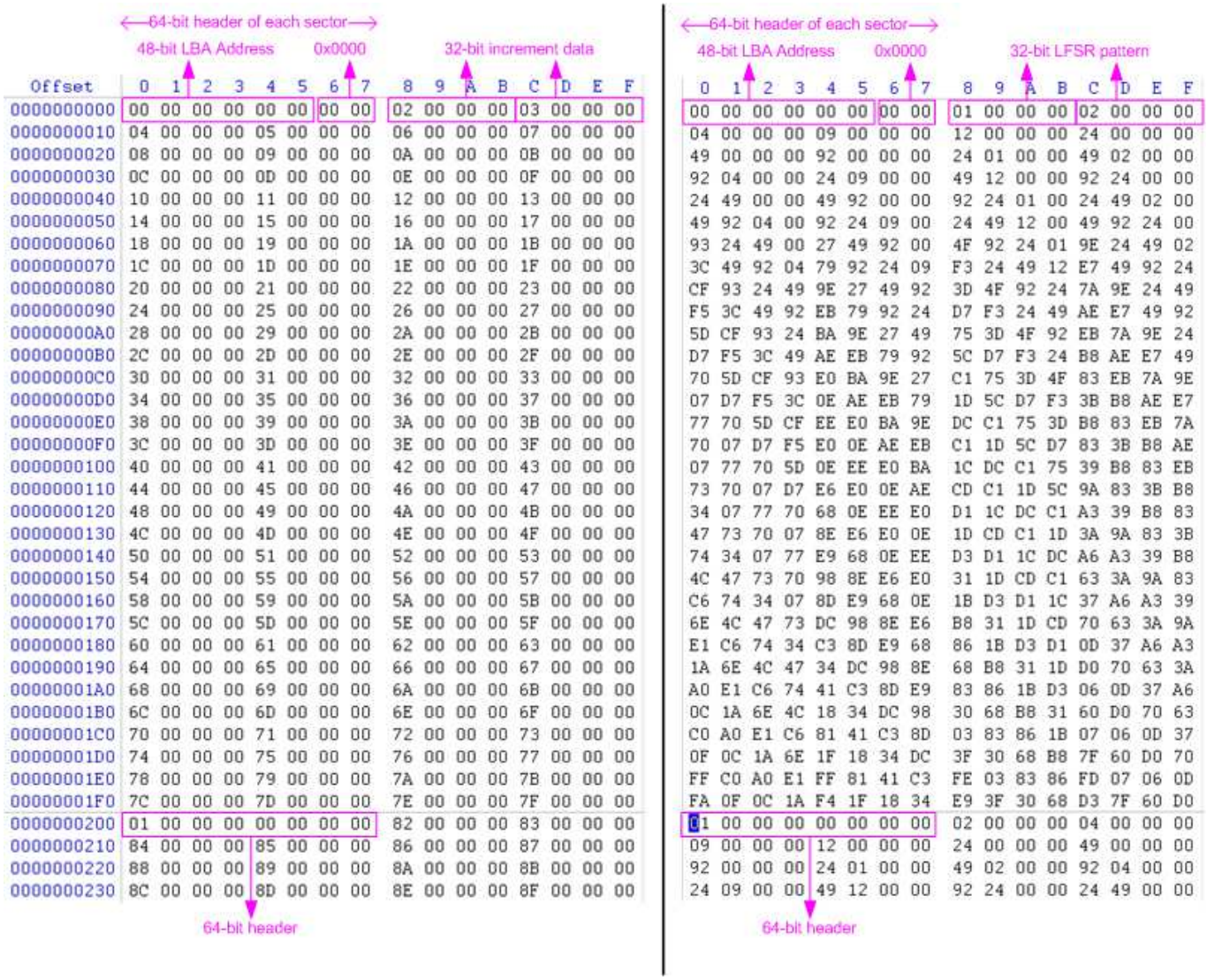

Figure 3-3 Example Test data in sector#0/#1 by increment/LFSR pattern

Test data of each sector has different 64-bit header. 64-bit header consists of 48-bit LBA address and 16-bit zero value. 48-bit LBA address is unique value for each sector. The data after 64-bit header is the test pattern which is selected by user. The example of test pattern is shown in Figure 3-3. 32-bit increment pattern is shown in the left window while 32-bit LFSR pattern is shown in the right window.

Figure 3-4 – Figure 3-6 show the error message when user input is invalid. “Invalid input” message is displayed on the console and then returns to main menu to receive new command.

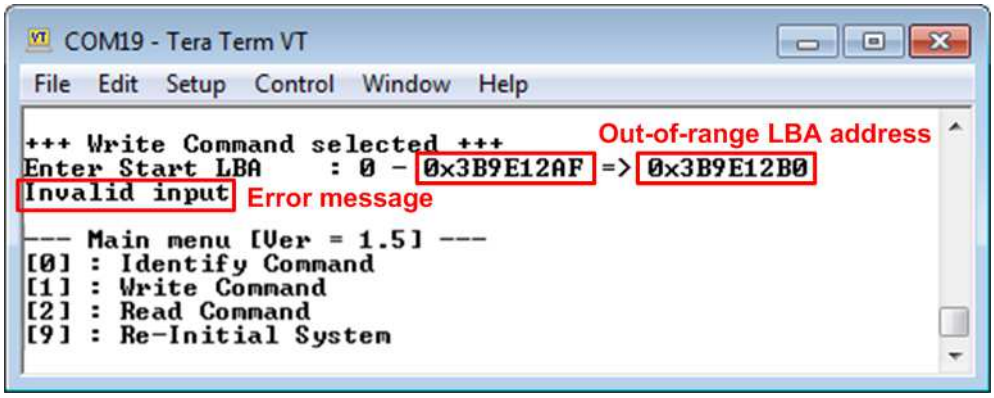

Figure 3-4 Invalid Start LBA input

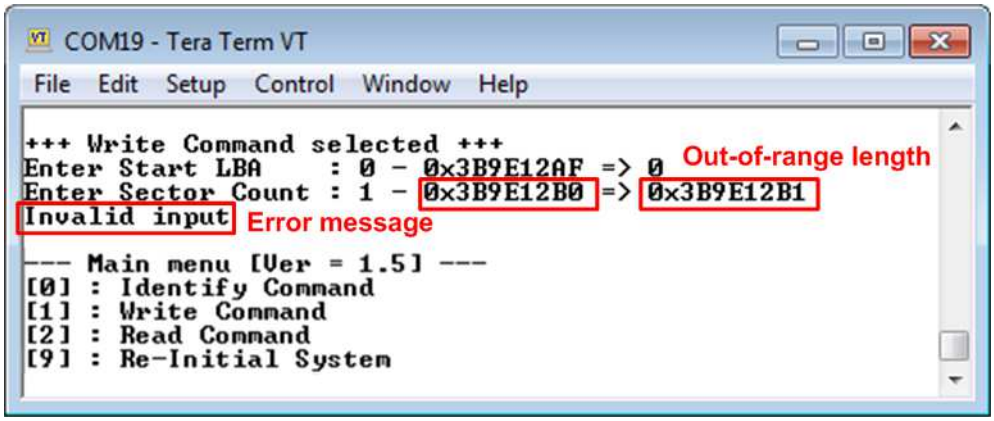

Figure 3-5 Invalid Sector count input

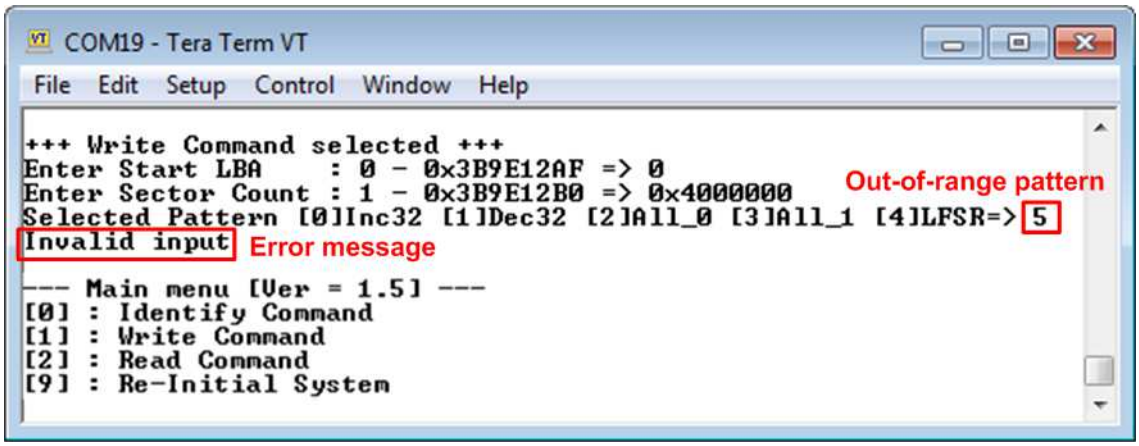

Figure 3-6 Invalid Test pattern input

3.3 Read Command

Select '2' to send Read command to NVMe SSD. Three inputs are required for this menu.

1) Start LBA: Input start address of SSD in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit.
3) Test pattern: Select test pattern to verify data from SSD. Test pattern must be matched with the test pattern using in Write Command menu. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

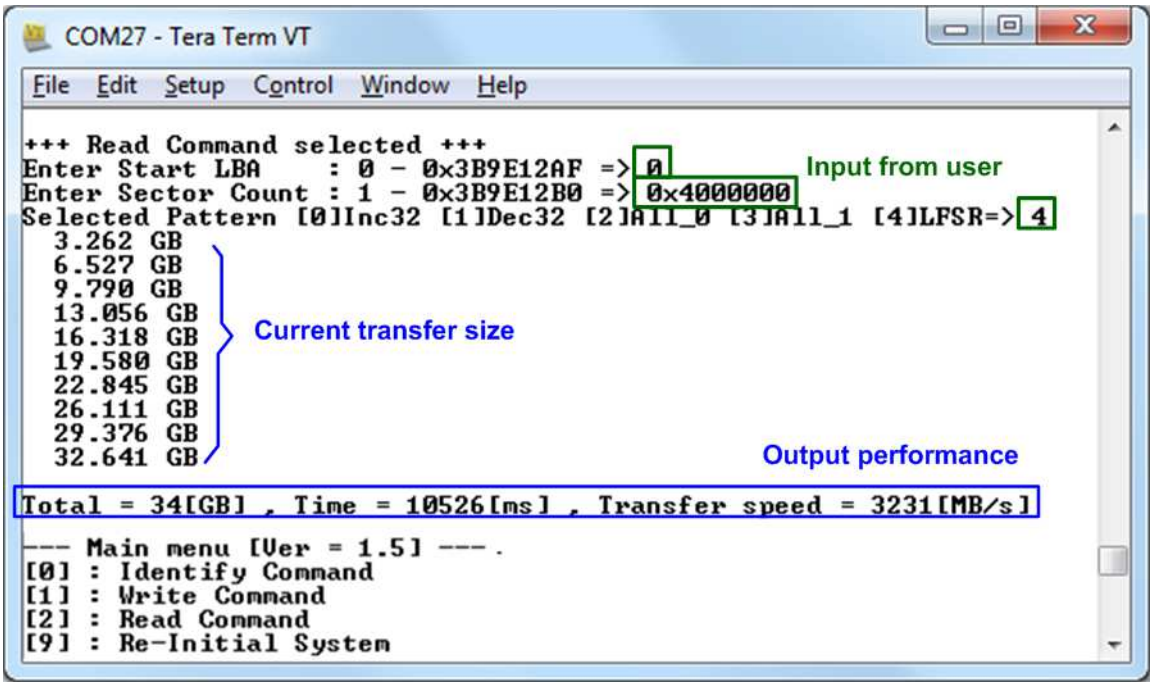

Figure 3-7 Input and result of Read Command menu

Similar to Write Command menu, if all inputs are valid, test system will read data from SSD. Test performance, total size, and total time usage are displayed after end of transfer. "Invalid input" will be displayed if some inputs are out-of-range.

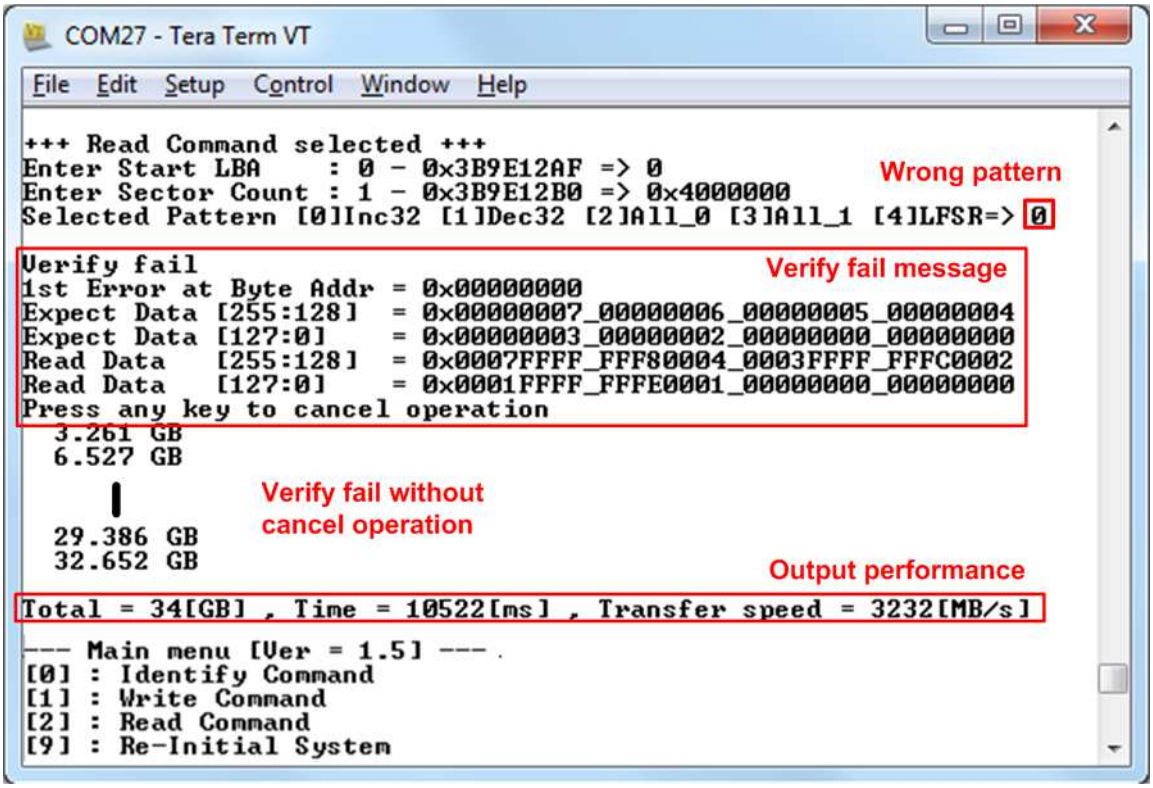

Figure 3-8 Data verification is failed but wait until read complete

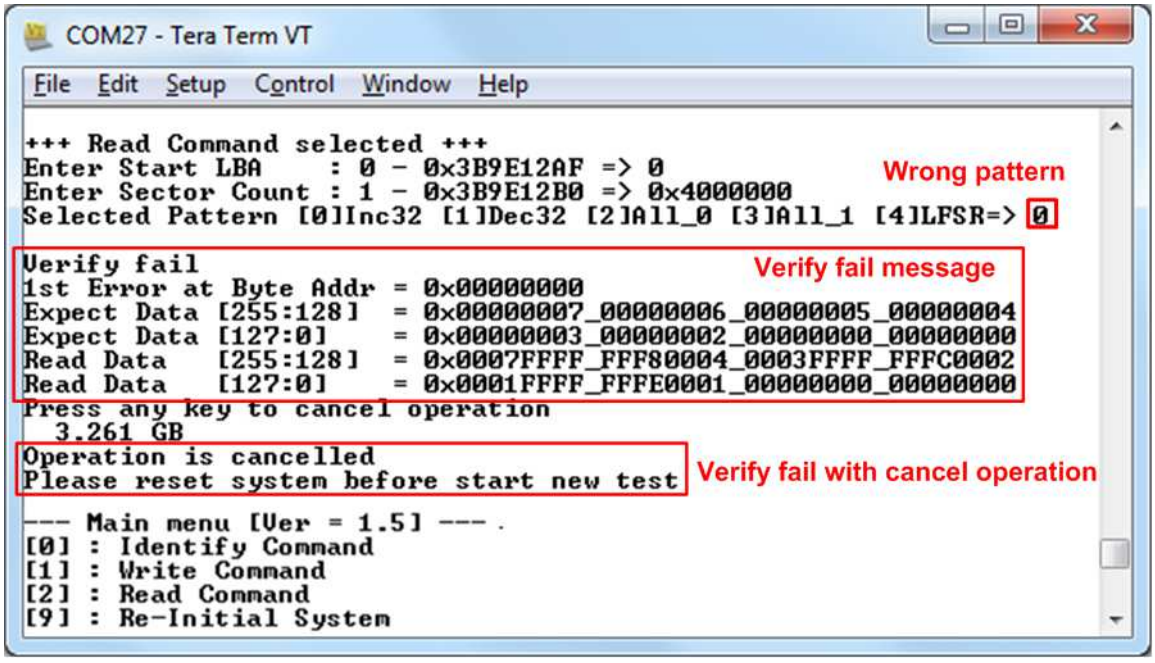

Figure 3-9 Data verification is failed and press any key to cancel operation

Figure 3-8 and Figure 3-9 show error message when data verification is failed. “Verify fail” is displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete.
If read process is completed, output performance from read process will be displayed.

In case of cancel operation, the previous command does not complete in good sequence. It is recommended to run menu [9] to restart system.

3.4 Re-initialize System

Select '9' to re-initialize system. This menu is applied to reset system or change device number on PCIe switch. The step to re-initialize is as follows.

1) The step to reset system is displayed on the console.

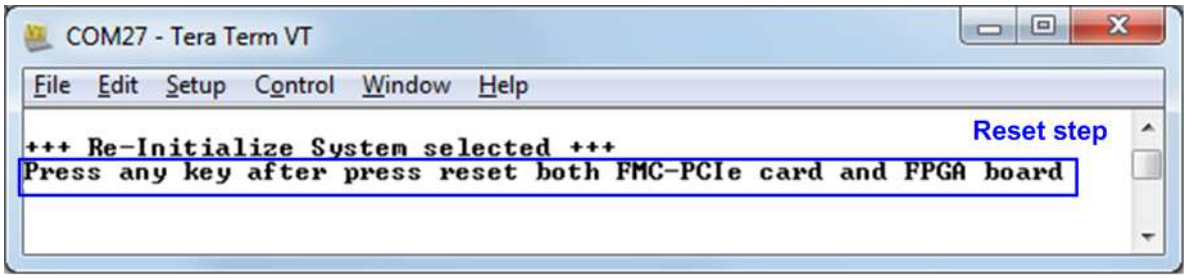

Figure 3-10 Re-Initialize system

2) User press FPGA RESET on FPGA board and PCIe RESET on FMC-to-PCIe card, as shown in Figure 3-11.

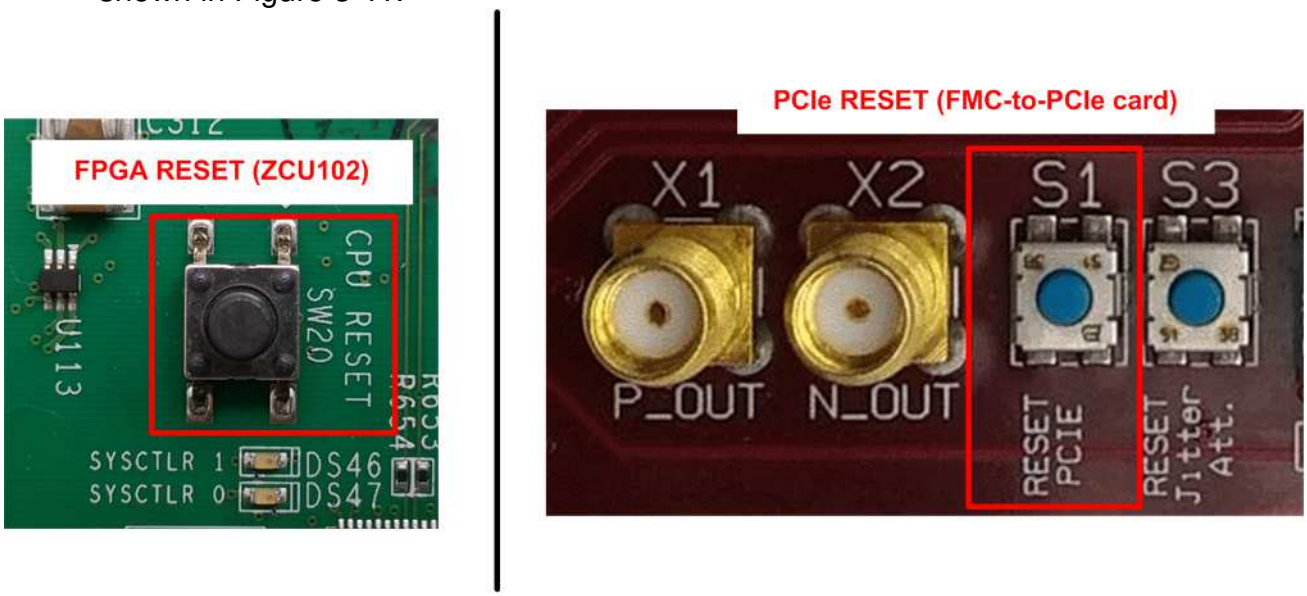

Figure 3-11 Press Reset SW

3) Press any keys to start PCIe initialization. The sequence after this step is same as Figure 2-11.

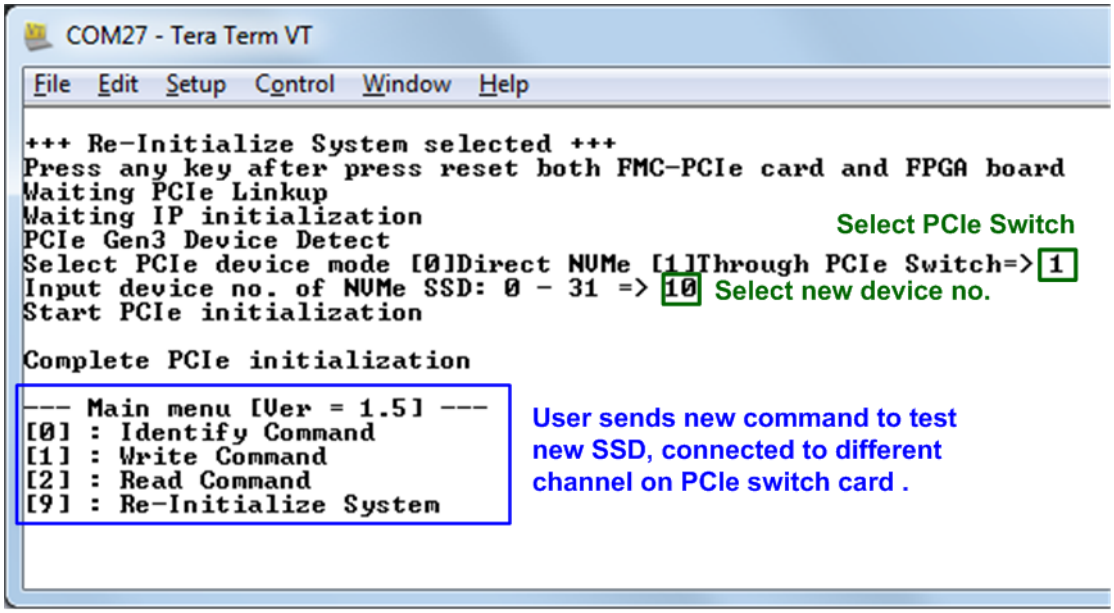

Figure 3-12 Re-Initialize process

4 Revision History

Revision	Date	Description
1.0	30-Jan-19	Initial version release