

# SATA Host-IP Demo Instruction

Rev1.2 15-Nov-17

This document describes the instruction to run SATA Host-IP demo on FPGA development board and AB09-FMCRAID/AB12-HSMCRAID adapter board. The demo is designed to write and verify data with SATA-III device. User can control test operation through NiosII command shell.

#### **1** Environment Requirement

To demo SATA Host-IP on IntelFPGA board, please prepare the following hardware/software.

- 1) IntelFPGA board:
  - ArriaV GX Starter board
  - Arria10 SoC Development board
  - Alaric board from Reflex
- 2) PC with QuartusII programmer and NiosII command shell software
- 3) SATA adapter board
  - a) For Arria10 SoC board/Alaric board: AB09-FMCRAID
  - b) For ArriaV GX board: AB12-HSMCRAID
- 4) SATA-III device
- 5) Power adapter for FPGA board and ATX power supply for SSD
- 6) A cable for programming FPGA and NiosII command shell connecting between FPGA board and PC,
  - a) For Arria10 SoC/Alaric board: use micro USB cable
  - b) For ArriaV GX Starter board: use USB A-B cable

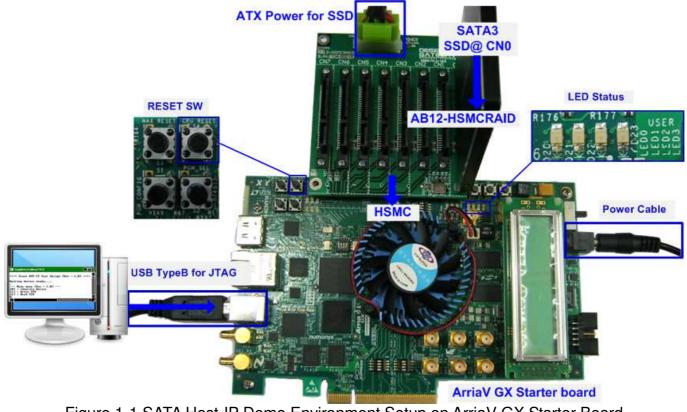






Figure 1-2 SATA Host-IP Demo Environment Setup on Arria10 SoC Development Board

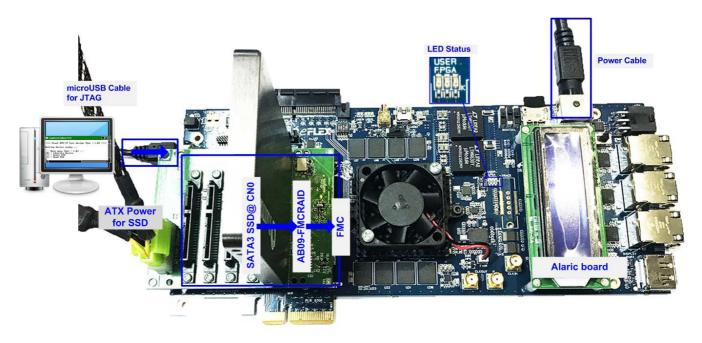


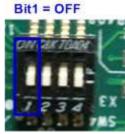
Figure 1-3 SATA Host-IP Demo Environment Setup on Alaric board

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### 2 Demo setup

- 1) Power off system.
- 2) Setup board option.
  - a) For ArriaV GX Starter board only, set bit1 of SW4 to OFF position.



#### Figure 2-1 Set SW to select clock input for ArriaV GX Starter board

- 3) Setup RAID adapter board.
  - i. For Arria 10 SoC Development board/Alaric board: Connect AB09-FMCRAID to FMC#A

For ArriaV GX Starter board: Connect AB12-HSMCRAID to HSMC

- ii. Connect SATA-III device to CN0 on AB09/AB12.
- iii. Connect power to power connector on AB09/AB12

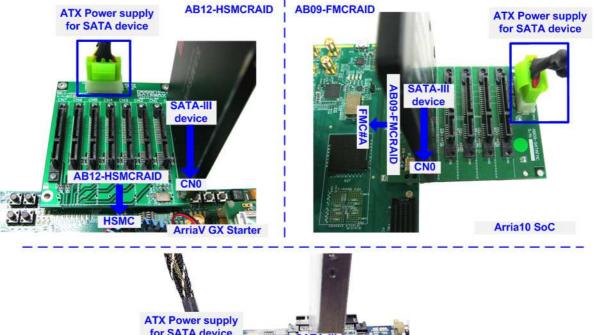




Figure 2-2 AB09/AB12 connection to FPGA board



4) Connect USB Type A or micro USB cable from FPGA board to PC for JTAG programming and JTAG UART.



Figure 2-3 USB cable for JTAG connection

- 5) Power on FPGA development board and power supply for SATA device.
- 6) Open "Clock Control" application to program 150 MHz clock for Intel board.
  - a) For ArriaV GX Starter board only, select 1<sup>st</sup> tab (U4), set CLK0 frequency = 150 MHz, and click "Set New Frequency" button.

\land Clock Contro	I			
U4 X1				
F_vco	: 000MHz			
Registers	1	Fre	quency (MHz)	Disable all 📃
CLK0	-	CLK0	150.00	Disable CLK0 📄
CLK1	-	CLK1	150.00	Disable CLK1 📃
	-	CLK2	150.00	Disable CLK2 📃
CLK3	-	CLK3	150.00	Disable CLK3 📃
	read		Default	Set New Frequency
Messages				
	sterII on lo SPM221002	ocalhos	st (USB-1)	/5M(1270ZF324
Figure 2	-4 Set clock	k freau	ency for A	ArriaV GX board



7) Use QuartusII Programmer to program "HSataIPTest.sof" file, as shown in Figure 2-5.

			127					_
Hardware Setup	USB-Blasterii [USB-1]	Mode:	JTAG		Progress:	100%	6 (Success	ful)
Enable real-time ISP	to allow background programming w	hen availab	ble					
Start	File	De	evice	Checksum	Usercode	Program/ Configure	Verify	Blank Chec
Stop	D:/SATA-IP/HostIP/HSataIPTest.sof	5AGXFB3	H4F35	04979C38	04979C38			
Auto Detect	<none></none>	5M2210Z		0000000	<none></none>			
X Delete	4	111						
Add File								
Change File Save File Add Device	TDI	→ [A1	M2210Z					
Change File Save File Add Device T <sup>ND</sup> Up		→ [A1						
Change File Save File Add Device		→ [A1			€ <u>F</u> ind	💏 Find Ne <u>x</u> i	E	
Change File  Change File  Save File  Add Device  Dup  Dup  Dup  Tup  Tup  Tup  Iu  Constant  Type ID  Constant  Iu  Iu  Iu  Iu  Iu  Iu  Iu  Iu  Iu  I	TDI SAGXFB3H4F35 TDO Control Control Contro	→	A2210Z			💏 Find Ne <u>x</u>	B	
Change File  Change File  Save File  Add Device  Dup  Dup  Dup  Tup  Tup  Tup  Iu  Constant  Type ID  Constant  Iu  Iu  Iu  Iu  Iu  Iu  Iu  Iu  Iu  I	TDI SAGXFB3H4F35 TDO Control Control Contro	→	A2210Z	oct 28 15:3		Find Neg	Ł	

Figure 2-5 Programmed by QuartusII Programmer

8) Open NiosII Command Shell and run nios2-terminal command. Boot message are displayed.

"Waiting device ready" message is displayed during system initialization.

"SATA Gen3 Device Detect" shows SATA speed after complete SATA initialization.

Main menu is displayed to receive command from user.

/cygdrive/c/altera/16.0	
++++ Start SATAHost-IP Test d	esign [Ver = 1.3] ++++
Waiting device ready Wait	SATA Linkup
SATA Gen3 Device Detect SAT/	A Speed = Gen3
Main menu [Ver = 1.3] [0] : Identify Device [1] : Write SSD [2] : Read SSD [3] : Security Erase	Main menu to select operating command
	-
] • [	<b>&gt;</b>

Figure 2-6 NiosII Terminal



9) Check LED status on FPGA board. The description of LED is shown as follows. Note: LED [3] is not available on Alaric board. There are three LEDs on the board.

		Johnhon
GPIO LED	ON	OFF
0	Normal operation	System is in reset condition
1	System is busy	Idle status
2	Error detect	Normal operation
3	Data verification fail	Normal operation

Table 1 LED Definition
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ArriaV Starter Board	Arria10 SoC Board	Alaric Board
	C70 H110 VDD20U3	

Figure 2-7 4-bit LED Status for user output

10)After programming completely, LED[0] and LED[1] are ON during SATA initialization process. LED[1] is OFF after SATA Host-IP completes initialization process and system is ready to receive command from user.

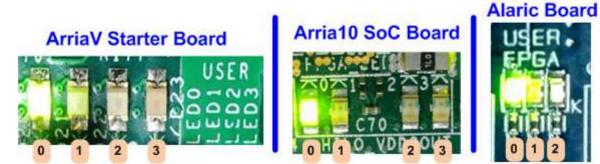


Figure 2-8 LED status after program configuration file and SATA initialization complete



### 3 Test Menu

#### 3.1 Identify Device

Select '0' to send Identify device command to SATA device. When operation is completed, four information are displayed on NiosII command shell, i.e.

- 1) SSD Model number
- 2) Security feature set is supported or not. If not supported, user must not use menu 3 for the test.
- 3) Normal Erase Mode Time: This is estimation time to complete security erase command. Minimum valid value is 2 minutes. This information is displayed when the device can support Security feature set.
- 4) SSD capacity which is output value from SATA Host-IP.

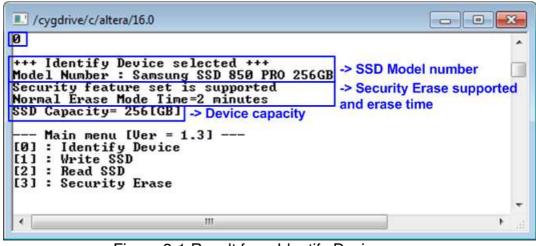


Figure 3-1 Result from Identify Device menu



#### 3.2 Write SSD

Select '1' to send Write command to SATA device. Three inputs are required for this menu. 1) Start LBA: Input start address of SATA device in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit. 2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit. 3) Test pattern: Select test pattern of test data for writing to SATA device. Five types can be

selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

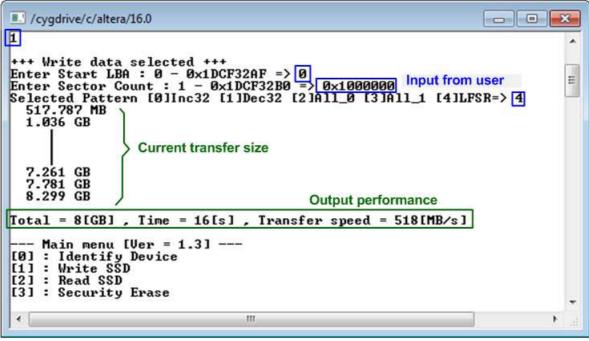


Figure 3-2 Input and result of Write SSD menu

As shown in Figure 3-2, if all inputs are valid, the operation will be started. During writing data, current transfer size is displayed to NiosII command shell to show that system still run. Finally, test performance, total size, and total time usage are displayed on NiosII command shell as test result.



	-	34-61	t hea	der	of ea	ich s	ecto	$\rightarrow$									(	64-b	it hea	ader	of ea	ich s	ecto	$\rightarrow$								
	48	-bit I	BA	Addr	ess		0x00	000		-	2-bi	incr	eme	nt da	ala		48	3-bit	LBA	Addr	ess		0x0	000			32-b	it LF	SR	atte	m	
Offset	0		2	3	4	5	6	7	8	9	4	В	c	AD	E	F	0		4			F	e	47	8	9	4	D		4	÷	F
0000000000	_						-	-	_		00	_	_	_	00		00		-	3	4	5	6	-	01	-	00	B	C	D	E 00	
0000000010	_				_		-			_			-		00		04	-	1.2	00			10.7	100	12				24		and the local data	00
0000000020	10707	0.7050	0.253	12.2		1.1.1	25.65	20.25	100000	1.7.7.1	1202	17.TO	07334	1000	00	100	49	1997		00			100 C	12.1	07377						00	
0000000030	OC	00	00	00	OD	00	00	00	OE	00	00	00	OF	00	00	00	1055	0.00	107055	00		1000	1.5.5	1000	1000	124220	12.20	0.5.5	1.5		00	10.00
0000000040	10	00	00	00	11	00	00	00	12	00	00	00	13	00	00	00				00											02	
0000000050	14	00	00	00	15	00	00	00	16	00	00	00	17	00	00	00	49	92	04	00	92	24	09	00							24	
0000000060	18	00	00	00	19	00	00	00	1A	00	00	00	1B	00	00	00	93	24	49	00	27	49	92	00	4F	92	24	01	9E	24	49	02
0000000070	1C	00	00	00	1D	00	00	00	1E	00	00	00	1F	00	00	00	3C	49	92	04	79	92	24	09	FЗ	24	49	12	E7	49	92	24
0000000080	20	00	00	00	21	00	00	00	22	00	00	00	23	00	00	00	CF	93	24	49	9E	27	49	92	ЗD	4F	92	24	7A	9E	24	49
000000090	24	00	00	00	25	00	00	00	26	00	00	00	27	00	00	00	F5	3C	49	92	EB	79	92	24	D7	F3	24	49	AE	E7	49	92
00000000A0	28	00	00	00	29	00	00	00	2A	00	00	00	2B	00	00	00	5D	CF	93	24	BA	9E	27	49	75	ЗD	4F	92	EB	7A	9E	24
0000000B0	2C	00	00	00	2D	00	00	00	2E	00	00	00	2F	00	00	00	D7	F5	3C	49	AE	EB	79	92	5C	D7	F3	24	B8	AE	E7	49
000000000000000000000000000000000000000					12.75		00	00	32	00	00	00	33	00	00	00				93					C1	75	3D	4F	83	EB	7A	9E
00000000000							00			00	12.7	0.00	12.25	10.01	00		07			3C											AE	E7
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00000000F0	1257	00.21	10.00		1000	0.5.54	0.777	1000			12:25	1.10	12.34	1.527	00	1.5.5	1.000	- 3200		F5	2000	1000	1000								B8	
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0000000110															00		100.77	- 2072	12.770	D7	_										ЗB	
000000120				0.00											00					70											B8	
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0000000140															00					77											39	
0000000150	10705	10000	0.7474	1.7.12.1	0.00	2002	0.000	26.73	125.71	1000	10.00	1997.0	1229124	1000	00	1222	4C		1.1.2	70	2152	10.50	1087		1212	100	122	22.92	0.00	0000	9A	10.000
0000000160	1.			1275	- 5:52		0000	1000	0.020	10.000	12.51	15.50	NEE 1	10101	00	10000				07					07.73	1000	12.2	100	-530	3250	A3	2022
0000000170								00							00					73											3A	
0000000180	1.5.5				~ ~										00					34 47				200	100	1000			2.77		A6 63	
00000001A0	12.2	- 6-51	- 505.5		0.00	1500	0.00	10.50		0.00			522	1000	00	1000			10 m	74	12020		0.000		1.111	1000	1.5		2.22	1257	37	0.255
00000001B0	1.352	1993		1997	12.63	12.5	1999	00	1000			2000	1997		00		1.2.2	0.0	10.00	4C		1.1	1.00		1000	1.			1.1.1.1.1.1.1		70	1012210
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00000001D0	1007	- 3 6		1.5	131.77		1007	00	0.07	10.00	100.74	15.70	10.070	0.772.5	00	1.5.5	1000	- 30.5	1.00	6E	1000		34	1.202	0.000	15157.5	105 510	12.2	563.0	12.22	DO	256
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#### Figure 3-3 Example Test data in sector#0/#1 by increment/LFSR pattern

Test data of each sector has different 64-bit header which consists of 48-bit LBA address and 16-bit all 0 value. 48-bit LBA address is unique value for each sector. After that, the test pattern is filled following user selection such as 32-bit increment pattern (left window of Figure 3-3), 32-bit LFSR pattern (right window of Figure 3-3).



Figure 3-4 – Figure 3-6 shows error message when user input is invalid. "Invalid input" message are displayed on NiosII command shell. Then, it returns to main menu to receive new command.

		Out-of-range LBA address
Enter Start	lata selected +++ : LBA : 0 - 0×1DCF32AF => out Error message	0×20000000
Main me [0] : Ident	nu [Ver = 1.3] ify Device	
[1] : Write [2] : Read	SŠD	
	ity Erase	

Figure 3-4 Invalid Start LBA input

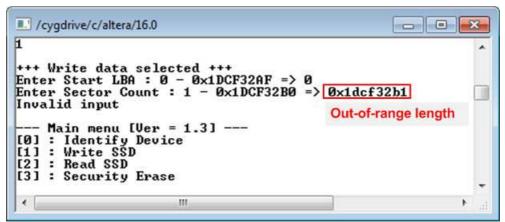


Figure 3-5 Invalid Sector count input

1		
Enter Start L Enter Sector	a selected +++ BA : 0 - 0x1DCF32AF => 0 Count : 1 - 0x1DCF32B0 => 0x1000 ern [0]Inc32 [1]Dec32 [2]All_0 [	000 3]A11_1 [4]LFSR=> 5 Out-of-range pattern
Main menu [0] : Identif [1] : Write S [2] : Read SS [3] : Securit	ŠD D	

Figure 3-6 Invalid Test pattern input

#### 3.3 Read SSD

Select '2' to send Read command to SATA Device. Three inputs are required for this menu. 1) Start LBA: Input start address of SATA Device in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit. 2) Sector Count: Input total transfer size in sector unit. The input is decimal unit when input only digit number. User can add "0x" to be prefix when input is hexadecimal unit. 2) Test pattern: Select test pattern to verify date from SATA Device. Test pattern must be

3) Test pattern: Select test pattern to verify data from SATA Device. Test pattern must be matched with the test pattern which is used during write test. Five types can be selected, i.e. 32-bit increment, 32-bit decrement, all 0, all 1, and 32-bit LFSR counter.

/cygdrive/c/altera/16	.0	
2		
+++ Read data sel Enter Start LBA : Enter Sector Coun Selected Pattern 561.984 MB 1.125 GB	lected +++ : 0 - 0x1DCF32AF => 0 nt : 1 - 0x1DCF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x1000000 Input from u t : 1 - 0x10CF32B0 => 0x10000000 Input from u t : 1 - 0x10CF32B0 => 0x10000000 Input from u t : 1 - 0x10CF32B0 => 0x100000000 Input from u t : 1 - 0x10CF32B0 => 0x100000000 Input from u t : 1 - 0x10CF32B0 => 0x100000000000000000000000000000000000	ser
>	Current transfer size	
7.319 GB		
7.882 GB 8.445 GB	Output performance	
[otal = 8[GB] , ]	<pre>[ime = 15[s] , Transfer speed = 563[MB/s]</pre>	
Main menu [Ue [0] : Identify De [1] : Write SSD [2] : Read SSD [3] : Security Er	evice	
iss - securicy Er	rase	
	III	

Similar to write test if all inputs are valid, the operation will read data from SATA device. Test performance, total size, and total time usage are displayed after end of transfer. "Invalid input" will be displayed if any input value is out-of-range.



Figure 3-8 and Figure 3-9 show the error message when data verification is failed. "Verify fail" message is displayed with error address, expected data, and read data. User can press any key to cancel read operation or wait until all read process complete.

"RESET" button should be pressed to restart the system when user cancel the operation. Note: Alaric board does not have "RESET" button

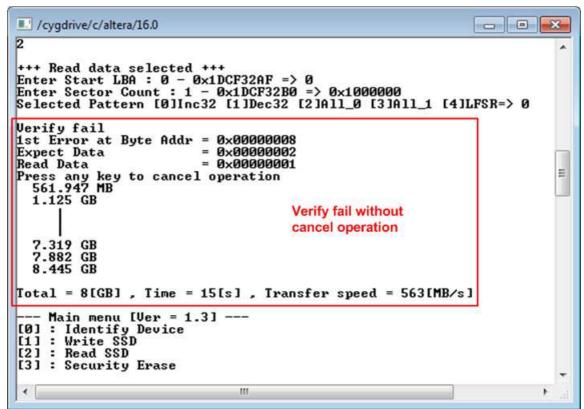


Figure 3-8 Data verification is failed, but wait until read complete

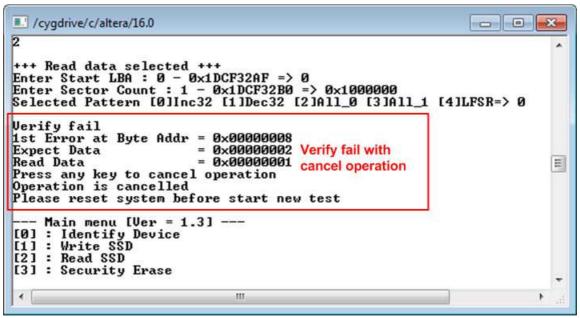


Figure 3-9 Data verification is failed, and press key to cancel operation



#### 3.4 Security Erase

Select '3' to send Security Erase command to SATA Device. Please confirm that SATA device supports Security Erase feature by using Identify device menu. The estimated time of security erase operation is also displayed in Identify device menu.

After selecting the menu, confirmation message is displayed on NiosII command shell. User can input 'y' or 'Y' to continue security erase operation or input other keys to cancel operation.

Number 0-9 is displayed on NiosII command shell every second to show that system still run. After complete the operation, total time usage is displayed as a test result.

Figure 3-11 shows the example when user inputs other keys to cancel the command.

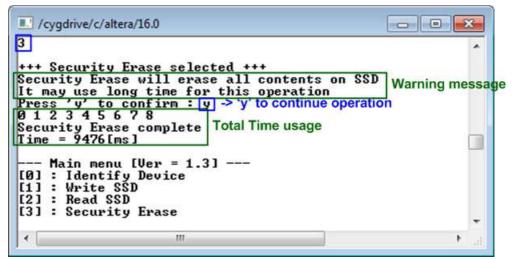


Figure 3-10 Result from Security Erase command

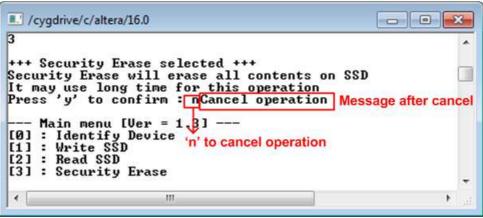


Figure 3-11 Cancel Security Erase command



## 4 Revision History

Revision	Date	Description
1.0	28-Oct-16	Initial version release
1.1	24-Nov-16	Correct security erase menu
1.2	15-Nov-17	Add LFSR pattern and Alaric board