SATA AHCI IP by Baremetal Demo Instruction

Rev1.1 10-Nov-16

This document describes step-by-step to run AHCI-IP demo by using baremetal OS on FPGA board and AB09-FMCRAID board. The host can transfer with SATA-II/III device which supports NCQ command only.

1 Environment Setup

To demo AHCI-IP baremetal OS design, please prepare following hardware.

1) Supported FPGA development board: ZC706/Zynq-Mini-ITX(Z100 model)
2) PC with Xilinx programmer software (iMPACT/Vivado) and Serial console software
3) SATA cable for Zynq Mini-ITX (Z100) or AB09-FMCRAID board for other boards.
4) SATA-II/III device
5) Xilinx Power adapter for Xilinx board or ATX power supply for Zynq Mini-ITX board
6) micro USB cable for programming FPGA between FPGA Development board and PC
7) mini/micro USB cable for Serial console connecting between FPGA board and PC

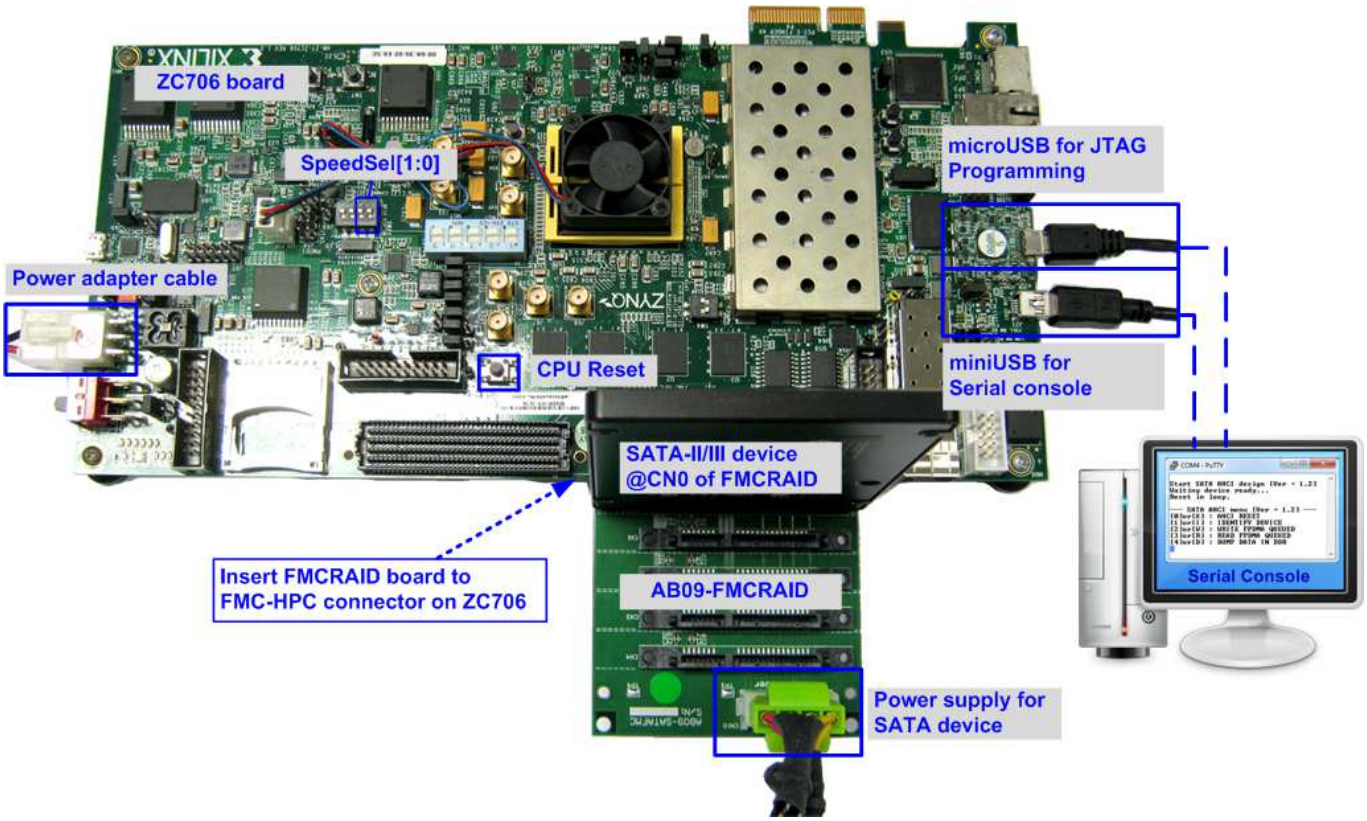

Figure 1-1 SATA AHCI-IP baremetal OS demo environment on ZC706 board

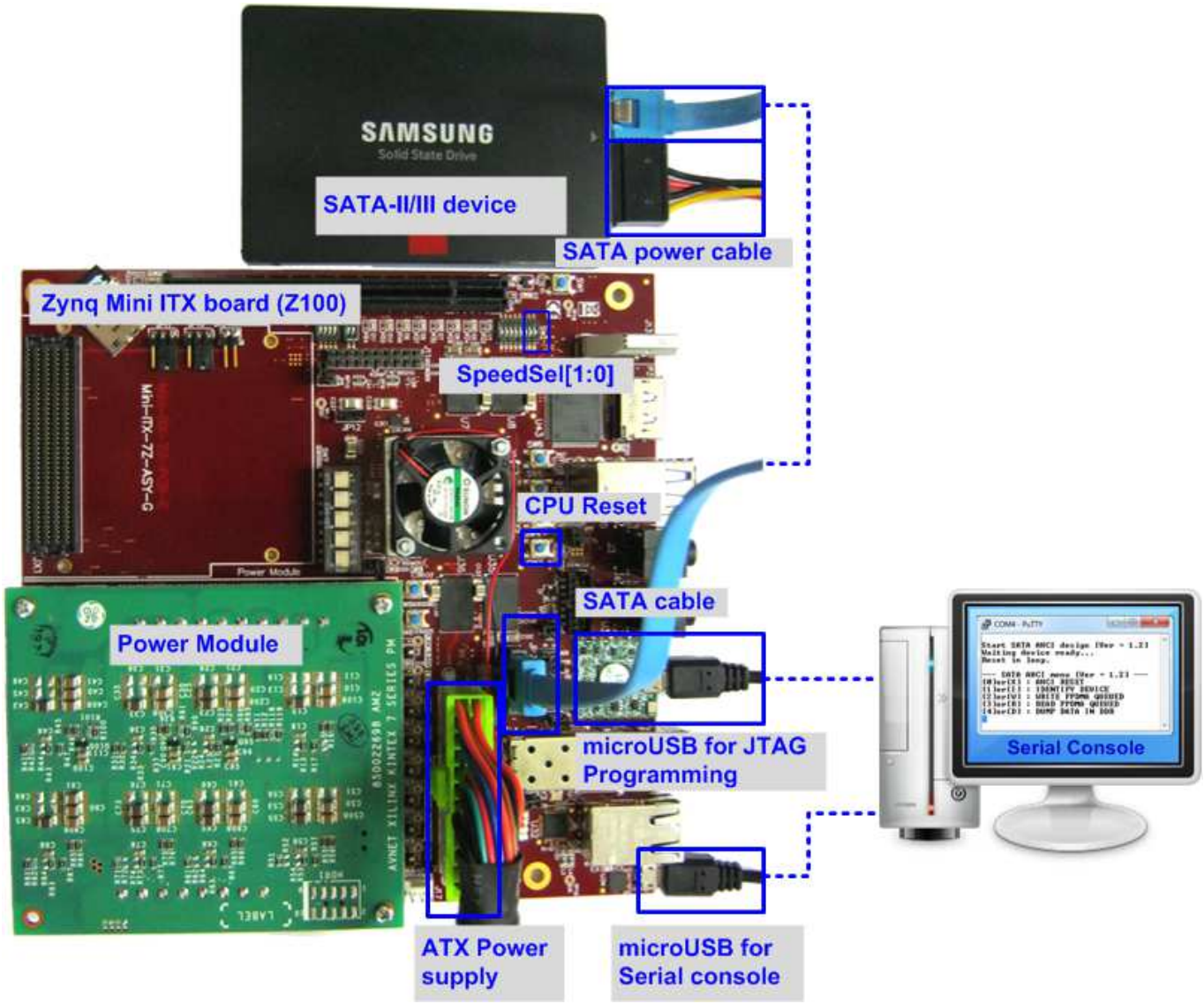

Figure 1-2 SATA AHCI-IP baremetal OS demo environment on Zynq Mini-ITX(Z100) board

2 Demo setup

1) Check all system is power off.
2) Set up board option
   a) For ZC706 board only,
      i. Set SW11=”00000” to configure PS from JTAG, as shown in Figure 2-1.
      ii. Det SW4=”01” to connect JTAG with USB-to-JTAG interface, as shown in Figure 2-2.

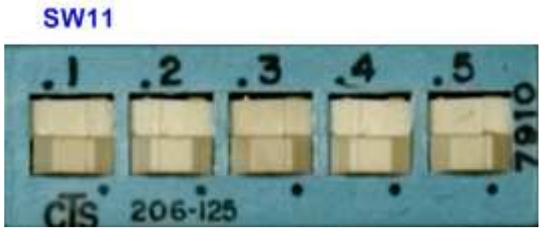

Figure 2-1 SW11 setting to configure PS from JTAG on ZC706 board

Figure 2-2 SW4 setting to use USB-to-JTAG on ZC706 board

   b) For Zynq Mini-ITX board only,
      i. Set SW7="00000" to configure PS from JTAG, as shown in Figure 2-3.
      ii. As shown in Figure 2-4, install a jumper on JP1 pins 1-2 to enable JTAG chain, install the power module onto the board via J8, J9, J10 connectors, and connect ATX power cable to FPGA board via P2 connector.

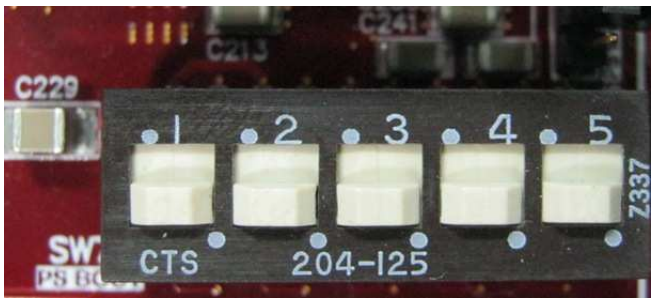

Figure 2-3 SW7 setting to configure PS from JTAG on Zynq Mini-ITX

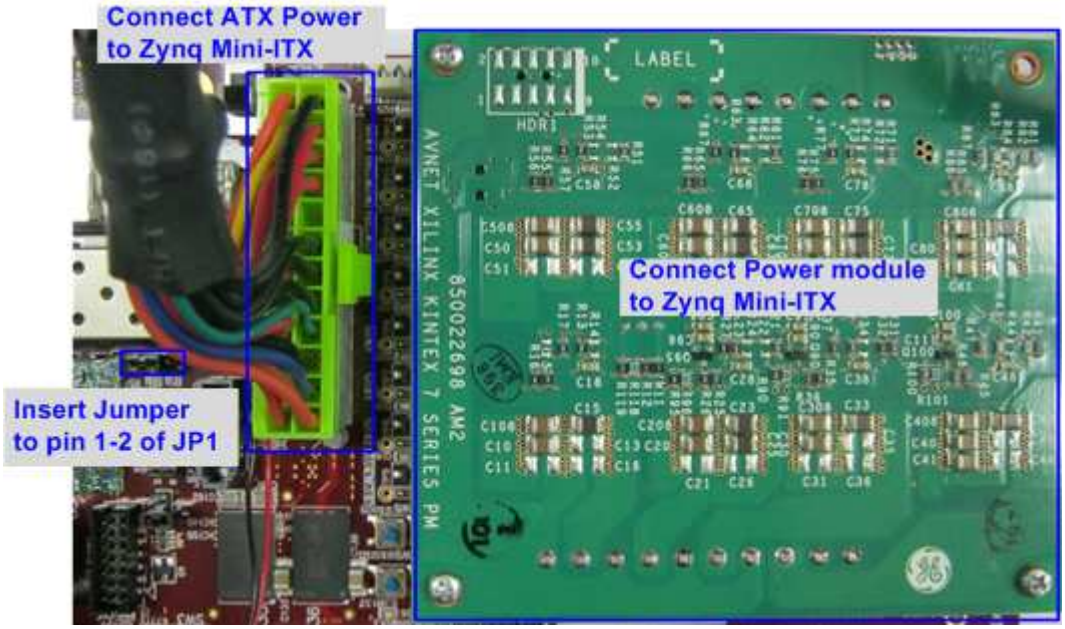

Figure 2-4 The power module installed onto the board

3) Connect the SATA-II/III device to the board by the following steps.
   a) For Xilinx board,
      i. Connect AB09-FMCRAID board to FMC(1)-HPC connector on Xilinx development board.
      ii. Connect SATA-II/III device to CN0 on FMCRAID board.
      iii. Connect power to power connector on FMCRAID board.

   The connections are shown in Figure 2-5.

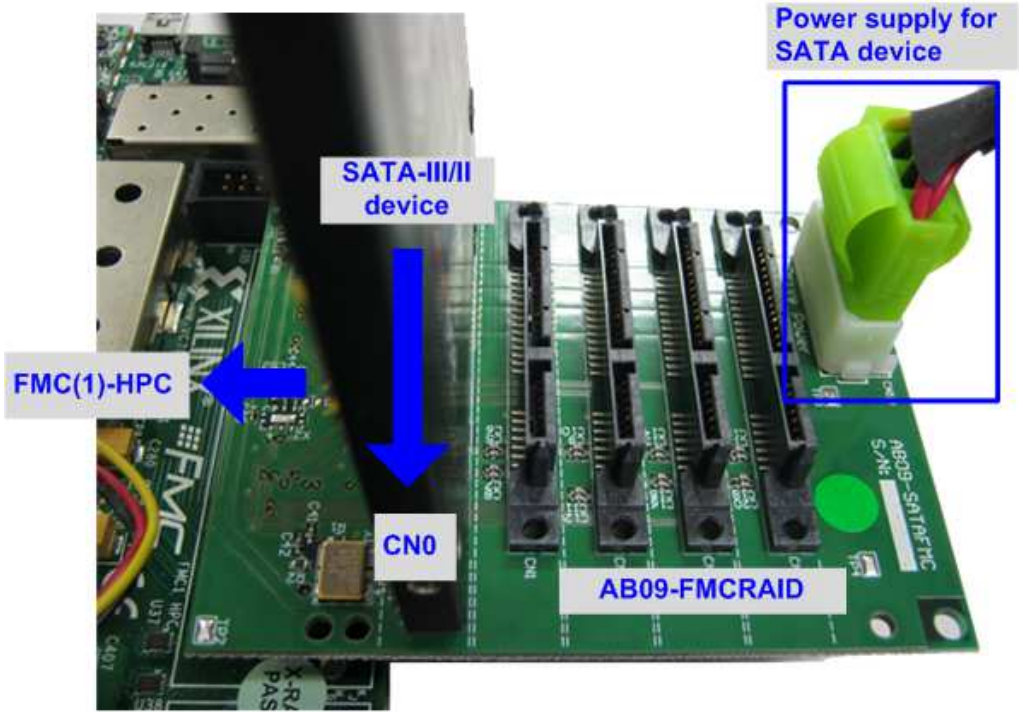

Figure 2-5 AB09-FMCRAID connection

b) For Zynq Mini ITX board,
   i. Connect the device to the SATA connector (J12) on the board using SATA cable.
   ii. Connect SATA Power cable to the device.

The connections are shown in Figure 2-6.

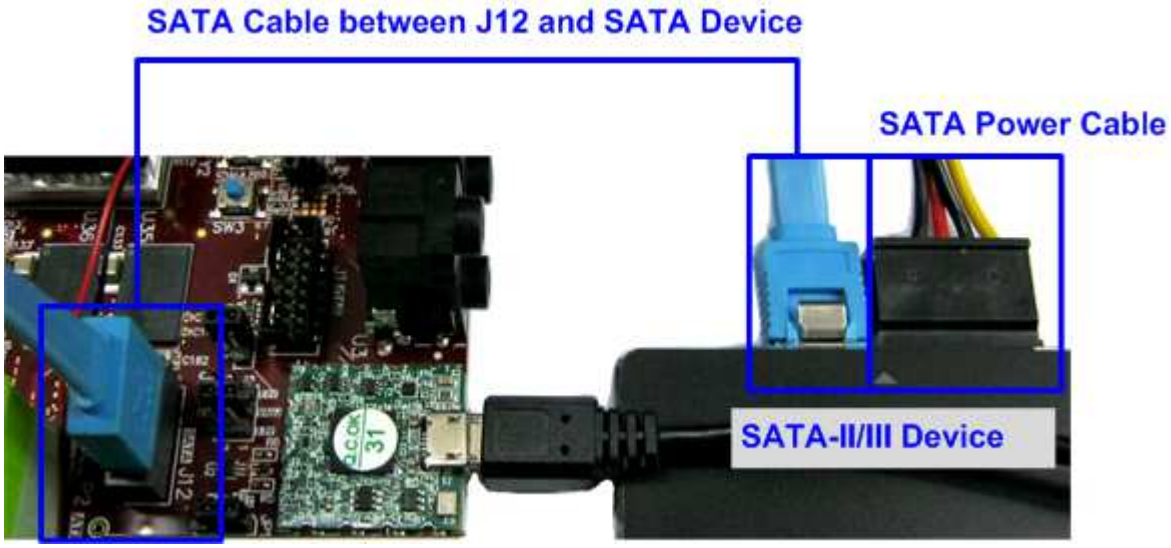

Figure 2-6 SATA-II/III device connection for Zynq Mini ITX

4) Set DIPSW bit 1-2 to select SATA speed mode.

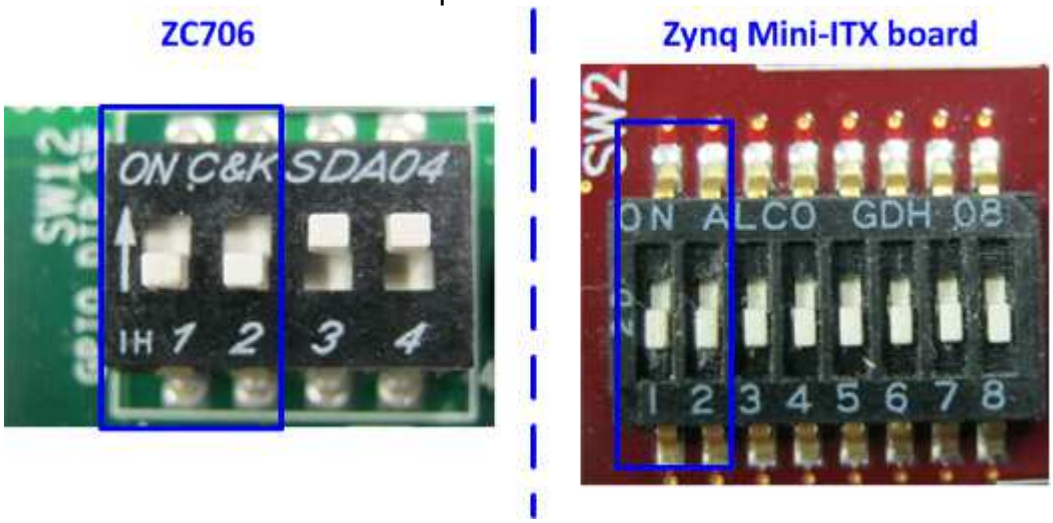

Figure 2-7 DIPSW to select SATA speed mode

DIPSW[2]	DIPSW[1]	Description
'1'	'1'	Fixed-speed at SATA3 (6.0 Gbps)
'1'	'0'	Fixed-speed at SATA2 (3.0 Gbps)
'0'	'X'	Auto-speed negotiation mode

Table 2-1 Descripiton of DIPSW for SATA speed

5) Connect micro USB cable from FPGA development board to PC for JTAG programming
6) Connect mini/micro USB cable from FPGA board to PC for Serial console.

Figure 2-8 USB cable connection

7) Power on FPGA development board and power supply for SATA device.
8) Open Serial console such as TeraTerm, HyperTerminal and set Buad rate=115,200 Data=8 bit Non-Parity Stop=1.
9) For Zynq Mini-ITX (Z100)/ZC706 board, open ISE command prompt or Vivado TCL shell, change current directory to baremetalOS folder, and run MiniITX_7z100/ zc706_sata_ahci.bat, as shown in Figure 2-9 and Figure 2-10.

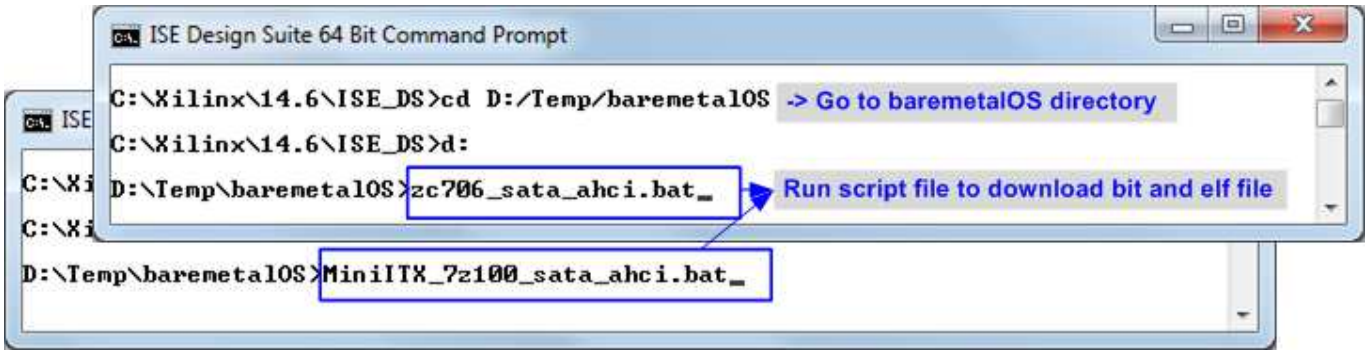

Figure 2-9 Command script for download demo file by ISE tool

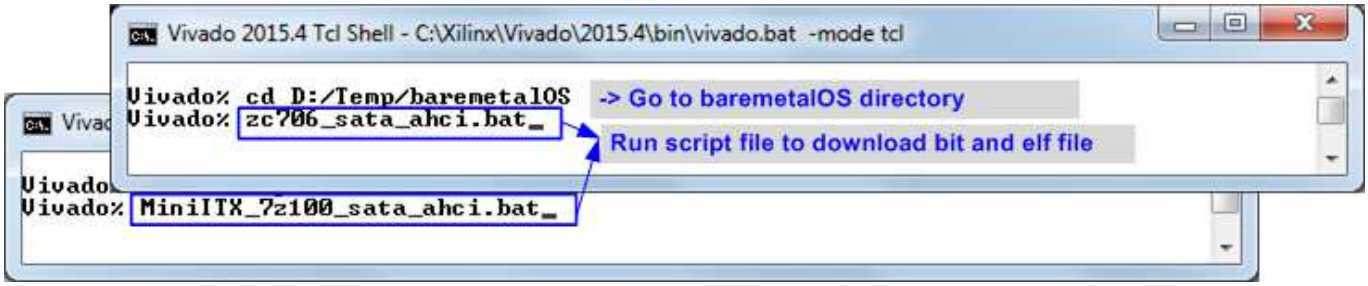

Figure 2-10 Command script for download demo file by Vivado tool

10) Check LED status on FPGA development board. The description of LED is follows.

LED	ON	OFF
LEDL/D4	OK	150 MHz of SATA clock cannot lock. Please check 150 MHz clock source for SATA.
LEDC/D5	OK	SATA-IP cannot detect SATA device. Please check SATA device and the connection.
LEDR/D6	SATA-III	SATA-II
LED0/D7	Always OFF	

Table 2-2 LED Status of reference design on FPGA board

11) After programming completely, LEDL/D4 and LEDC/D5 will be ON after complete SATA initialization process. LEDR/D6 shows SATA speed status, as shown in Figure 2-11.

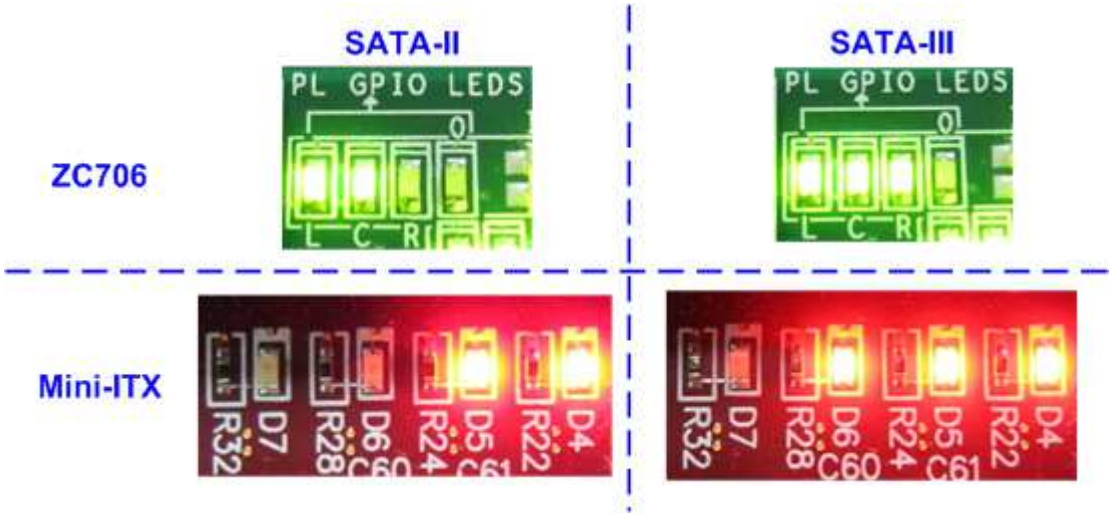

Figure 2-11 LED status after system set up complete on SATA-3/2 speed

12) Main menu will be displayed on Serial console as shown in Figure 2-12. Then, user can execute each command operation. Please check serial cable connection if this menu is not displayed on the console.

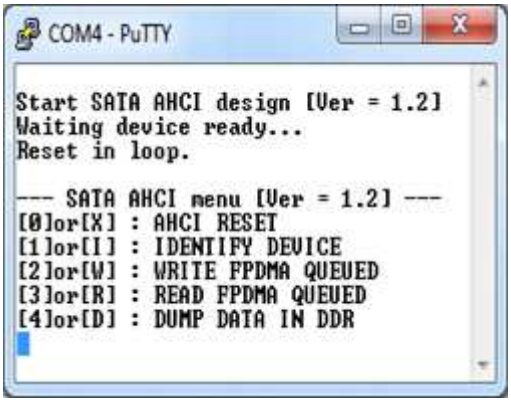

Figure 2-12 Main Menu

3 Main Menu

3.1 AHCI RESET

Select ‘0’ or ‘X’ for sending hardware reset signal to AHCI-IP. “AHCI RESET selected” is displayed before reset IP asserted. After complete reset sequence, main menu will be displayed, as shown in Figure 3-1.

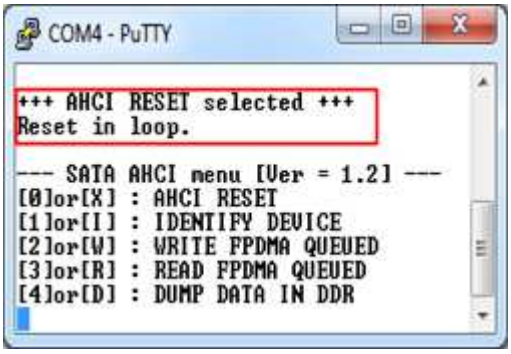

Figure 3-1 AHCI Reset Output

3.2 IDENTIFY DEVICE

Select ‘1’ or ‘I’ for sending “IDENTIFY DEVICE” command to HDD/SSD. Disk information (Model name, disk capacity) will be displayed by using this menu. In the last line, it will show that the device can or cannot support Native Command Queuing feature. This demo can run only with SATA device which can support NCQ.

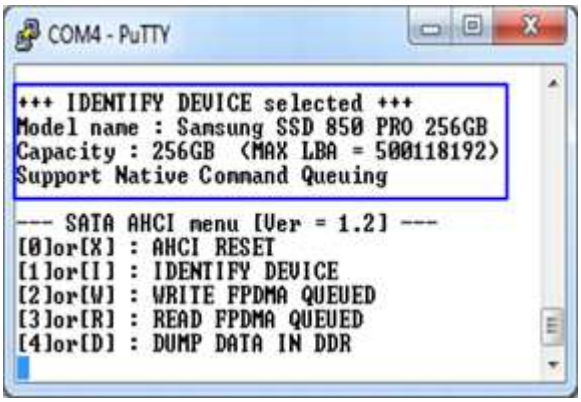

Figure 3-2 Disk Information from IDENTIFY DEVICE command

3.3 WRITE FPDMA QUEUED

Select '2' or 'W' for sending "WRITE FPDMA QUEUED" command to HDD/SSD. Three inputs are required for this menu, i.e.

- Start LBA: this value is the start sector number of HDD/SSD to write data.
- Sector Count: this value is the total transfer size in sector unit (512 byte) for writing HDD/SSD. This size is the data size for CPU to fill to write buffer. If the input is more than 65536 (maximum size for one SATA command), only 65536 sector data is filled and the next command will use same data area with the first command.
- Write Pattern: this value is used for selecting test pattern to write to buffer and then forward to HDD/SSD. There are six test patterns in this demo, i.e. 32-bit increment [0], 32-bit decrement [1], 00000000H [2], FFFFFFFFH [3], current data in read buffer [4], and LFSR counter [5].

After software receives all inputs correctly,

- "Prepare data" will be displayed during CPU writing test pattern data to write buffer.
- "Execute Write" will be displayed during CPU sending WRITE FPDMA QUEUED command and transferring data from write buffer to HDD/SSD.
- Transfer speed will be displayed after write operation complete.

Figure 3-3 shows the example of test result when operation complete. Write operation will be cancelled if receiving error input as shown in Figure 3-4.

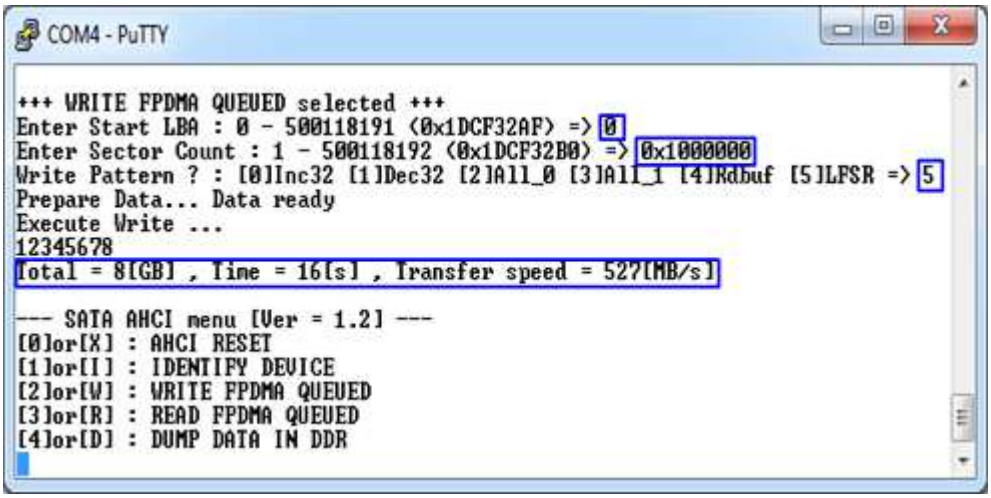

Figure 3-3 WRITE FPDMA QUEUED command input and output

Figure 3-4 Write Operation cancelled from error input

3.4 READ FPDMA QUEUED

Select '3' or 'R' for sending "READ FPDMA QUEUED" command to HDD/SSD. Two or three inputs are required for this menu, i.e.

- Start LBA: same description with Start LBA in WRITE FPDMA QUEUED menu.
- Sector Count: same description with Sector Count in WRITE FPDMA QUEUED menu. If this input is not more than 65536, the third input will be displayed for selecting verification pattern. If input is more than 65536, the third input will not be displayed to skip data verification process for checking performance only, as shown in Figure 3-5.
- Verify Pattern (Optional): this value is used for selecting verification pattern. This input should be matched with the pattern in WRITE FPDMA QUEUED menu. Six verification patterns can be selected, similar to write pattern. "Verify Data … Success" is displayed for success case, and "Data Mismatch with failure value" is displayed for failure case, as shown in Figure 3-7.

Similar to WRITE FPDMA QUEUED menu, Read operation will be cancelled if receiving error input, as shown in Figure 3-7.

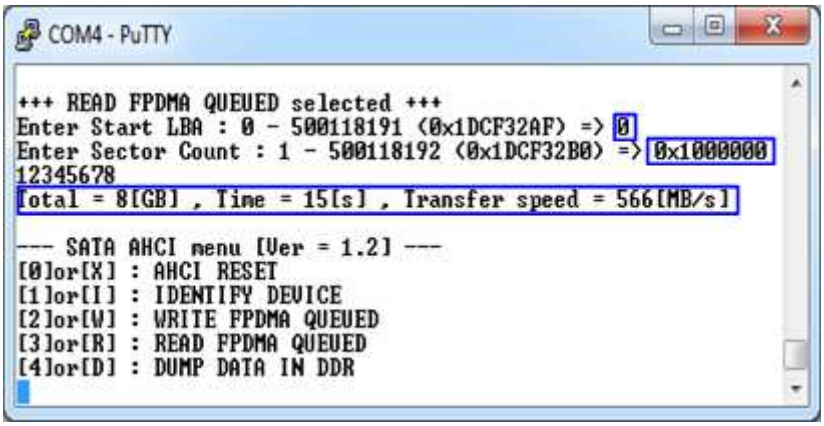

Figure 3-5 READ FPDMA QUEUED command without verify

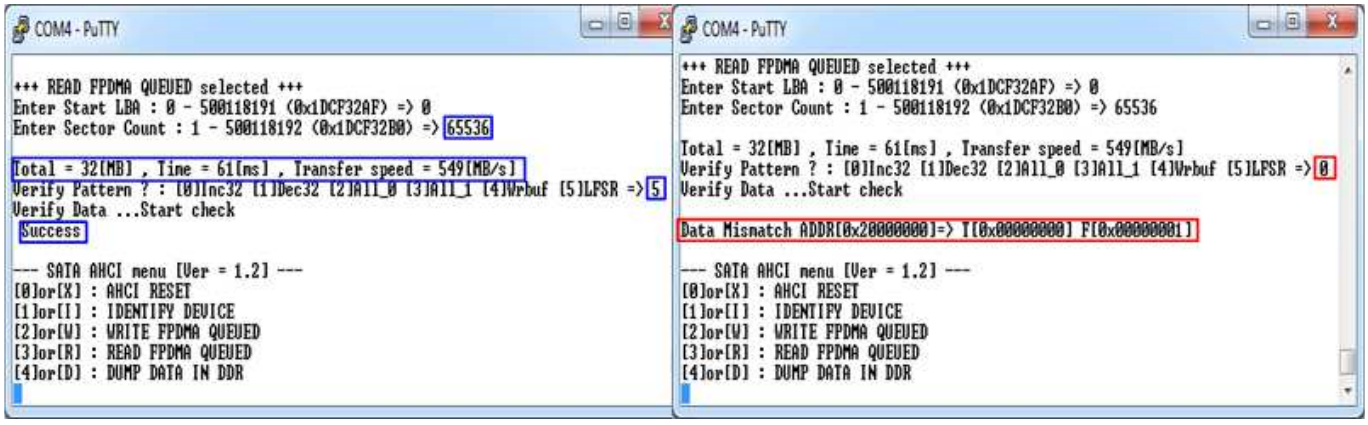

Figure 3-6 READ FPDMA QUEUED with verify process

Figure 3-7 Read Operation cancelled from error input

3.5 DUMP DATA IN DDR

Select '4' or 'D' to dump data from buffer to display on Serial Console. In this demo, DDR is mapped to address = 0000_0000h - 3FFF_FFFFh. Six submenus can be selected, i.e.

- 'G': this submenu is used to select the address to read, as shown in Figure 3-8. The address can be input to be hex value by adding prefix "0x", so normally input will be received in decimal value.

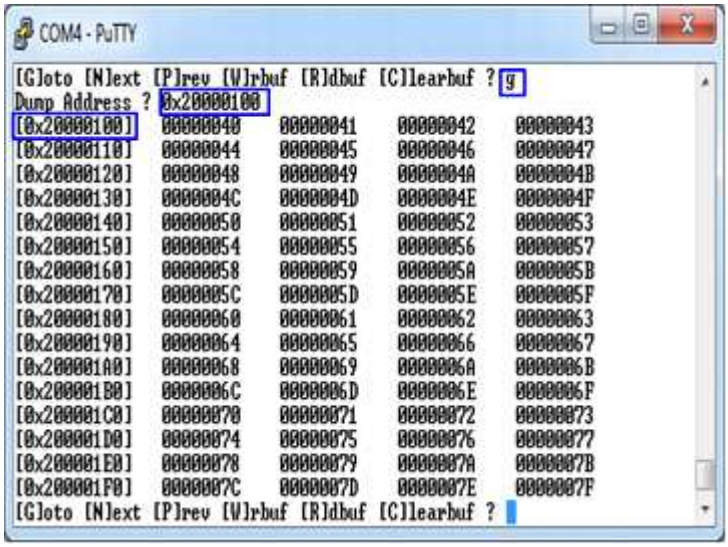

Figure 3-8 Goto submenu example

- 'N': this submenu is used to read next 256 byte data in buffer, as shown in Figure 3-9.
- 'P': this submenu is used to read previous 256 byte data in buffer, as shown in Figure 3-9.

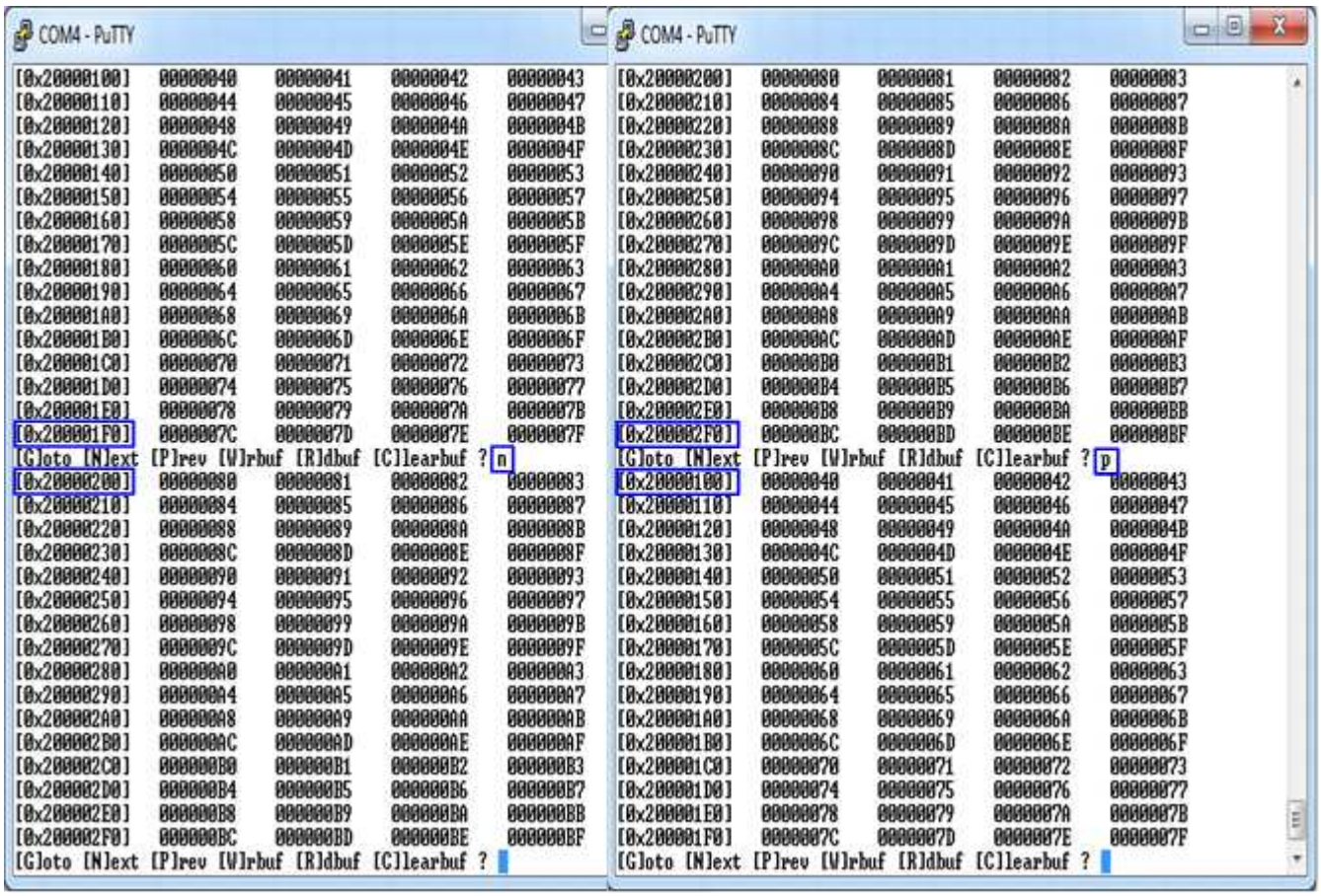

Figure 3-9 Read Next/Previous 256 byte data in buffer

- 'W': this submenu is used to read 256 byte data at top of write buffer, as shown in Figure 3-10.
- 'R': this submenu is used to read 256 byte data at top of read buffer, as shown in Figure 3-10.

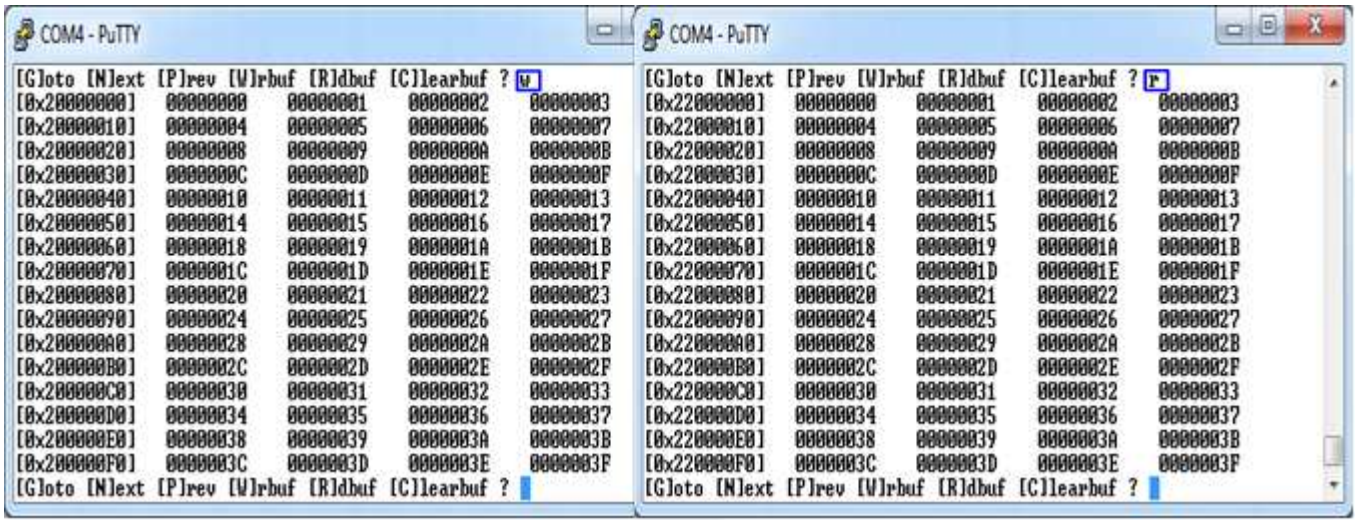

Figure 3-10 Read 256 byte data at top of write/read buffer

- ‘C’: this submenu is used to clear data in write/read buffer to be zero value. Select ‘Y’ to confirm for clear write/read buffer, but user can select ‘N’ to not clear the current buffer.

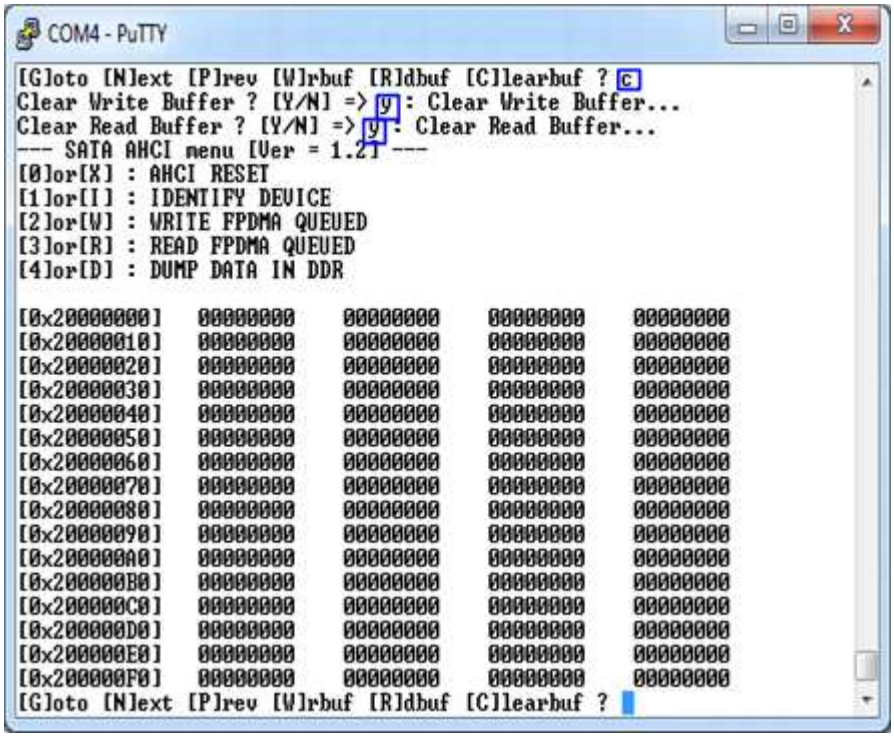

Figure 3-11 Clear buffer to be zero

User can exit this menu by input other key, such as ‘x’.

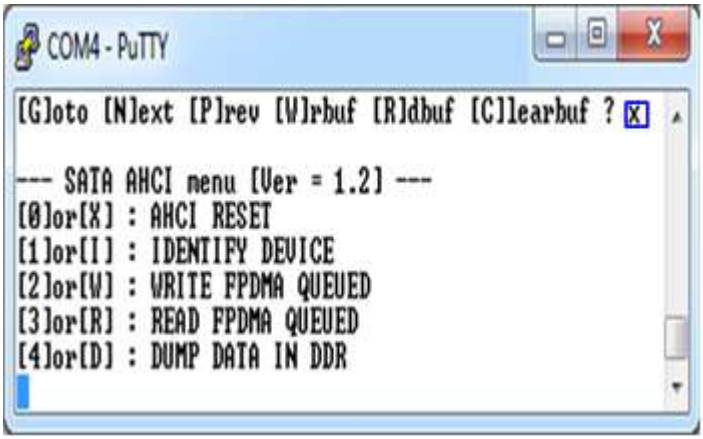

Figure 3-12 Exit dump menu

4 Revision History

Revision	Date	Description
1.0	9-Mar-16	Initial version release
1.1	10-Nov-16	Support Zynq Mini-ITX