TOE10G-IP Full Duplex Demo Instruction

Rev1.1 18-Nov-16

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between FPGA development board and PC in both directions at the same time through 10Gigabit Ethernet. This demo can select to run only supported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1-1, to run TOE10G-IP full duplex demo, please prepare

1) FPGA Development board (Arria10 SoC development board)
2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
4) micro USB cable for programming FPGA between FPGA Development board and PC
5) "tcp_client_txrx_10G.exe" which are test application designed by Design Gateway

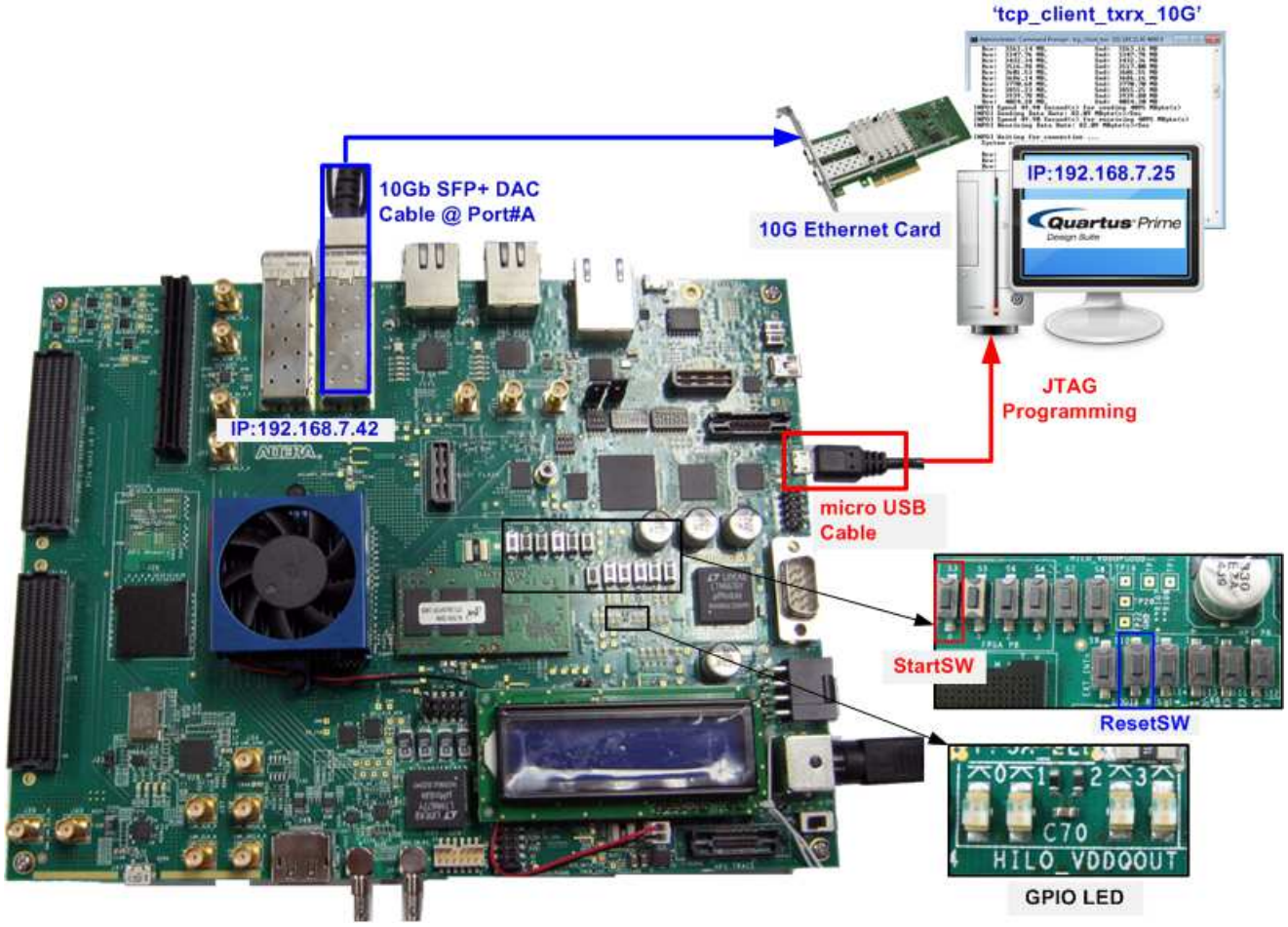

Figure 1-1 TOE10G-IP Full Duplex Demo Environment Setup on Arria10 SoC board

Note: Test result in this document is captured by using following test environment.

[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html

[2] 10-Gigabit SFP+ DAC cable
http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx

[3] PC: Motherboard ASUS H87M-E, 32 GB RAM, 64-bit Windows7 OS

2 Demo description

The logic on FPGA is designed to connect data input and output of TOE10G-IP as loopback connection. So, total transmit data from test application on PC will be returned to PC for verifying the data by test application. TCP connection is opened by PC, so PC runs on TCP Client mode while FPGA runs on TCP Server mode.

The status of the demo can be monitored by 4-bit FPGA LED (D25 - D28) as shown in Figure 2-1. The description of each status LED is shown Table 2-1.

Figure 2-1 FPGA LED t o show test status

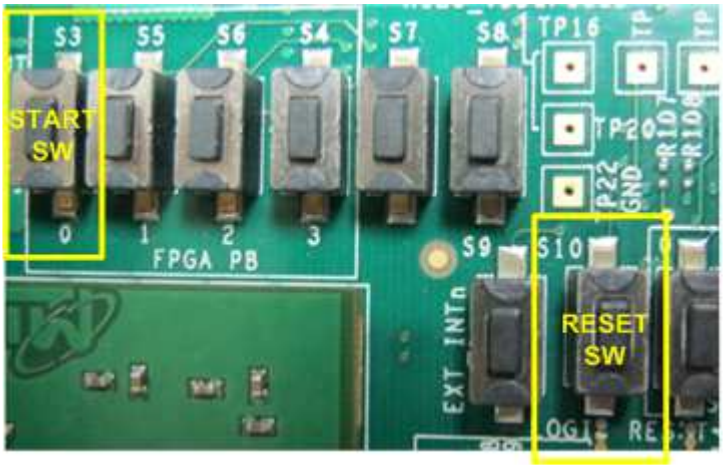

Figure 2-2 Start SW and Reset SW position

Table 2-1 LED Definition

FPGA LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (S3) has already been pressed and confirm IP address setting on PC that is correct.
1	BLINK: Operation timeout	Normal operation
2	N/A	N/A
3	ON: Port is established	No operation

3 How to run demo

3.1 FPGA Programming

To run the demo, please follow these steps.

- Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.

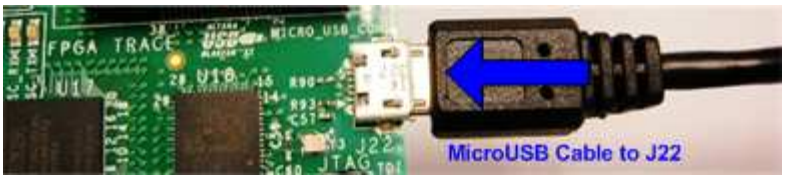

Figure 3-1 MicroUSB connection

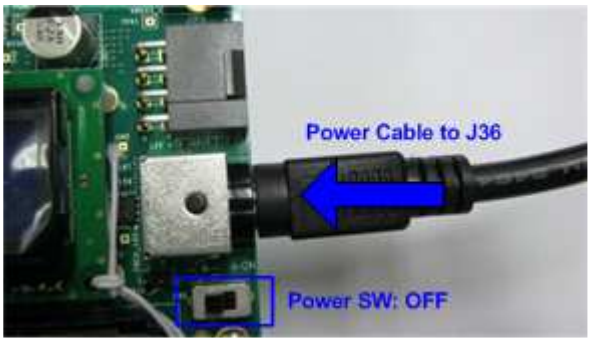

Figure 3-2 Power cable connection

- Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between SFP+ Port A and PC.

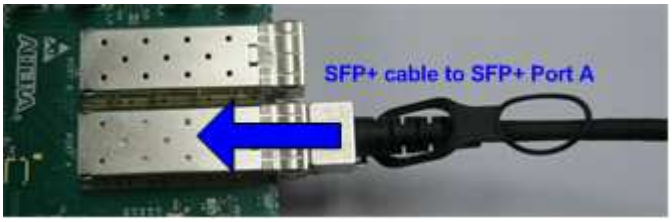

Figure 3-3 SFP+ cable connection

- Setup network setting on PC, following Topic 3 in “dg_toe10gip_instruction_altera” document.
- Power on FPGA development board.

- Open “Clock Controller” application which is provided in Arria10 SoC release package. Select Si5338(U50) tab, and set CLK3 value to be “322.265625”. Click “Set” button to program clock to be 322.265625 MHz, as shown in Figure 3-4.

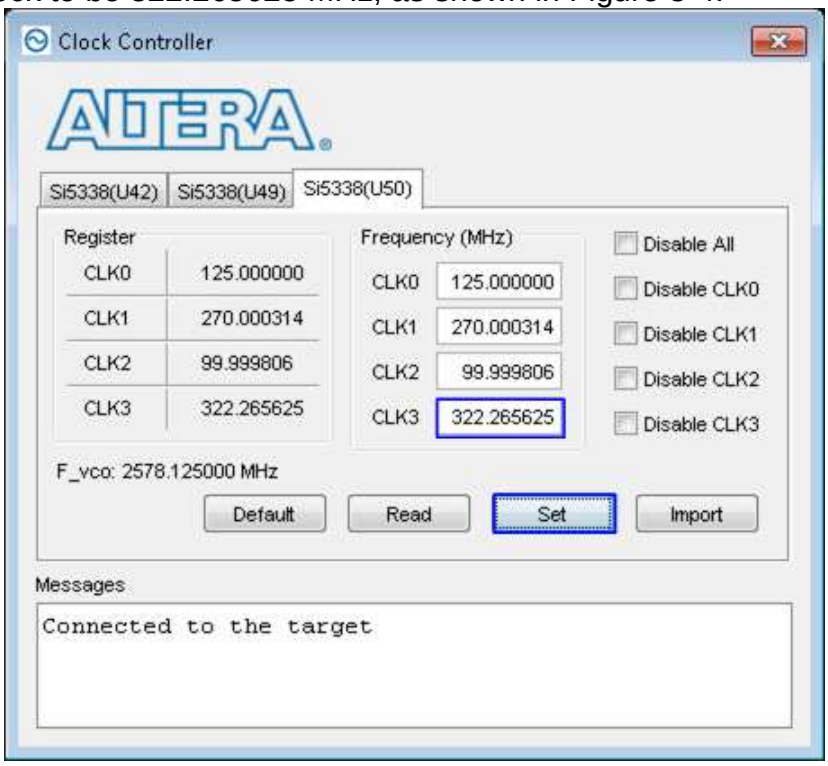

Figure 3-4 Reference clock programming

- Open Quartus Programmer, select SOF file, and program file to FPGA development board, as shown in Figure 3-5.

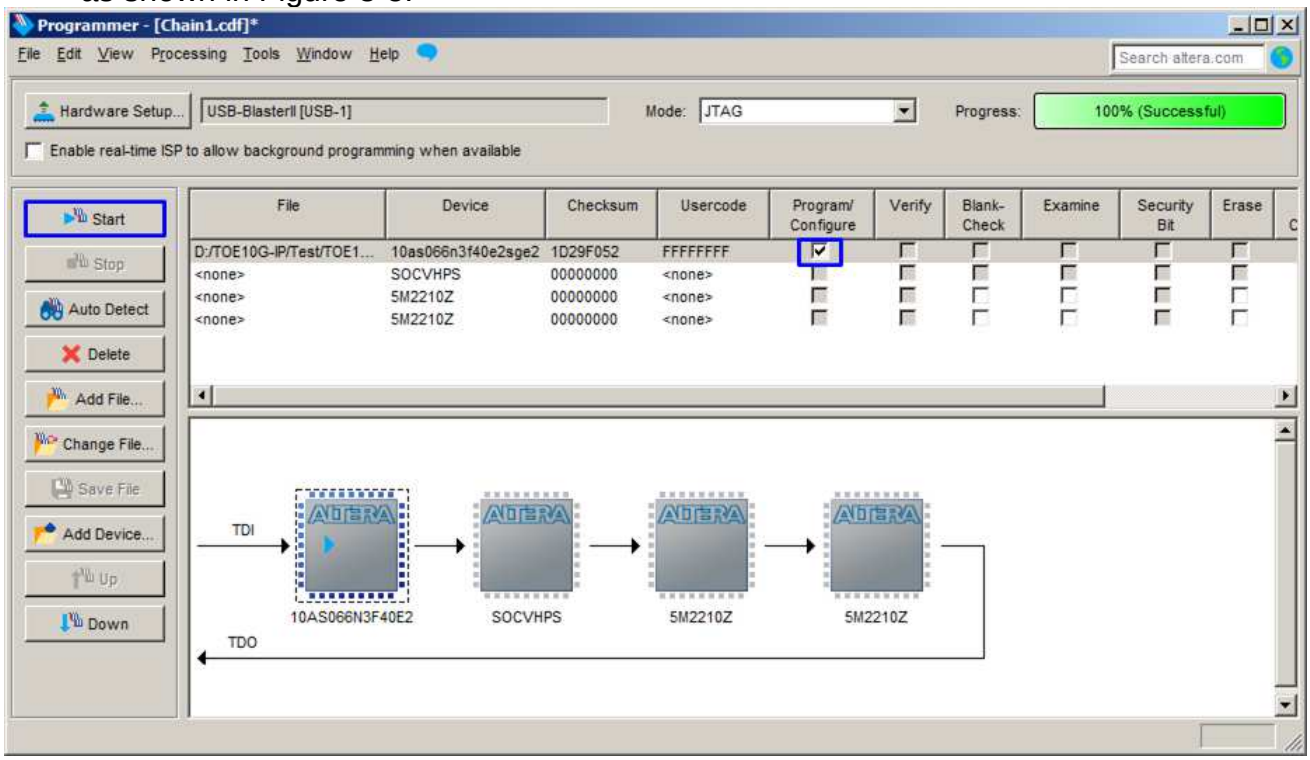

Figure 3-5 Program SOF File

- Since the reference design uses evaluation IP of 10G EMAC, warning message will be displayed after programming completely as shown in Figure 3-6. Reference design can run about 20 mins.

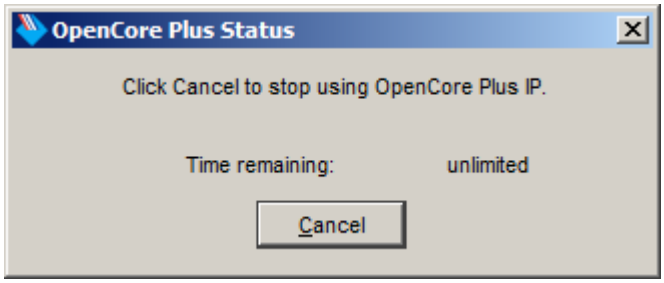

Figure 3-6 Warning message of OpenCore Plus IP

- Press StartSW at S3 position (as shown in Figure 2-2) to initialize parameter in system, and then LED0 will turn on, as shown in Figure 3-7.

Figure 3-7 LED Status after press StartSW

Note: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.

3.2 Run Test Application

Test application will operate to send and receive 32 GB data at the same time. After FPGA receives all 32 GB data and forwards all data completely, it will close port connection. Test application is designed to operate in forever loop. The new connection will be created by test application to rerun the test. User needs to cancel the application to stop the test.

There are two operation modes for running the demo, i.e. Performance test mode, and Verification mode. The different point between Performance test mode and Verification mode is the operation on Test application that will be generated real data or dummy data. Hardware operation on FPGA is not different because the logic is used to forward packet only.

On performance test mode, PC will generate all ‘0’ data pattern and will not verify returned data from FPGA to reduce the task in application. So, in this mode PC can achieve the best performance for transferring 10-Gb data.

For verification mode, 32-bit increment data will be generated by test application while the received data will be verified with expect pattern. In this mode, performance will be slower from higher PC resource utilization. It is designed to check data reliability on the network. The details of each mode are follows.

3.2.1 Performance test mode

- Open “command prompt” on PC, and run “tcp_client_txrx_10G” test application by following command
  >> tcp_client_txrx_10G <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without HDL code modification.
  - Mode: ‘0’-All ‘0’ pattern are sent out and no data verification

  For example,
  >> tcp_client_txrx_10G 192.168.7.42 4000 0

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 3-8.
- User can cancel operation by pressing “Ctrl+C”.

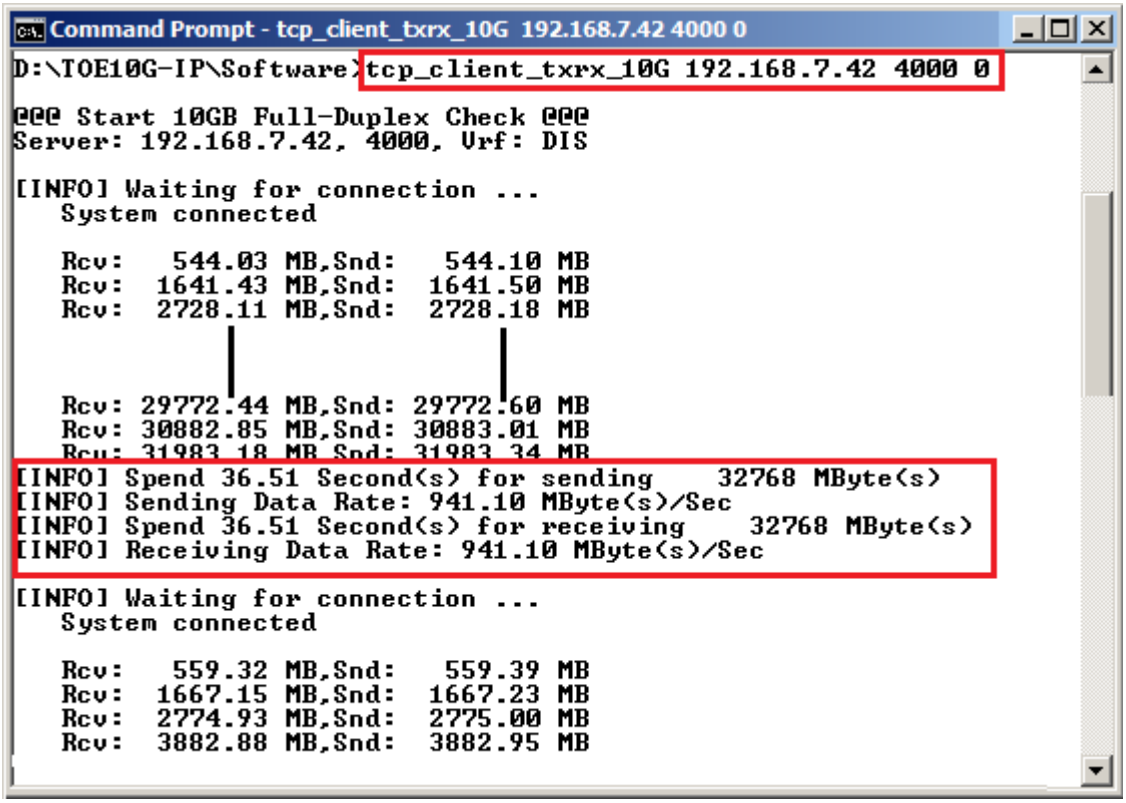

Figure 3-8 Test Result on Performance test mode

Figure 3-9 LED Status when running Performance Test mode

3.2.2 Verification mode

- Open “command prompt” on PC, and run “tcp_client_txrx_10G” test application by following command
  >> tcp_client_txrx_10G <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘1’-32-bit increment data are sent out and data verification is enabled.

  For example,
  >> tcp_client_txrx_10G 192.168.11.42 4000 1

- Test application displays the current number of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 3-10.
- User can cancel operation by pressing “Ctrl+C”.

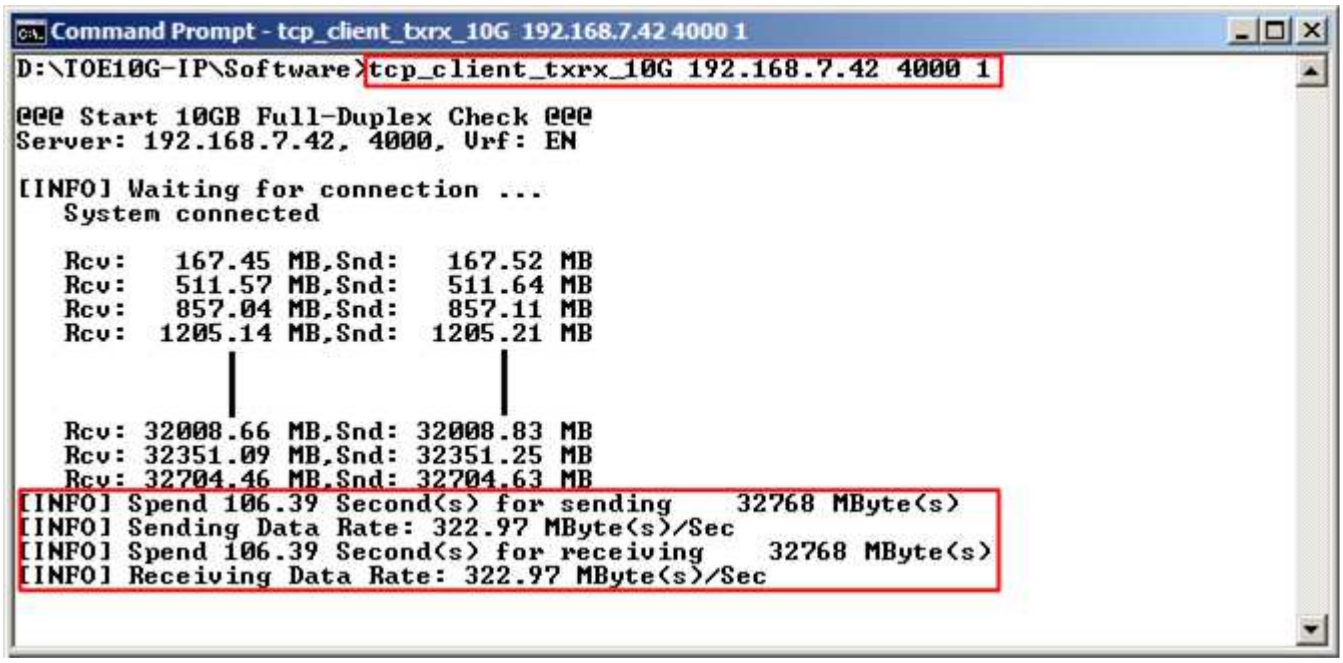

Figure 3-10 Test Result on Verification mode

4 Revision History

Revision	Date	Description
1.0	23-May-16	Initial version release
1.1	18-Nov-16	Update Figure 1-1