TOE10G-IP Full Duplex Demo Instruction

Rev1.1 10-Nov-14

This document describes the instruction to run TOE10G-IP for transferring 10-Gb data between FPGA development board and PC in both directions at the same time through 10Gigabit Ethernet. This demo can select to run only supported Jumbo frame PC.

1 Environment Setup

As shown in Figure 1 - Figure 3, to run TOE10G-IP full duplex demo, please prepare

1) FPGA Development board (KC705/VC707/ZC706)
2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
4) micro USB cable for programming FPGA between FPGA Development board and PC
5) "tcp_client_txrx_10G.exe", provided by Design Gateway, which are test application available on PC

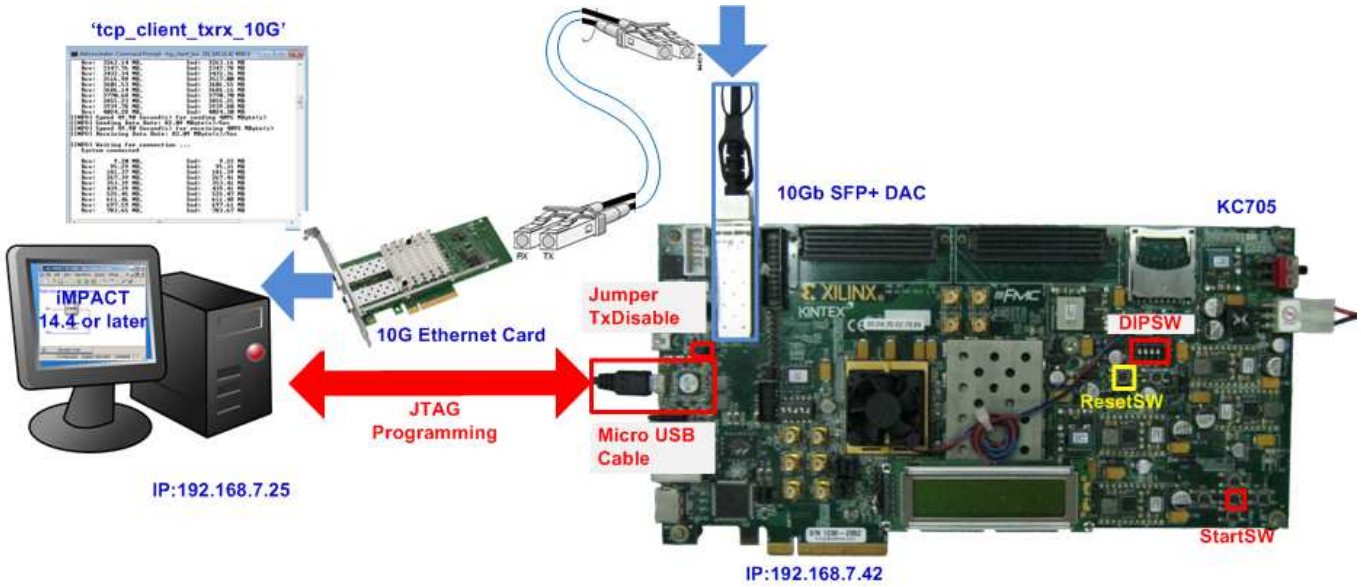

Figure 1 TOE10G-IP Full Duplex Demo Environment Setup on KC705

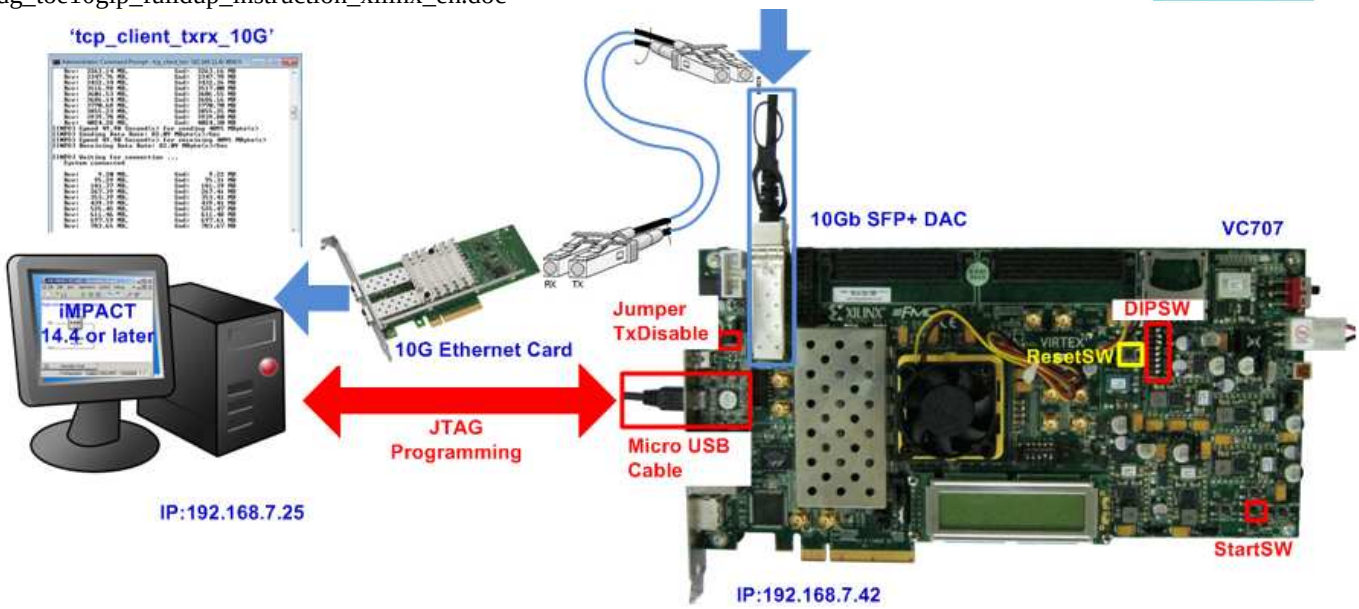

Figure 2 TOE10G-IP Full Duplex Demo Environment Setup on VC707

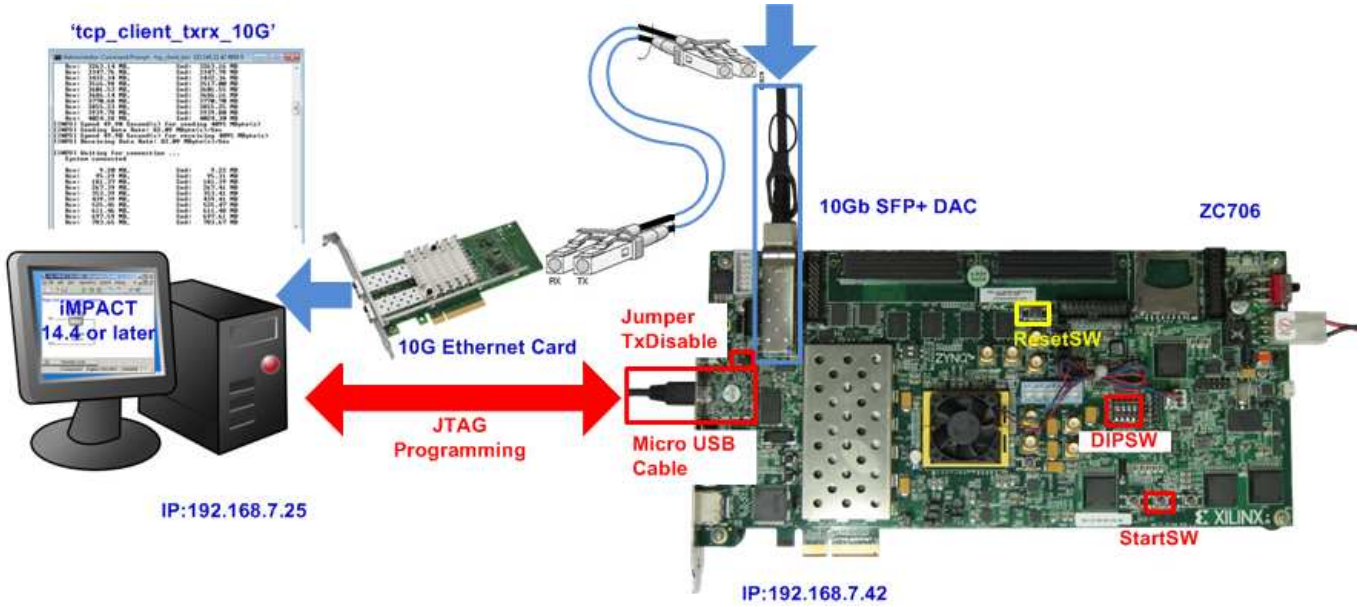

Figure 3 TOE10G-IP Full Duplex Demo Environment Setup on ZC706

Note: Test result in this document is captured by using following test environment.

[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html

[2] 10-Gigabit SFP+ DAC cable
http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx

[3] PC: Motherboard ASUS H87M-E, 8 GB RAM, 64-bit Windows7 OS

2 Demo description

The logic on FPGA is designed to connect data input and output of TOE10G-IP as loopback connection. So, total transmit data from test application on PC will be returned to PC for checking the data by test application. TCP connection is opened by PC, so PC runs on TCP Client mode while FPGA runs on TCP Server mode. The definition of LED on FPGA development board is described in Table 1.

Table 1 LED Definition

GPIO LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (CenterSW) has already been pressed and confirm IP address setting on PC that is correct.
1/R	BLINK: Operation timeout	Normal operation
2/C	N/A	N/A
3/L	ON: Port is established	No operation

3 How to run demo

3.1 FPGA Programming

To run the demo, please follow these steps.

- Insert jumper to enable SFP+ (J4 for KC705, J17 for ZC706, or J6 for VC707), as shown in Figure 4.

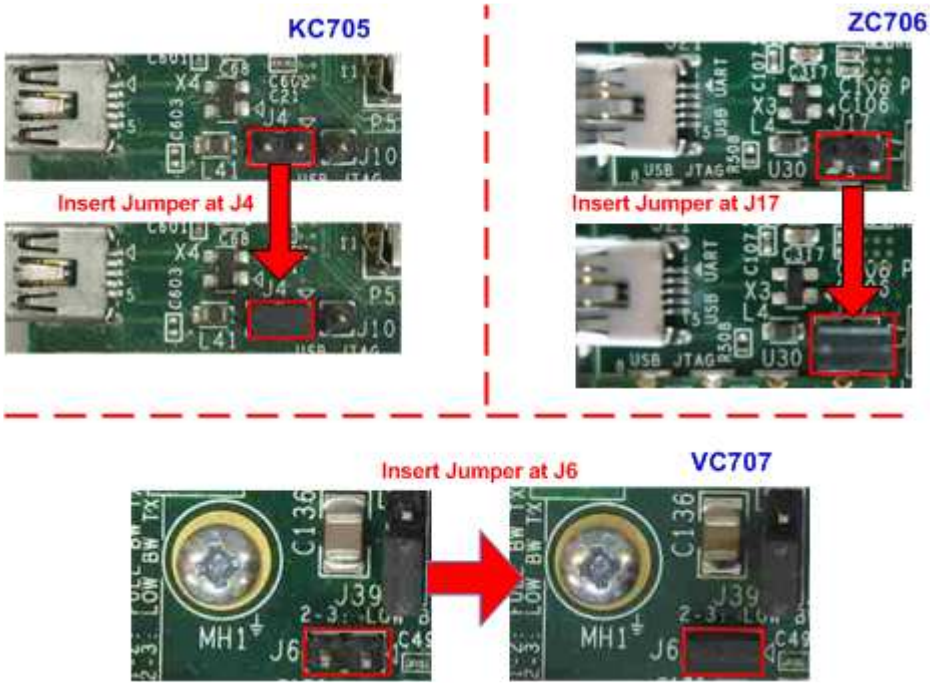

Figure 4 Insert jumper to enable SFP+

- For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 5 - Figure 6.

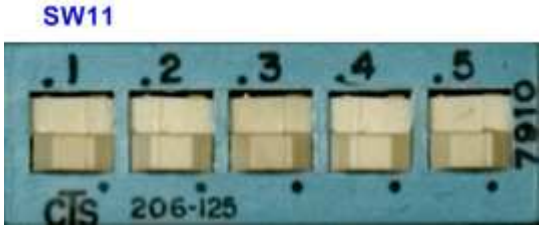

Figure 5 SW11 setting to configure PS from JTAG on ZC706 board

Figure 6 SW4 setting to use USB-to-JTAG on ZC706 board

- Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.
- Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between FPGA development board and PC.
- Setup network setting on PC, following Topic 3 in “dg_teo10gip_instruction_xilinx” document.
- Power on FPGA development board.
- Open iMPACT and download bit file to FPGA development board, as shown in Figure 7.

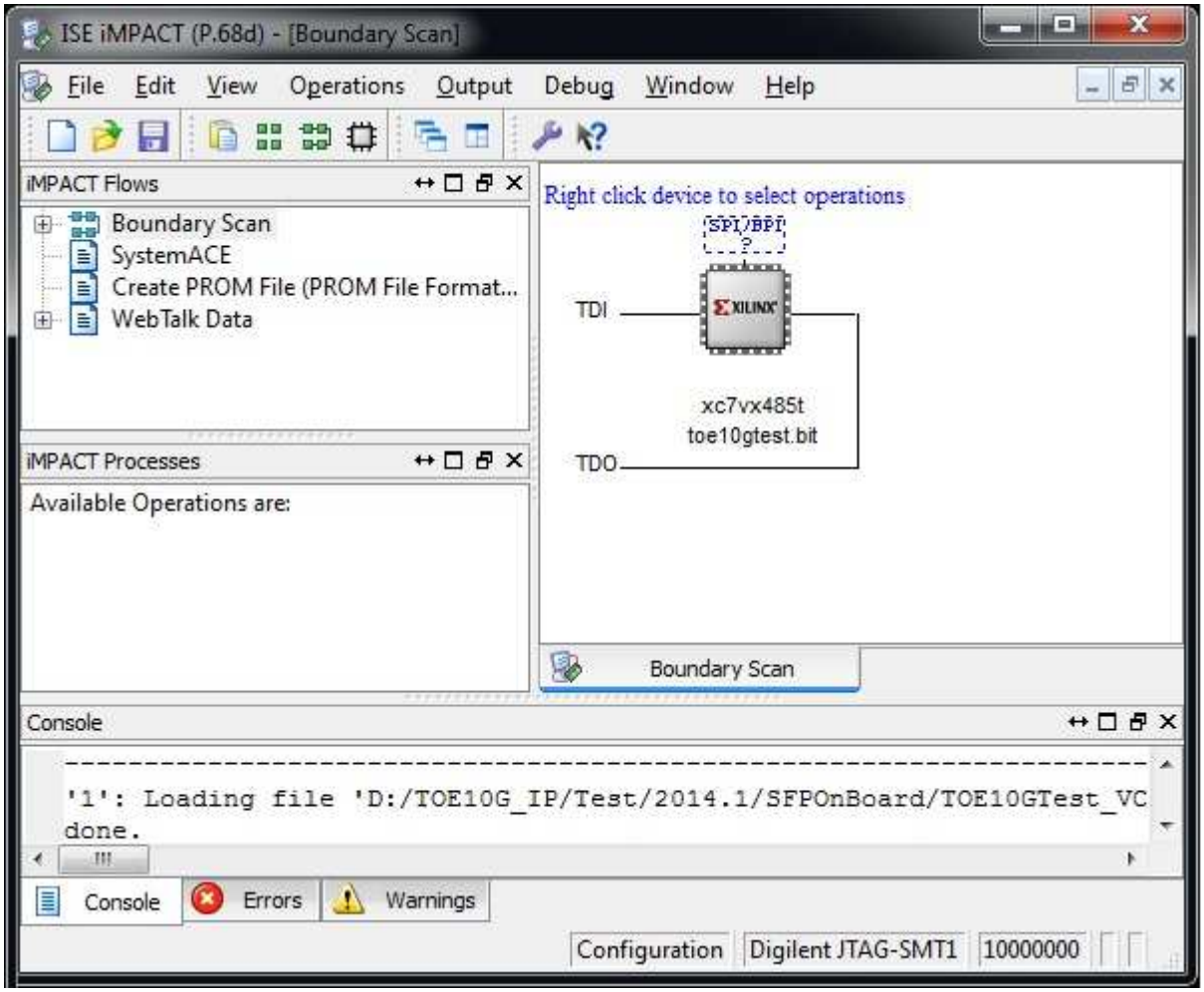

Figure 7 Programmer Environment

- Press StartSW at Center-SW as shown in Figure 1 - Figure 3 to initialize parameter in system, and then LED0 will turn on, as shown in Figure 8. Now system is ready to transfer data.

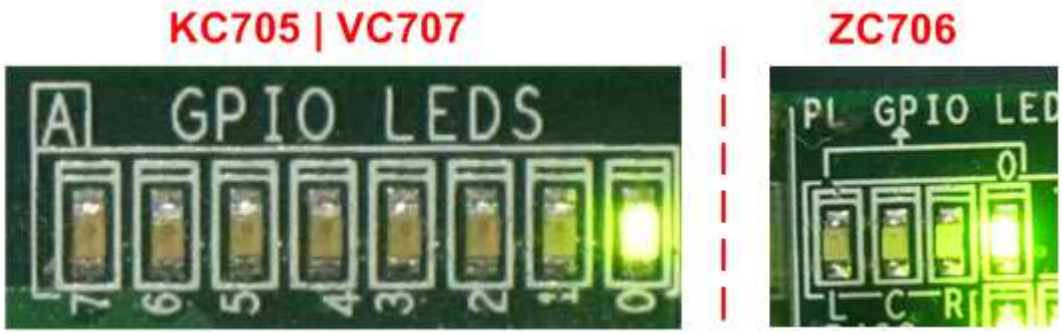

Figure 8 LED Status after push StartSW

Note: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.

3.2 Run Test Application

Test application will operate to send and receive 32 GB data at the same time. After FPGA receives all 32 GB data and forwards all data completely, it will close port connection. Test application is designed to operate in loop, so new connection will be created by Test application to rerun the test. User needs to cancel the application to stop the test.

There are two operation modes for running the demo, i.e. Performance test mode, and Verification mode. The different point between Performance test mode and Verification mode is the operation on Test application, while hardware operation on FPGA is the same by forwarding packet only. On performance test mode, PC will generate all ‘0’ data pattern and not verify returned data from FPGA to reduce the task in application. So, in this mode PC can achieve the best performance for transferring 10-Gb data. For verification mode, 32-bit increment data will be generated by test application while the received data will be verified with expect pattern. This mode will show lower performance, but it is designed to check data reliability on the network. The details of each mode are follows.

3.2.1 Performance test mode (Jumbo frame)

- Open “command prompt” on PC, and run “tcp_client_txrx_10G” test application by following command
  >> tcp_client_txrx_10G <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘0’-All ‘0’ pattern are sent out and no data verification

  For example,
  >> tcp_client_txrx_10G 192.168.7.42 4000 0

- Test application displays the current numbers of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 9.
- User can cancel operation by pressing “Ctrl+C”.

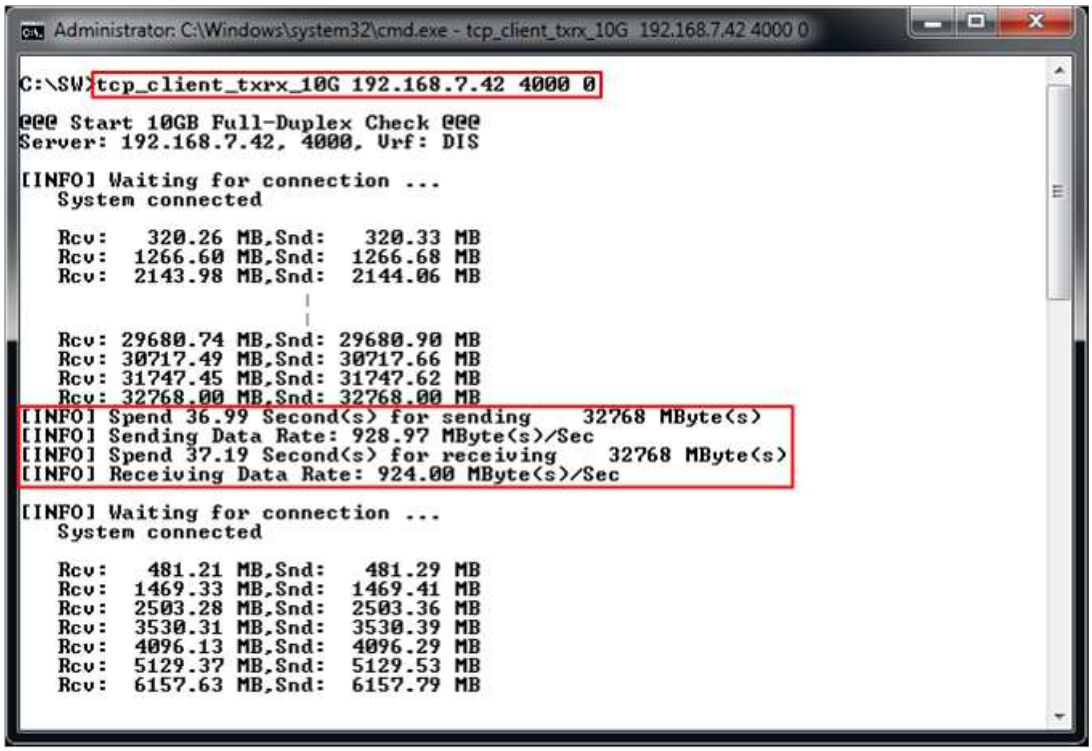

Figure 9 Test Result on Performance test mode

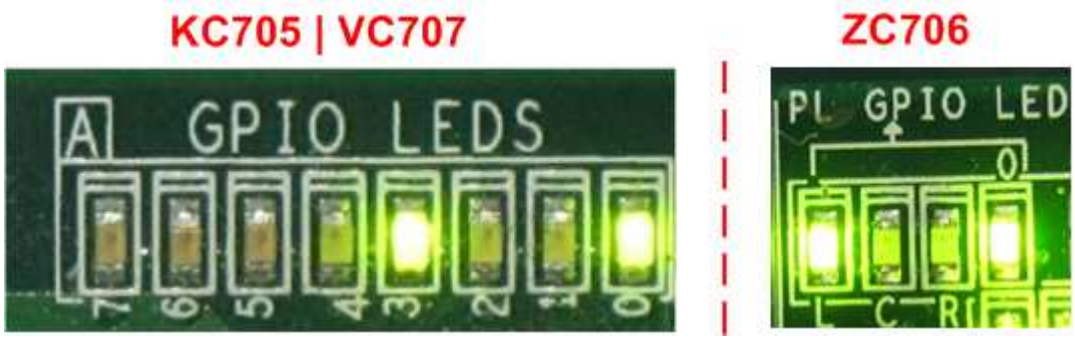

Figure 10 LED Status when running Performance Test mode

3.2.2 Verification mode

- Open “command prompt” on PC, and run “tcp_client_txrx_10G” test application by following command
  >> tcp_client_txrx_10G <FPGA IP address> <FPGA port number> <mode>
  - IP address and port number cannot change without vhdl code modification.
  - Mode: ‘1’-32-bit increment data are sent out and data verification is enabled.

  For example,
  >> tcp_client_txrx_10G 192.168.11.42 4000 1

- Test application displays the current numbers of transmit and received data every second. Time usage with performance will be displayed when end of each loop, as shown in Figure 11.
- User can cancel operation by pressing “Ctrl+C”.

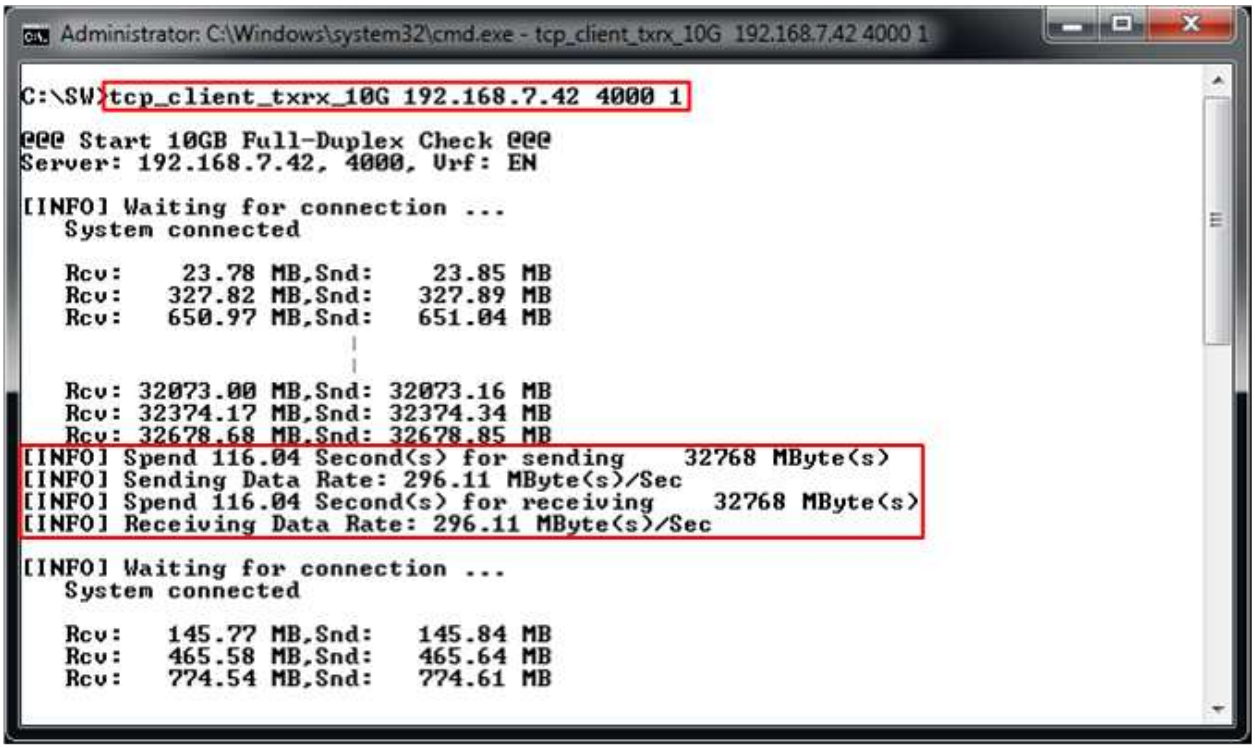

Figure 11 Test Result on Verification mode

4 Revision History

Revision	Date	Description
1.0	10-Sep-14	Initial version release
1.1	10-Nov-14	Add ZC706 support