TOE10G-IP Multisession Demo Instruction

Rev1.0 8-Nov-16

This document describes the instruction to show 10Gb Ethernet data transfer between FPGA board and PC. PC can run up to eight test applications for transferring data through eight sessions at the same time. Packet size in the demo is not Jumbo frame size.

1 Environment Setup

As shown in Figure 1-1 - Figure 1-3 to run TOE10G-IP full duplex demo, please prepare

1) FPGA Development board (KCU105/VC707/ZC706)
2) PC with 10Gigabit Ethernet support or 10Gigabit Ethernet card
3) 10 Gigabit SFP+ Copper Cable (DAC) or 2x10-Gigabit SFP+ Transceiver with Optical cable for network connection between FPGA Development board and PC
4) micro USB cable for programming FPGA between FPGA Development board and PC
5) Test application available on PC: “tcpdatatest.exe” provided by Design Gateway

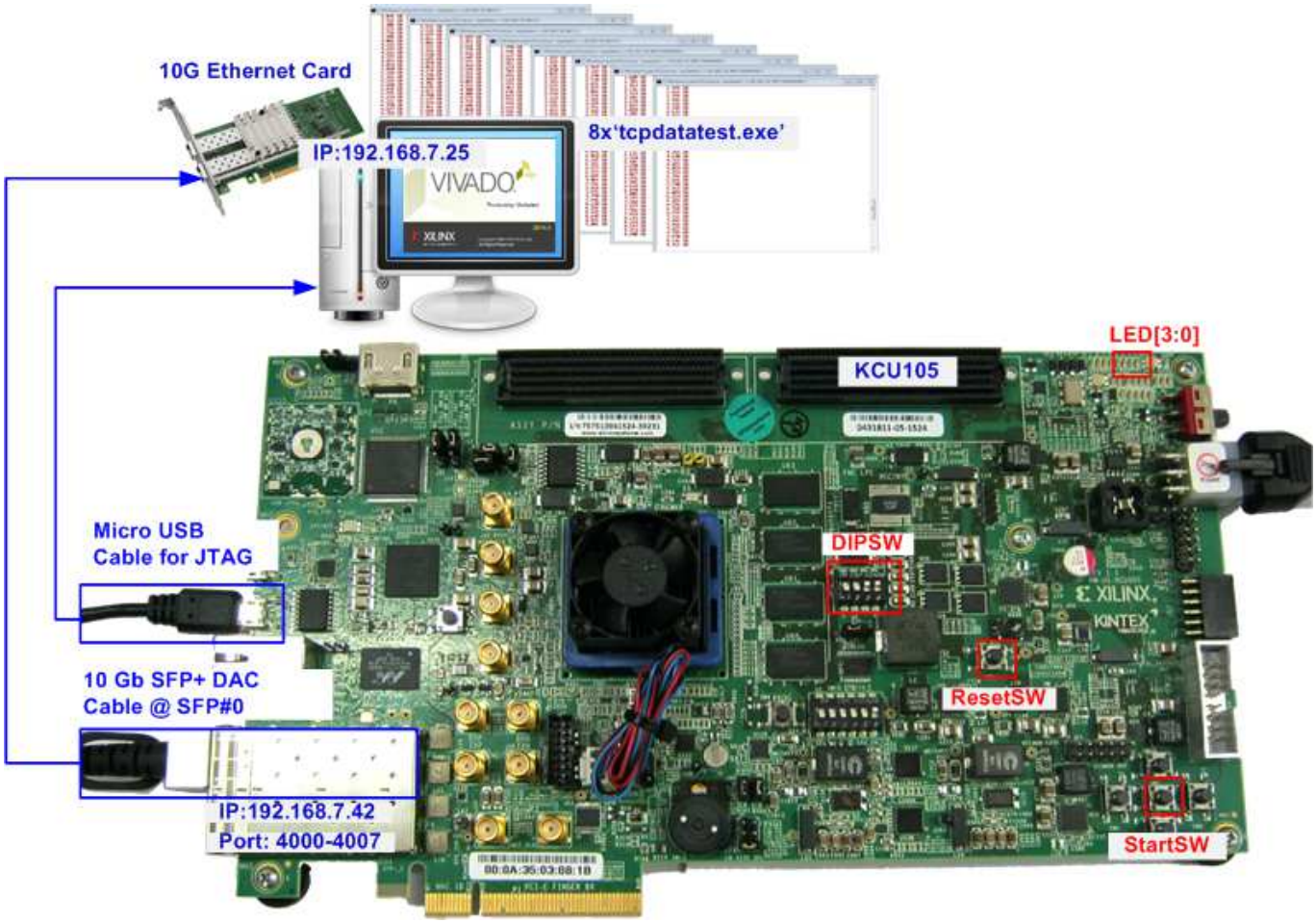

Figure 1-1 TOE10G-IP Multisession Demo Environment Setup on KCU105

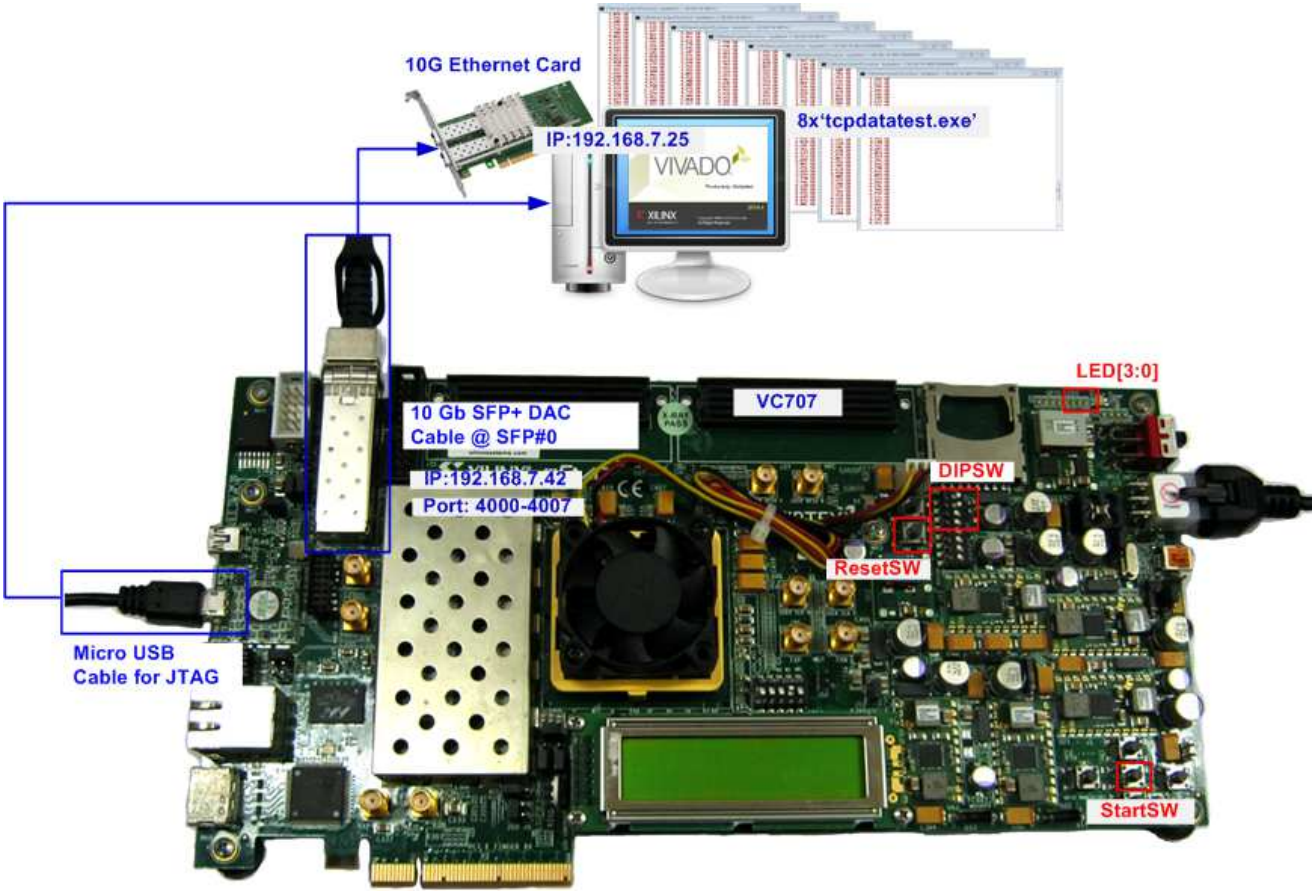

Figure 1-2 TOE10G-IP Multisession Demo Environment Setup on VC707

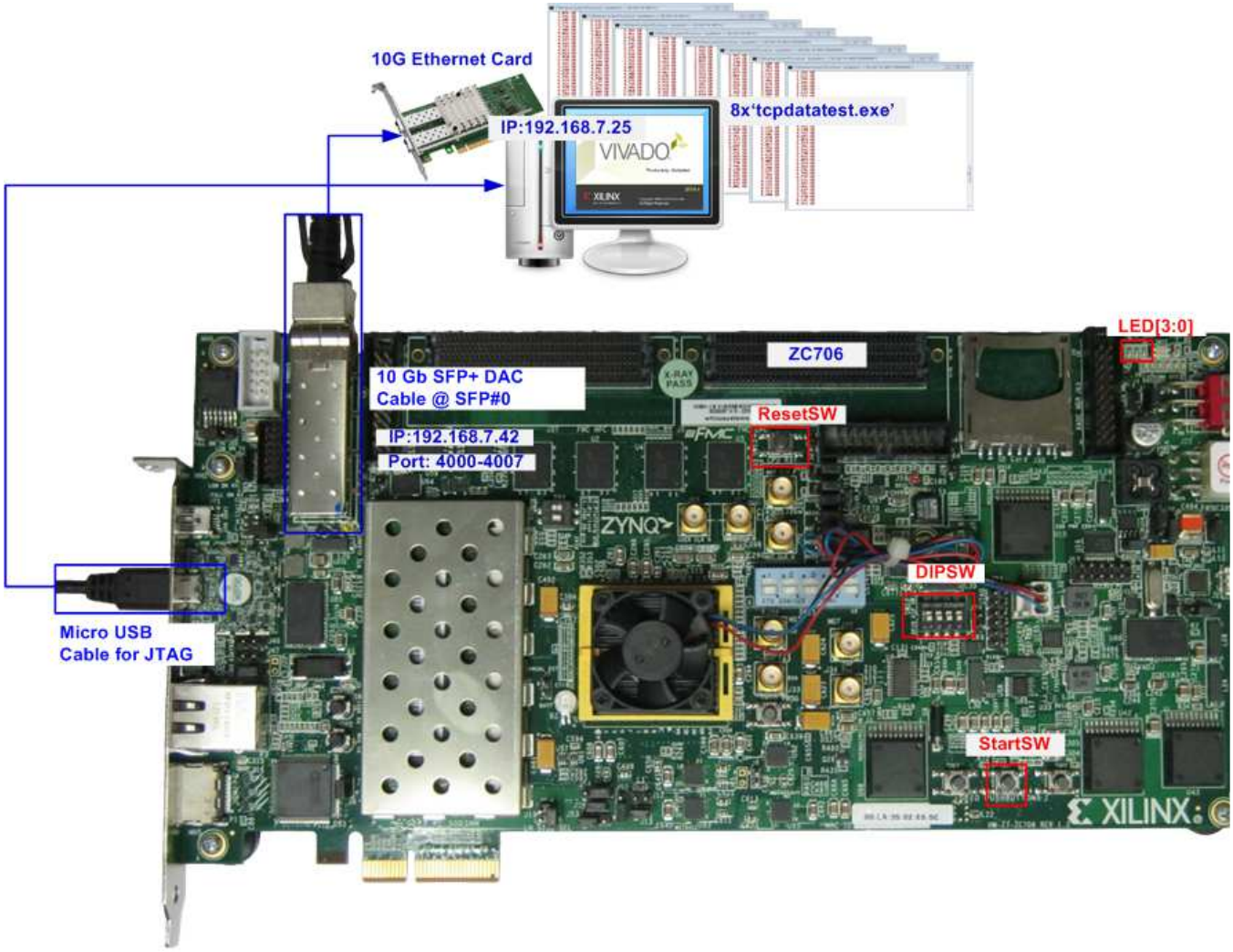

Figure 1-3 TOE10G-IP Multisession Demo Environment Setup on ZC706

Note: Test result in this document is captured by using following test environment.

[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html

[2] 10-Gigabit SFP+ DAC cable
http://www.netgear.com/business/products/switches/modules-accessories/axc761.aspx

[3] PC: Motherboard Z170-K, 32 GB RAM, 64-bit Windows7 OS, CPU i7-6700K@4.00 GHz

2 Demo description

Up to eight sessions can be operated at the same time for sending or receiving data with PC. Each session can be set transfer direction from 4-bit GPIO DIPSW on FPGA board. One bit is used to set for two sessions as follows.

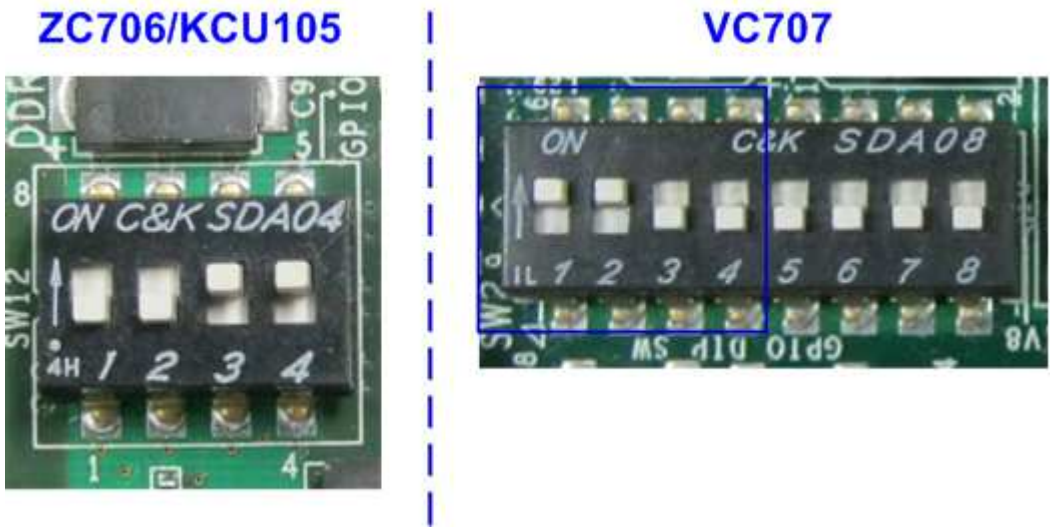

Figure 2-1 4-bit DIPSW in the demo

GPIO SW	ON	OFF
1	Port#4000 and #4001 receive data from PC	Port#4000 and #4001 send data to PC
2	Port#4002 and #4003 receive data from PC	Port#4002 and #4003 send data to PC
3	Port#4004 and #4005 receive data from PC	Port#4004 and #4005 send data to PC
4	Port#4006 and #4007 receive data from PC	Port#4006 and #4007 send data to PC

Table 2-1 4-bit DIPSW Definition

4-bit LED is used to show hardware status. The definition of LED on FPGA development board is described in Table 2-2.

GPIO LED	ON/BLINK	OFF
0	ON: IP initialize complete	Not complete. Please check that StartSW (CenterSW) has already been pressed and confirm IP address setting on PC that is correct.
1/R	BLINK: Timeout is found in some session.	Normal operation
2/C	N/A	N/A
3/L	ON: Connection of some sessions are established	No operation

Table 2-2 LED Definition

3 Demo setup

To set up the demo, please follow these steps.

1) Insert jumper to enable SFP+ (J17 for ZC706, or J6 for VC707/KCU105), as shown in Figure 3-1.

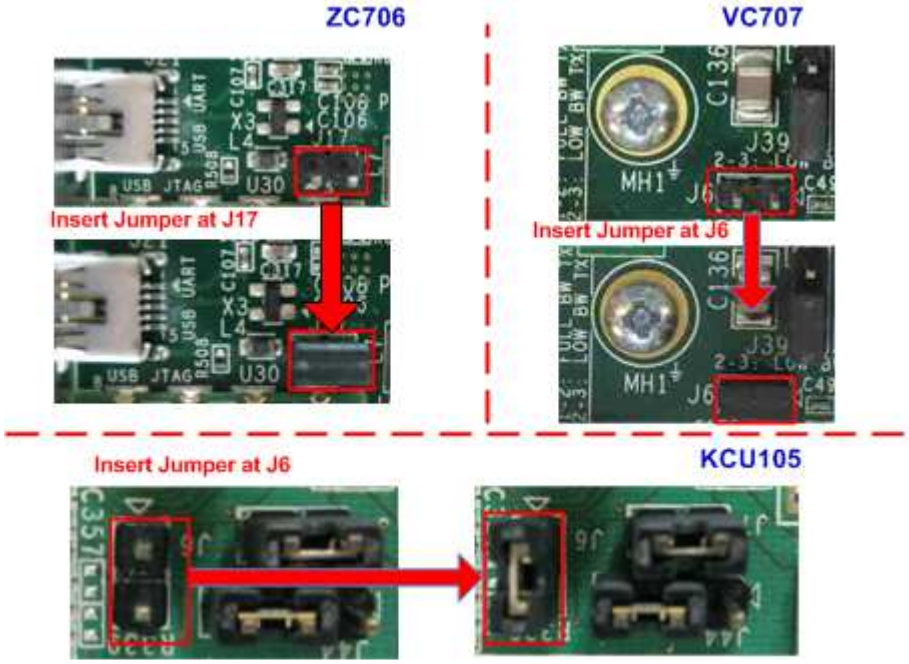

Figure 3-1 Insert jumper to enable SFP+

2) Set up board option
   a) For ZC706 board only, set SW11="00000" to configure PS from JTAG and set SW4="01" to connect JTAG with USB-to-JTAG interface, as shown in Figure 3-2 - Figure 3-3.

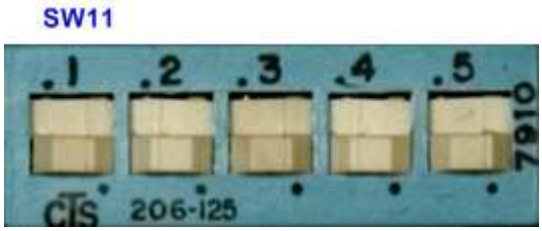

Figure 3-2 SW11 setting to configure PS from JTAG on ZC706 board

Figure 3-3 SW4 setting to use USB-to-JTAG on ZC706 board

3) Connect micro USB cable from FPGA development board to PC, and connect power supply to FPGA development board.
4) Insert 10-Gigabit SFP+ DAC or SFP+ transceiver with optical cable between FPGA development board and PC.

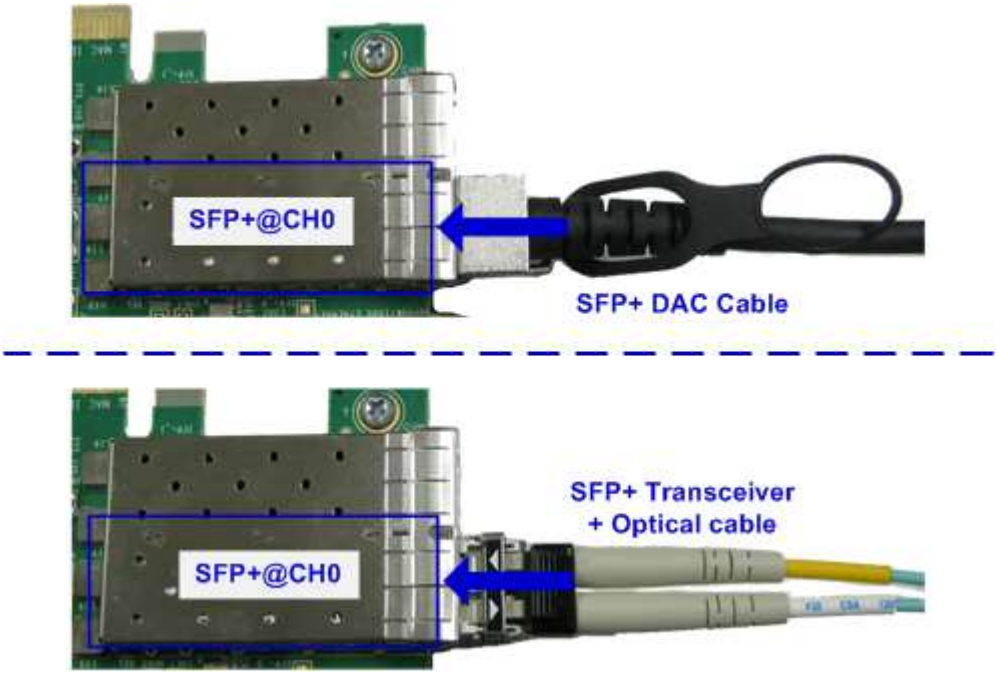

Figure 3-4 SFP+ cable connection

5) Setup network setting on PC, following Topic 3 in "dg_toe10gip_instruction_xilinx" document.
6) Power on FPGA development board.
7) Open iMPACT/Vivado to download bit file to FPGA development board, as shown in Figure 3-5.

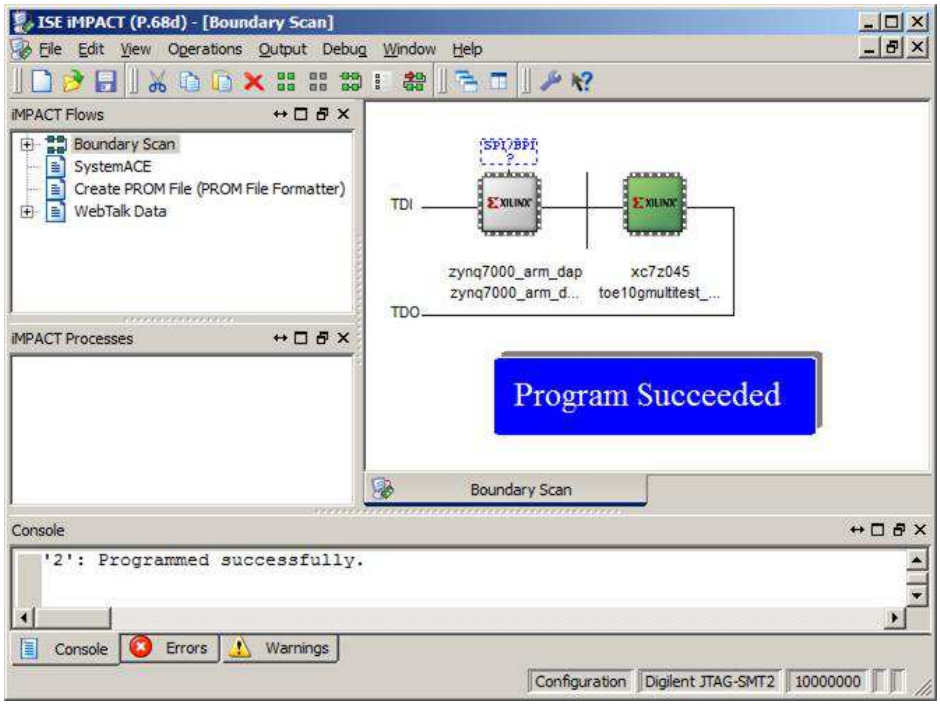

Figure 3-5 Programmed by iMPACT

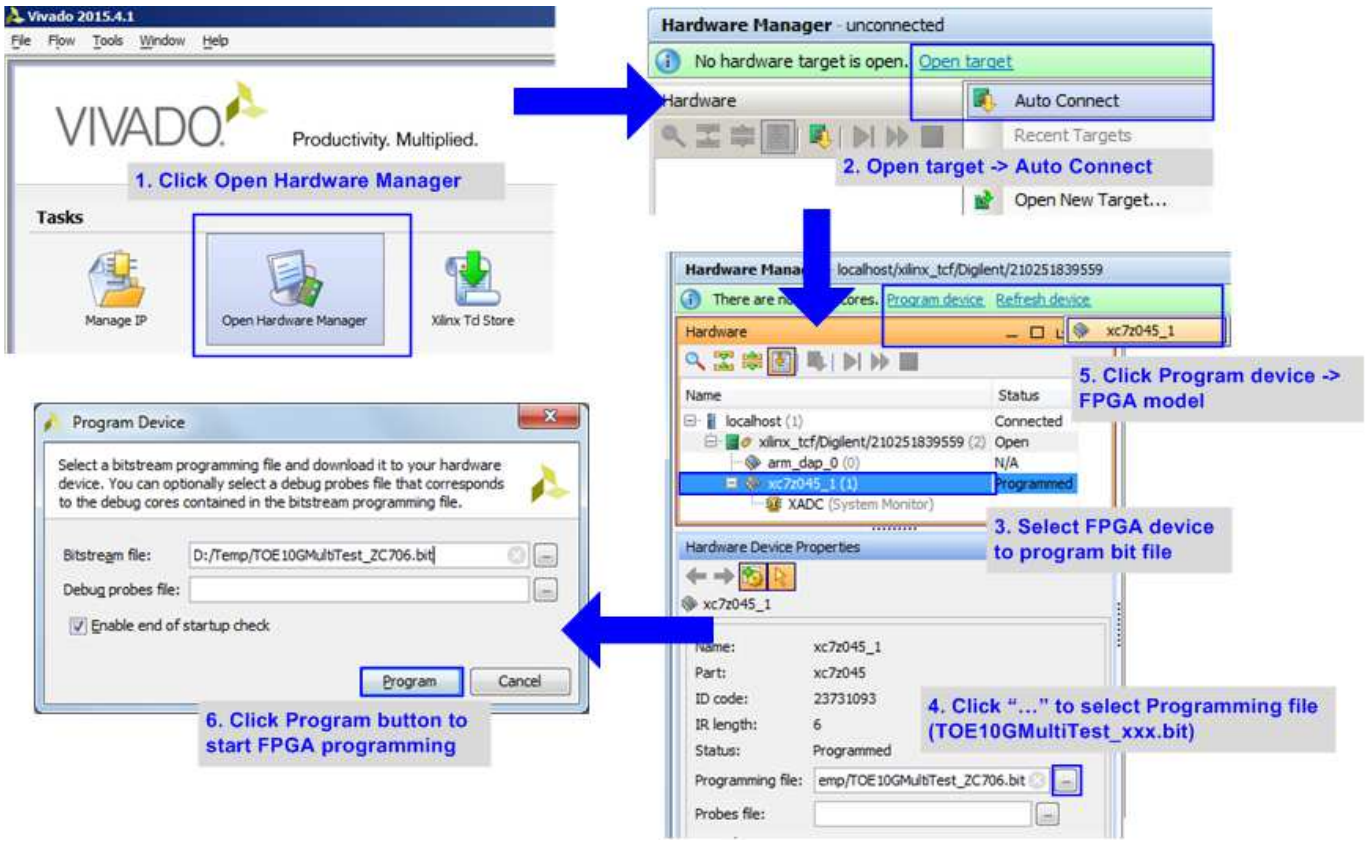

Figure 3-6 Programmed by Vivado

8) Press StartSW at Center-SW as shown in Figure 3-7 to initialize parameter in system, and then LED0 will turn on, as shown in Figure 3-8. Now system is ready to transfer data.

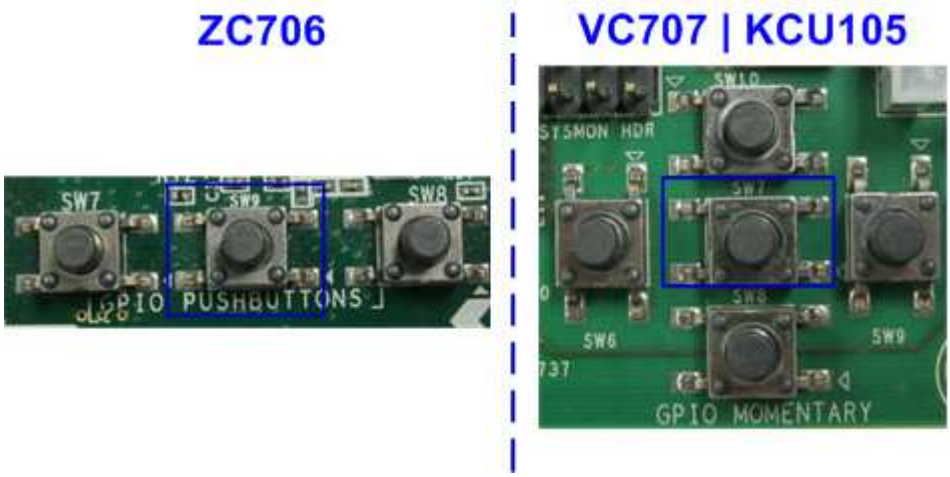

Figure 3-7 Center-SW on FPGA board

Figure 3-8 LED Status after push StartSW

Note: Demo transfer performance depends on Test PC performance within user platform that is high enough to send and receive 10-Gigabit data through Ethernet.

4 Run the demo

Please confirm that LED0 status now is ON to confirm that IP completes initialization process. In this reference design, “tcpdatatest” application is called in client mode to establish the new connection and send/receive data with the server which is implemented by TOE10G-IP. More details to run send or receive data test in each session are described as follows.

4.1 Send data test

This topic describes the step to run data sending test from FPGA to PC. Transfer size is fixed to be 32 GB. User can run up to eight sessions at the same time by running eight “tcpdatatest” with setting port number to be 4000 – 4007. DIPSW of selected port must be set to ‘0’ for send data test.

Type following command to run “tcpdatatest” in this test.
>> tcpdatatest c r 192.168.7.42 <4000-4007> 0 1

LED3 will turn on to show that port 4000-4007 is established. On PC console, total transfer size will be displayed every second. Test performance will be displayed after end of operation.

Figure 4-1 shows the example when running send data test by using Port#4000. DIPSW bit 1 must be set to ‘0’. Performance is about 1/4 times of standard demo because the IP in this demo uses only 4Kbyte buffer size while standard demo uses 64 Kbyte buffer size.

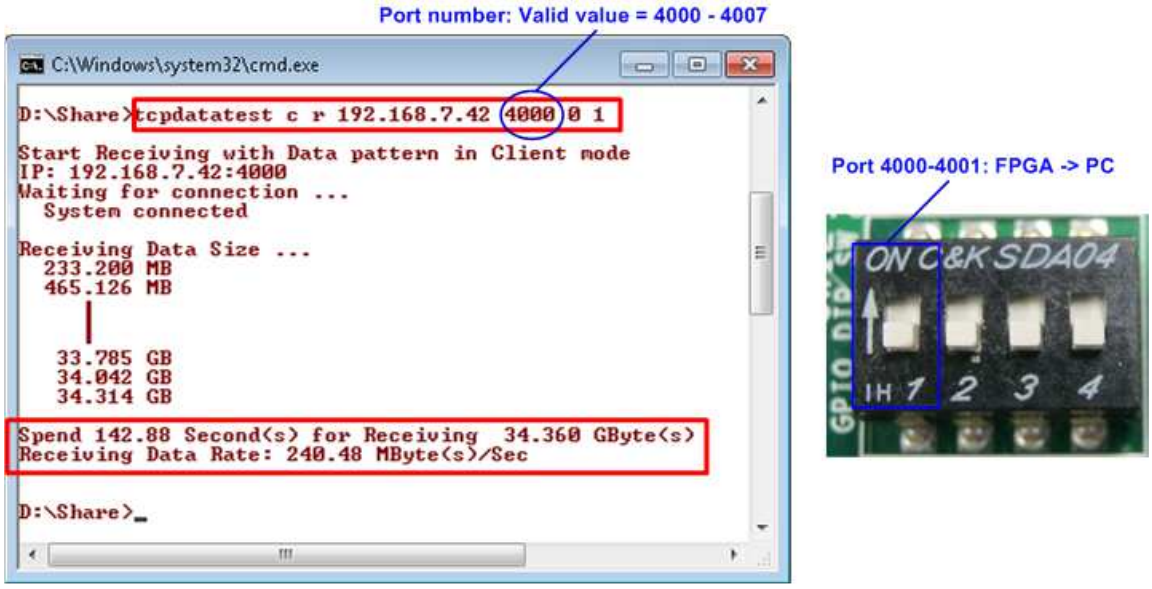

Figure 4-1 Send data test by using Port#4000 and DIPSW setting

Figure 4-2 shows the example when running send data test by using 8 sessions (Port 4000 – 4007) at the same time. Bit1-4 of DIPSW must be all set to '0'. Performance in Figure 4-3 for one session is about 145-147 MB/sec, so total performance is about 1160 MB/sec.

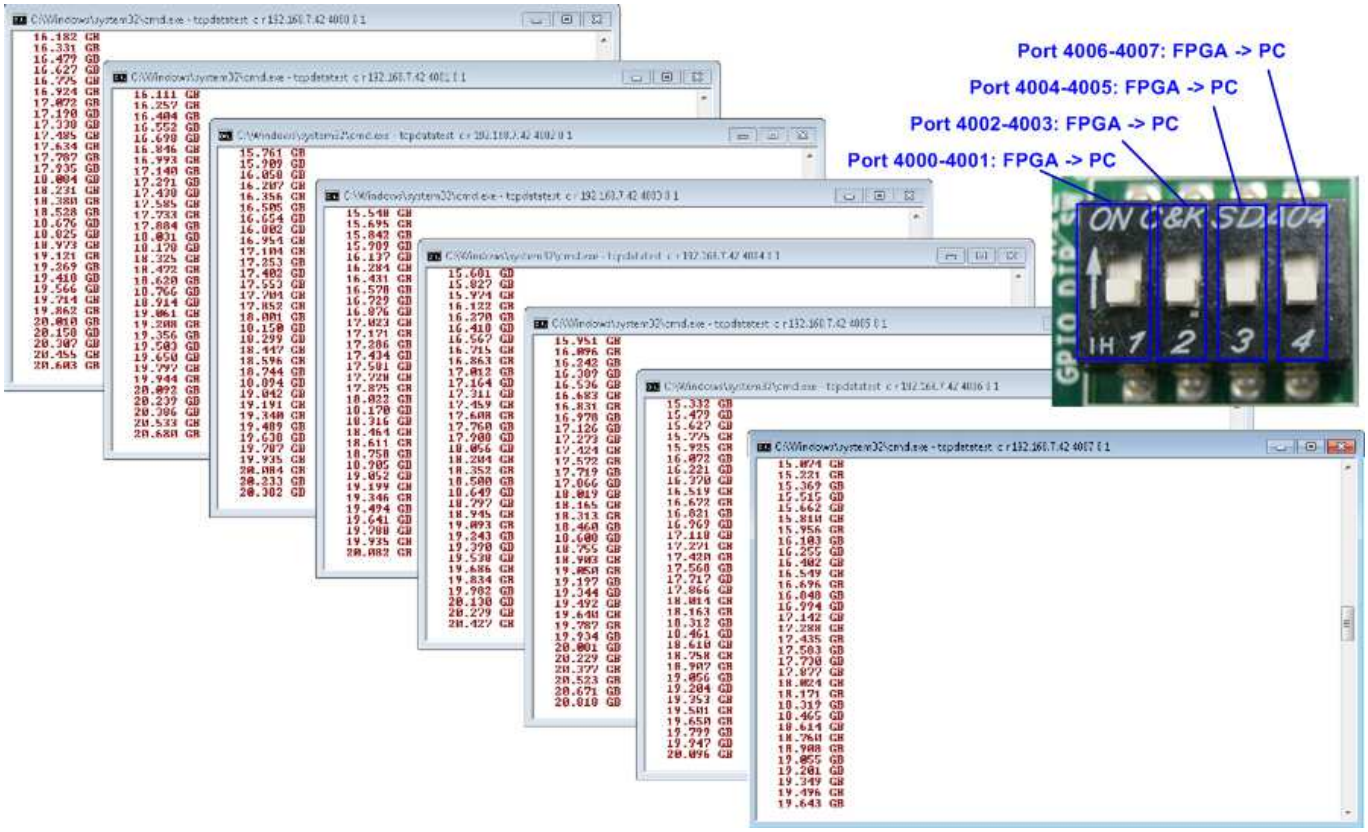

Figure 4-2 Send data test when running 8 sessions at the same time

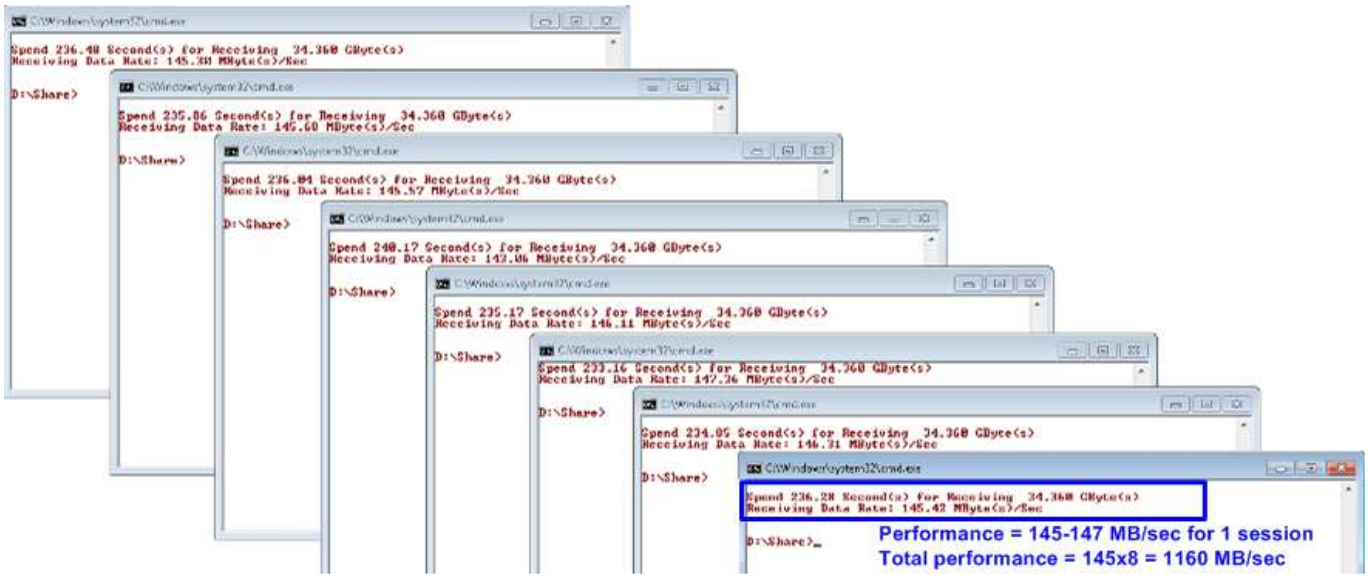

Figure 4-3 Performance when run send data test using 8 sessions at the same time

Figure 4-4 shows the example when running send data test by using 4 sessions (Port 4000 – 4003) at the same time. Performance of one session is about 216-223 MB/sec which is about 10% less than running only one session in Figure 4-1.

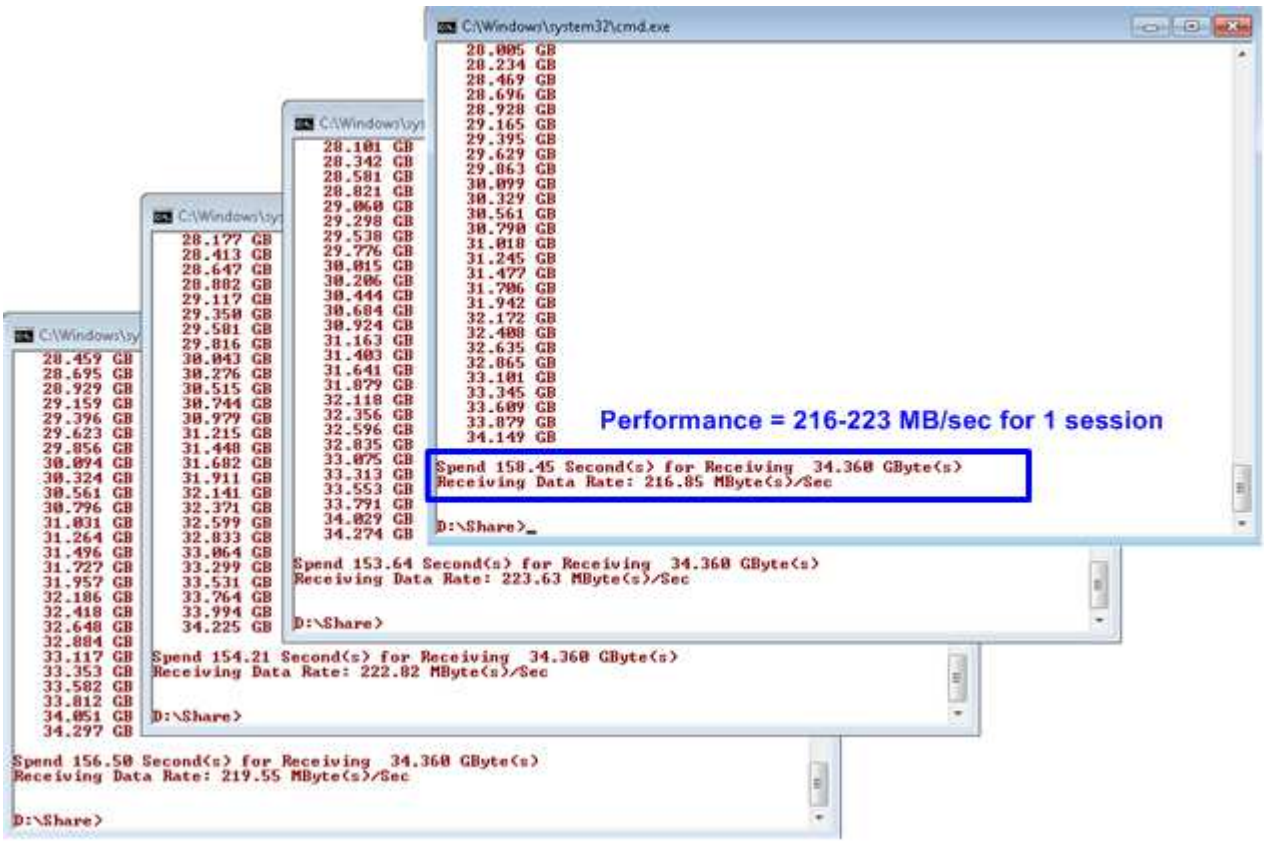

Figure 4-4 Performance when run send data test using 4 sessions at the same time

4.2 Receive data test

This topic describes the step to run the test to receive data from PC. User can set total transfer size from application. Up to eight sessions can run at the same time by running eight "tcpdatatest" with setting port number to be 4000 – 4007. DIPSW of selected port must be set to '1' for receive data test.

Type following command to run "tcpdatatest" in this test.
>> tcpdatatest c t 192.168.7.42 <4000-4007> <byte length> 1

LED3 will turn on to show that port 4000-4007 is established. On PC console, total transfer size will be displayed every second. Test performance will be displayed after end of operation.

Figure 4-5 shows the example when running receive data test by using Port#4000. DIPSW bit 1 must be set to '1'. Performance is about 1/4 times of standard demo because the IP in this demo uses only 4Kbyte buffer size while standard demo uses 64 Kbyte buffer size.

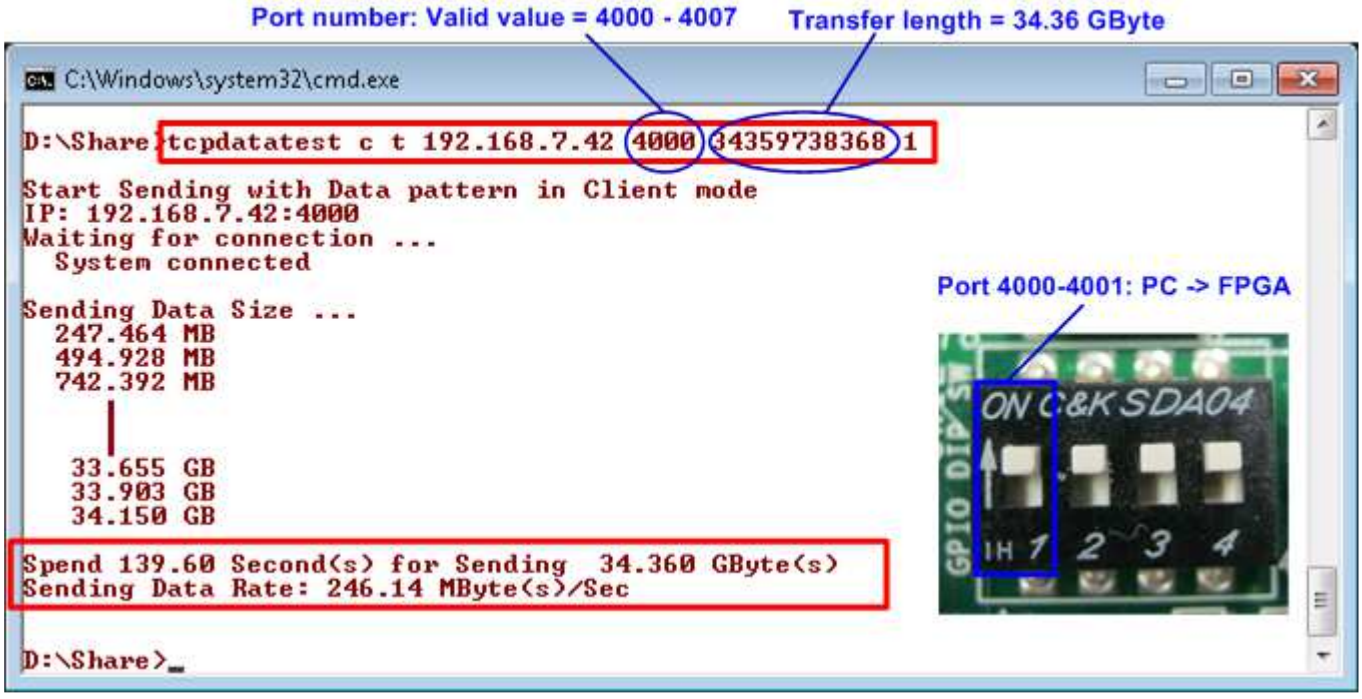

Figure 4-5 Receive data test by using Port#4000 and DIPSW setting

Figure 4-6 shows the example when running send data test by using 8 sessions (Port 4000 – 4007) at the same time. Bit1-4 of DIPSW must be all set to '1'. Performance in Figure 4-7 for one session is about 146-150 MB/sec, so total performance is about 1168 MB/sec.

Figure 4-6 Receive data test when running 8 sessions at the same time

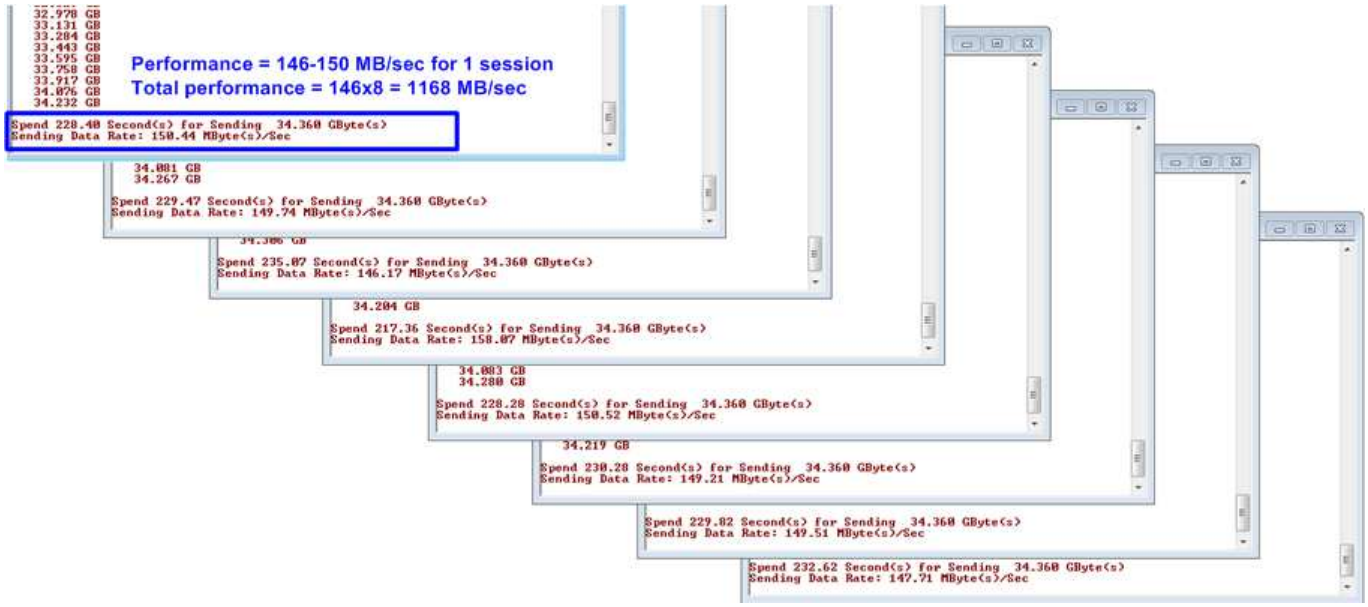

Figure 4-7 Performance when run receive data test using 8 sessions at the same time

Figure 4-8 shows the example when running send data test by using 4 sessions (Port 4000 – 4003) at the same time. Performance of one session is about 195-197 MB/sec which is about 20% less than running only one session in Figure 4-5.

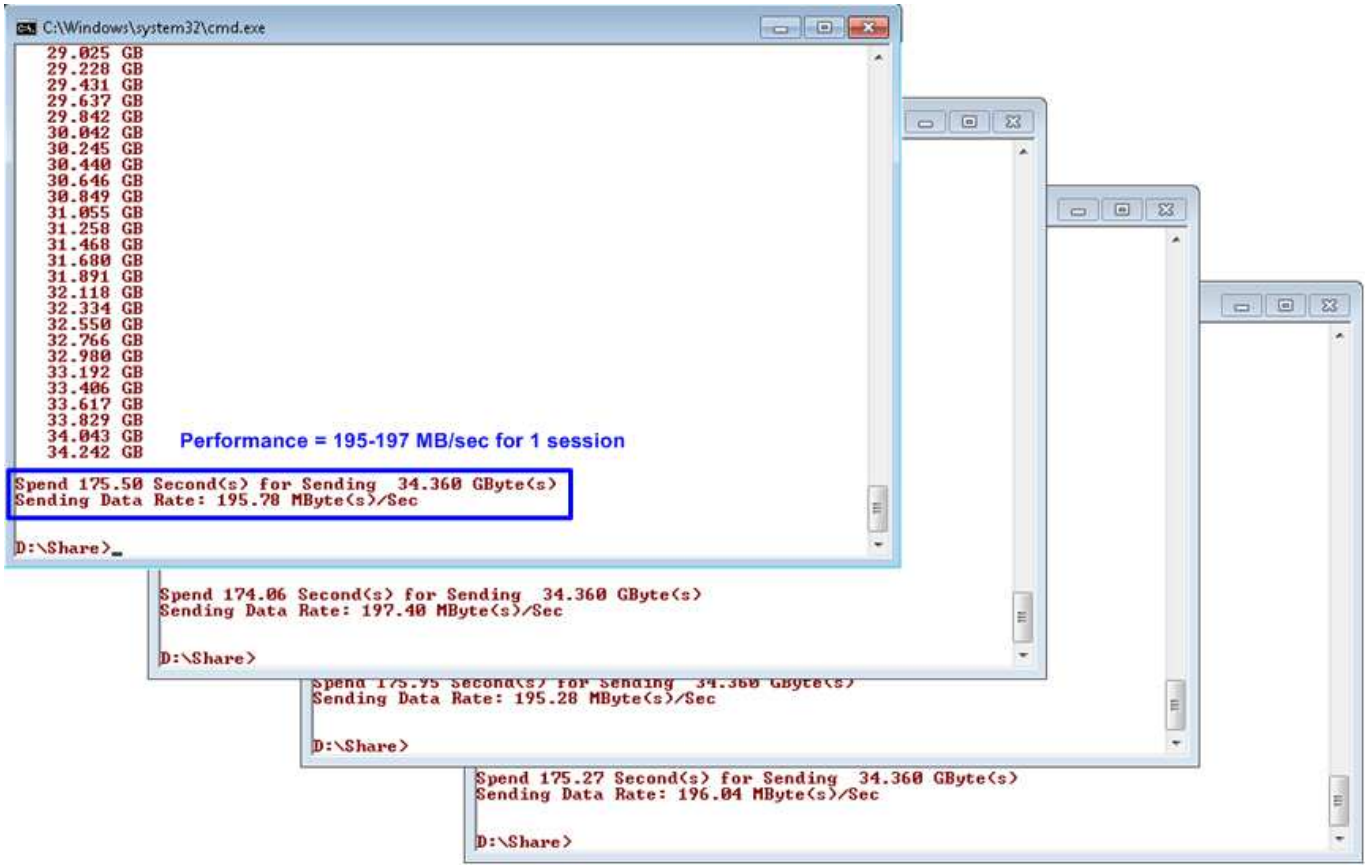

Figure 4-8 Performance when run receive data test using 4 sessions at the same time

4.3 Send and Receive data test

User can set 4-bit DIPSW to be different value to run send and receive data test by using different port number.

Figure 4-9 and Figure 4-10 shows the test result when running send and receive data test by using two and eight sessions sequentially.

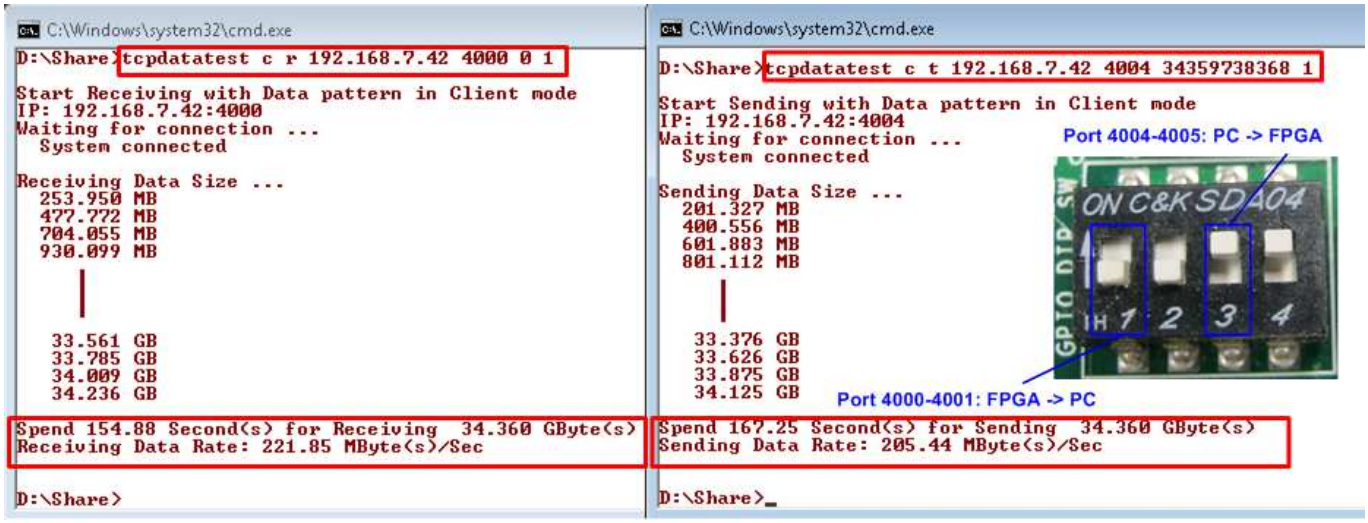

Figure 4-9 Send/Receive data test using two sessions

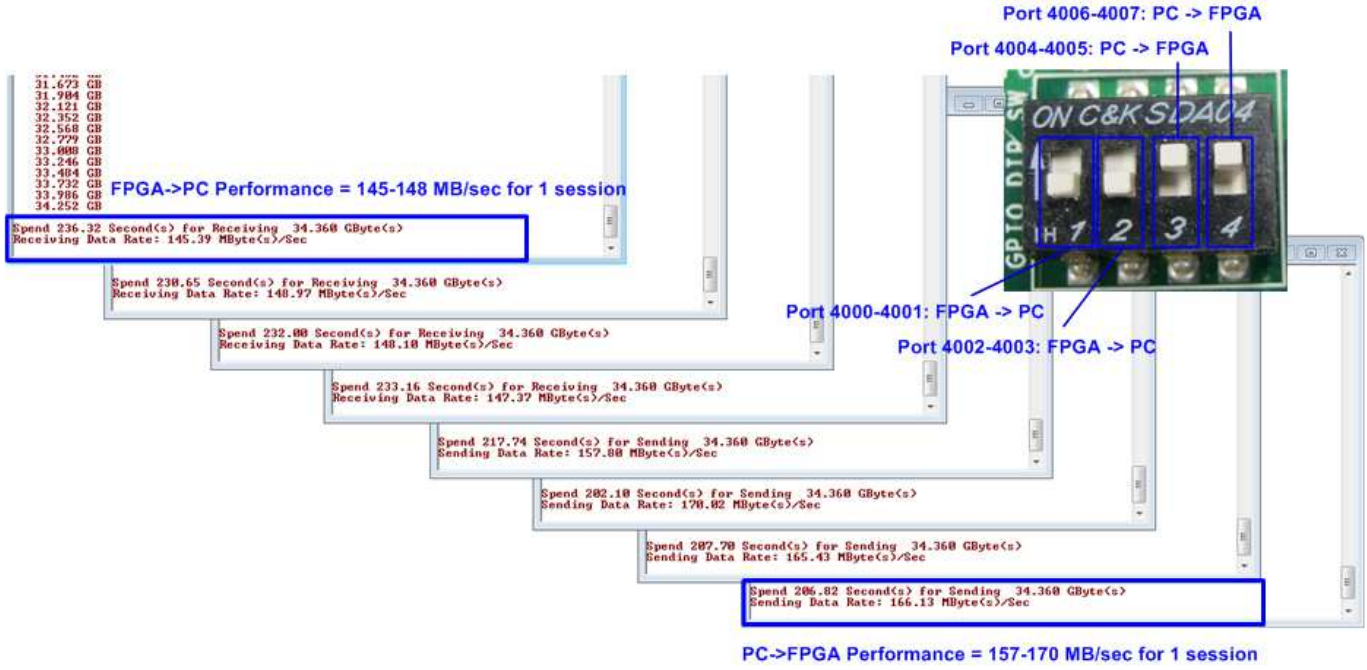

Figure 4-10 Send/Receive data test using eight sessions

5 Revision History

Revision	Date	Description
1.0	8-Nov-16	Initial version release