FPGA set up for TOE/UDP10G-IP with CPU Demo

FPGA set up for TOE/UDP10G-IP with CPU Demo

Rev3.1 15-Jun-23

This document describes how to setup FPGA board and prepare the test environment for running TOE10G-IP or UDP10G-IP demo. The user can setup two test environments for transferring TCP or UDP data via 10Gb Ethernet connection by using TOE10G-IP or UDP10G-IP, as shown in Figure 1-1.

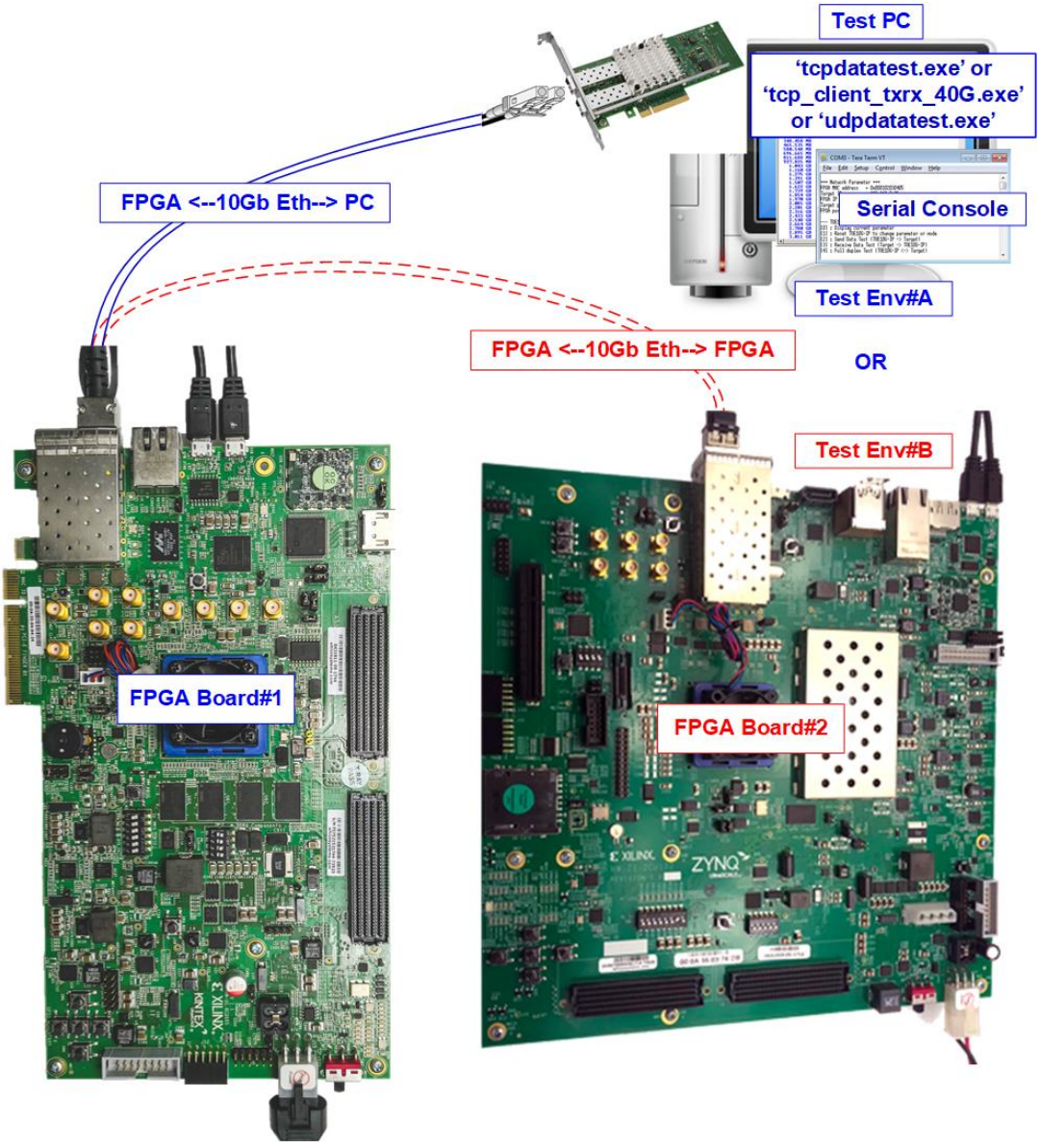

Figure 1-1 Two test environments for running the demo

First uses one FPGA board and Test PC with 10Gb Ethernet card for transferring the data. TestPC runs test application, i.e. tcpdatatest (half-duplex test for TOE10G-IP), tcp_client_txrx_40G (full-duplex test for TOE10G-IP) or udpdatatest (test application for UDP10G-IP). Also, Serial console is run on Test PC to be user interface console.

Second uses two FPGA boards which may be different board. Both boards run TOE10G-IP or UDP10G-IP demo with assigning the different initialization mode (Client for Server) for transferring data.

1 Test environment setup when using FPGA and PC

Before running the test, please prepare following test environment.

- FPGA development boards: ZC706/ZCU102/ZCU106/KCU105/VCU118 board
- PC with 10 Gigabit Ethernet or connecting with 10 Gigabit Ethernet card
- 10 Gb Ethernet cable:
  a) 10 Gb SFP+ Passive Direct Attach Cable (DAC) which has 1-m or less length
  b) 10 Gb SFP+ Active Optical Cable (AOC)
  c) 2x10 Gb SFP+ transceiver (10G BASE-R) with optical cable (LC to LC, Multimode)
  d) For VCU118 board only, QSFP+ to four SFP+ cable
- micro USB cable for programming FPGA connecting between FPGA board and PC
- mini USB cable (ZC706) or micro USB cable (ZCU102/ZCU106/KCU105/VCU118) connecting between FPGA board and PC for Serial console.
- Test application provided by Design Gateway for running on Test PC:
  TOE10G-IP: “tcpdatatest.exe” and “tcp_client_txrx_40G.exe”
  UDP10G-IP: “udpdatatest.exe”
- Serial console software such as TeraTerm installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity and Stop=1.
- Vivado tool for programming FPGA, installed on PC

Note: Example hardware for running the demo is listed as follows.
[1] 10G Network Adapter: Intel X520-DA2
http://www.intel.com/content/www/us/en/network-adapters/converged-network-adapters/ethernet-x520-server-adapters-brief.html
[2] a) 10-Gigabit SFP+ AOC cable (AOC-S1S1-001)
https://www.10gtek.com/10gsfp+aoc
b) 40-Gigabit QSFP to 4x10-Gigabit SFP+ cable
https://www.finisar.com/active-optical-cables/fcbn510qe2cxx
[3] PC: Motherboard ASUS Z170-K, 32 GB RAM, and 64-bit Windows7 OS

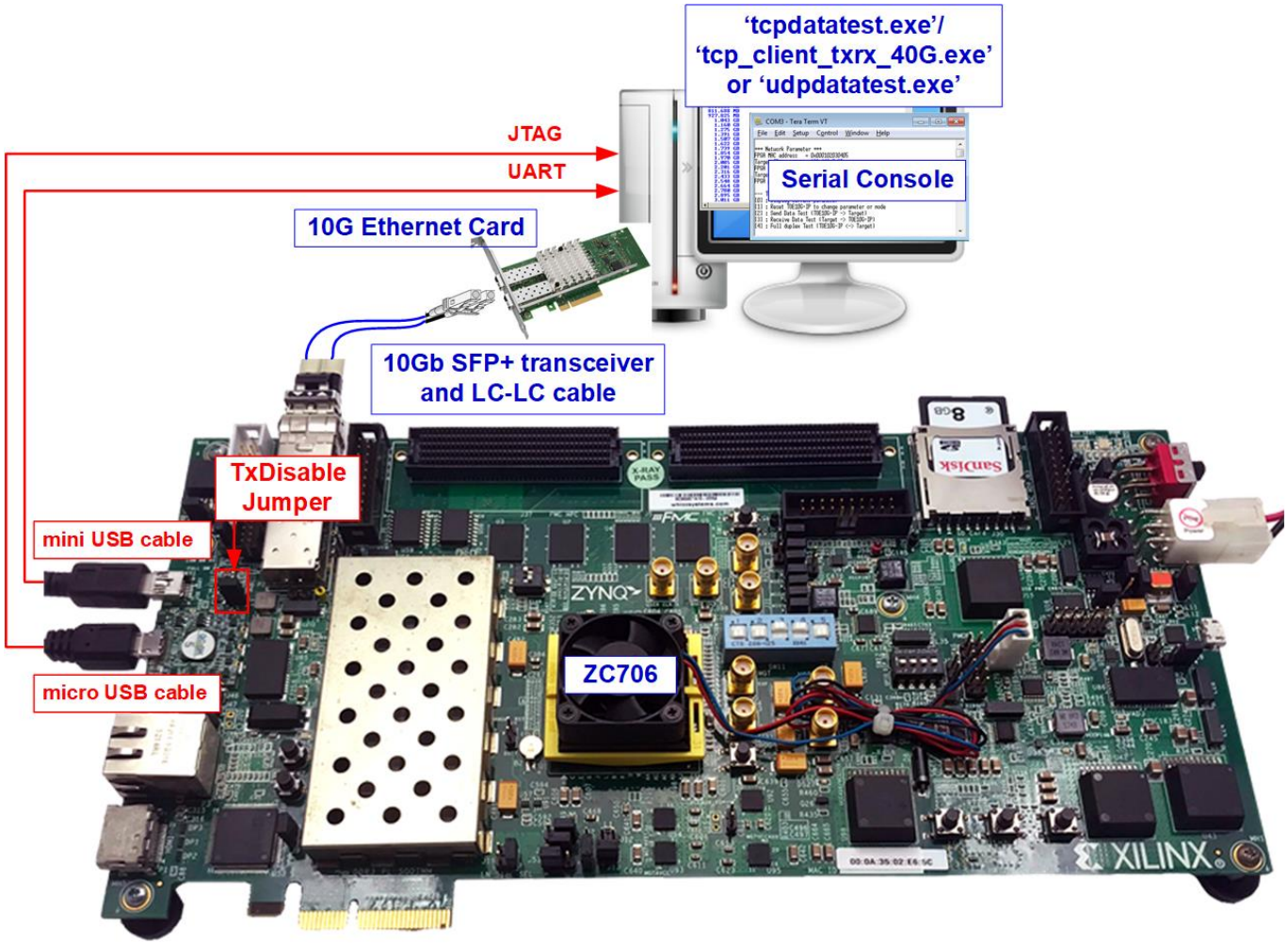

Figure 1-1 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZC706

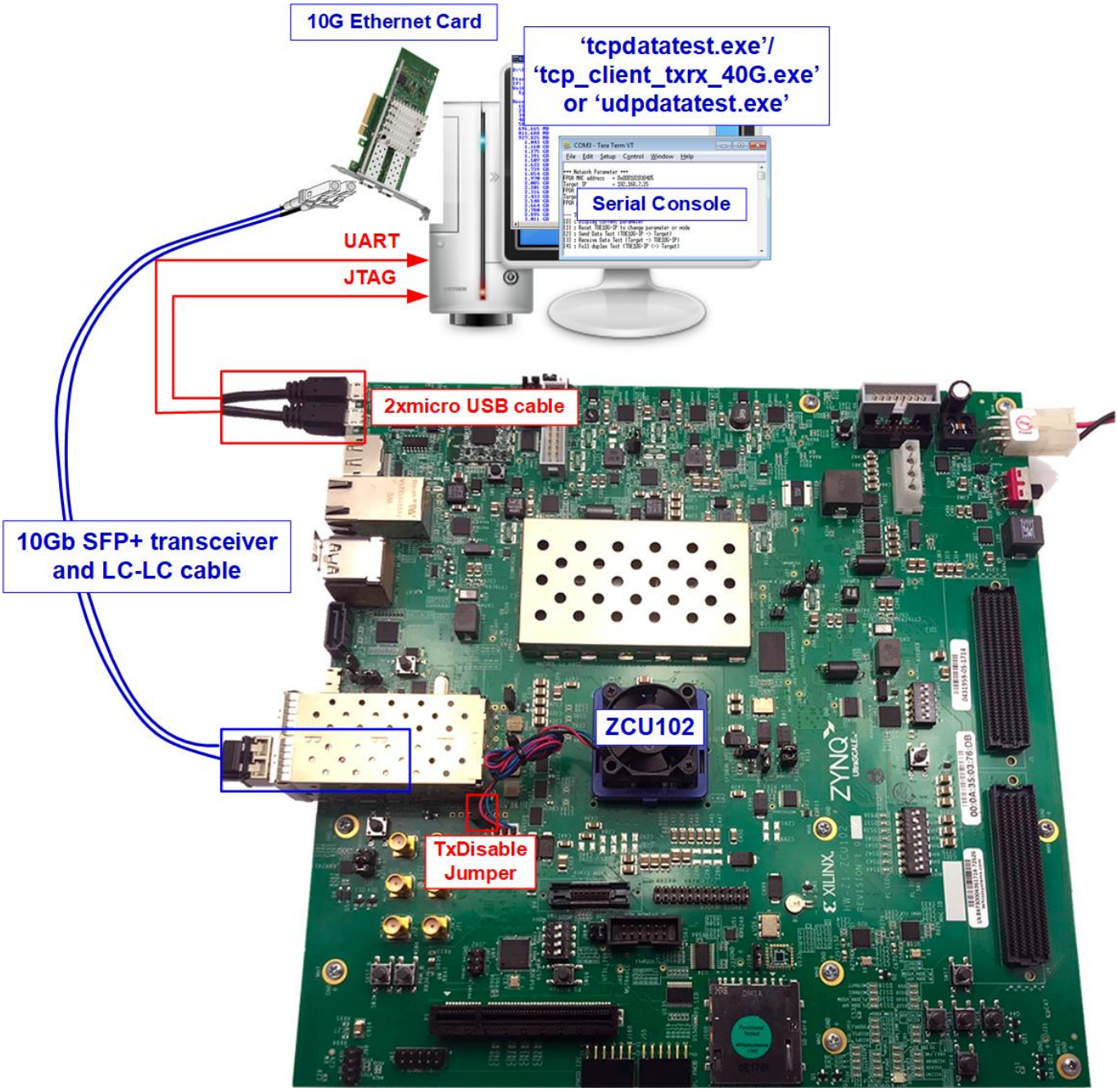

Figure 1-2 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZCU102

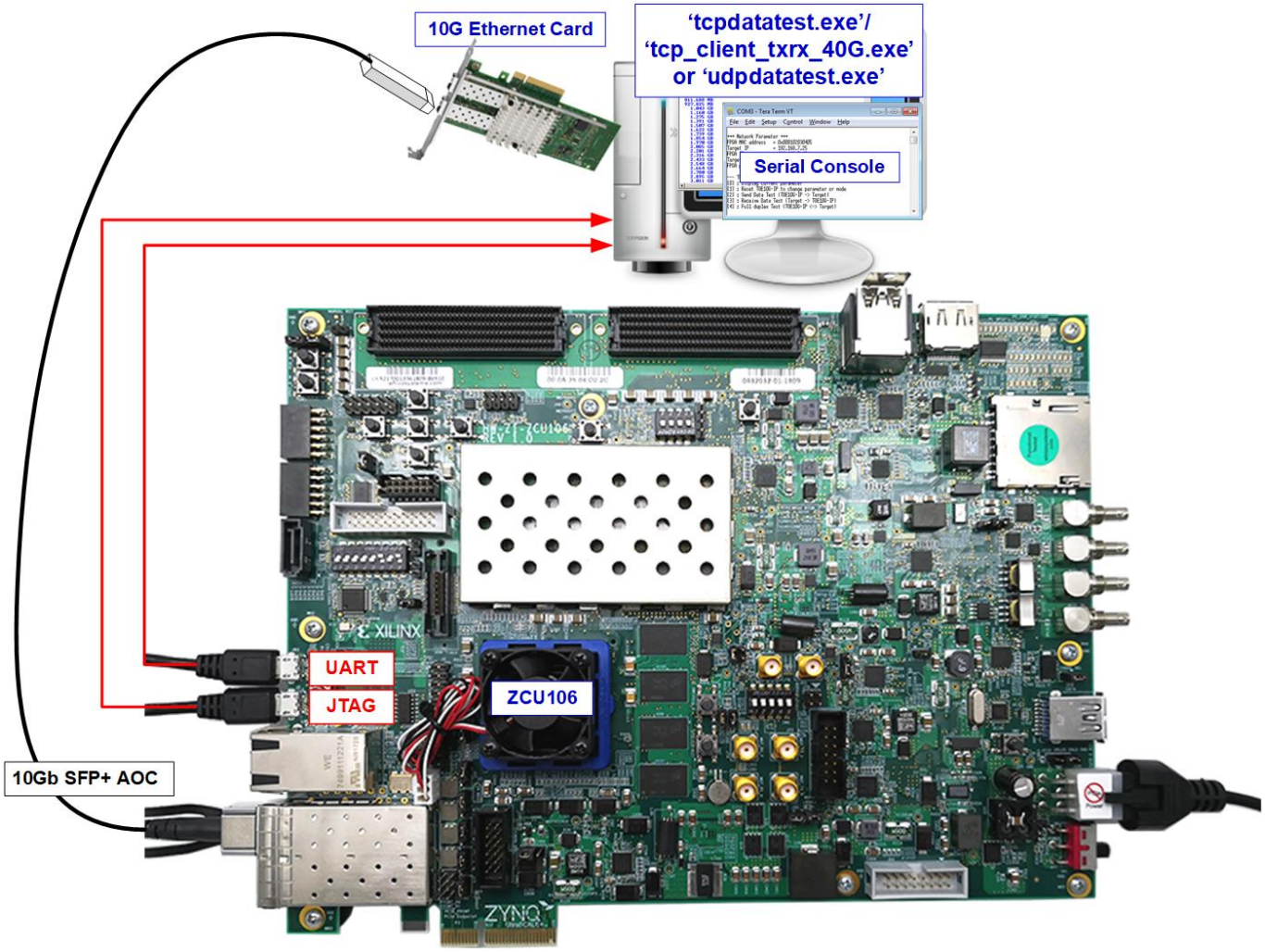

Figure 1-3 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on ZCU106

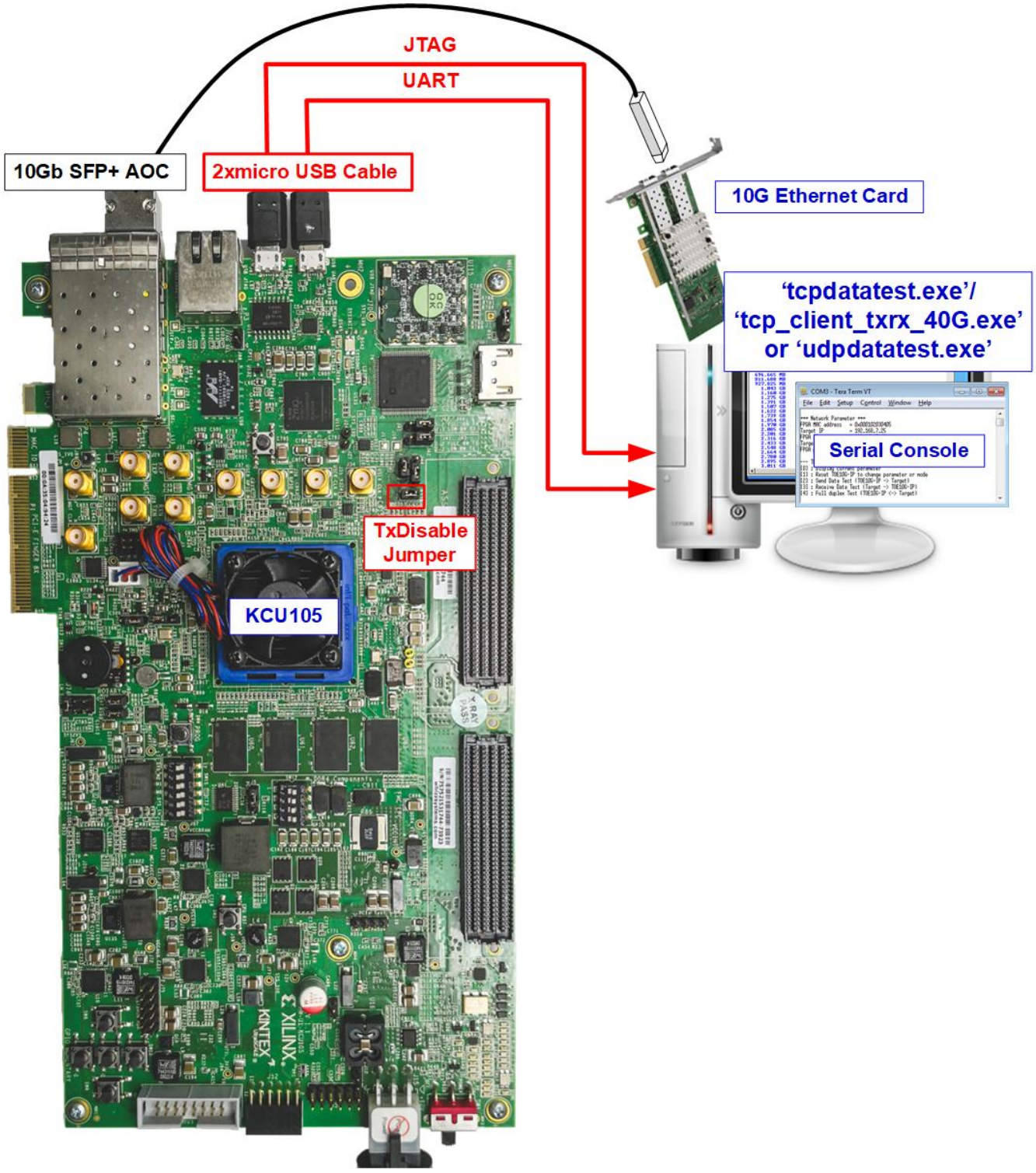

Figure 1-4 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on KCU105

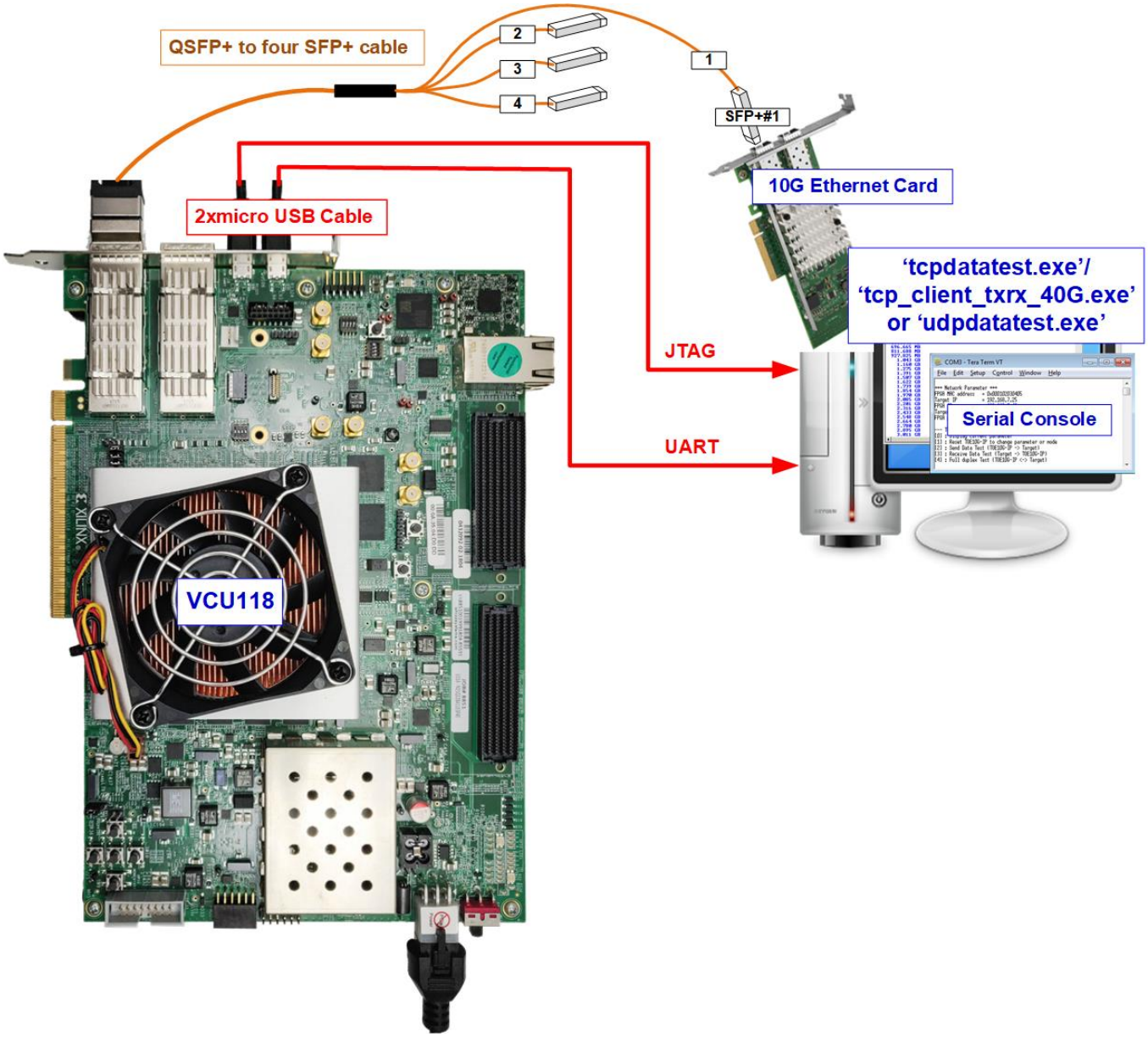

Figure 1-5 TOE10G-IP/UDP10G-IP with CPU demo (FPGA <-> PC) on VCU118

The step to setup test environment by using FPGA and PC is described in more details as follows.

1) Check DIPSW and jumper setting on FPGA board.
   a) Board setting on ZC706 board is shown in Figure 1-6.
      - Insert jumper to J17 to enable Tx SFP+
      - Set SW11 to configure PS from JTAG
      - Set SW4 to use USB-JTAG.

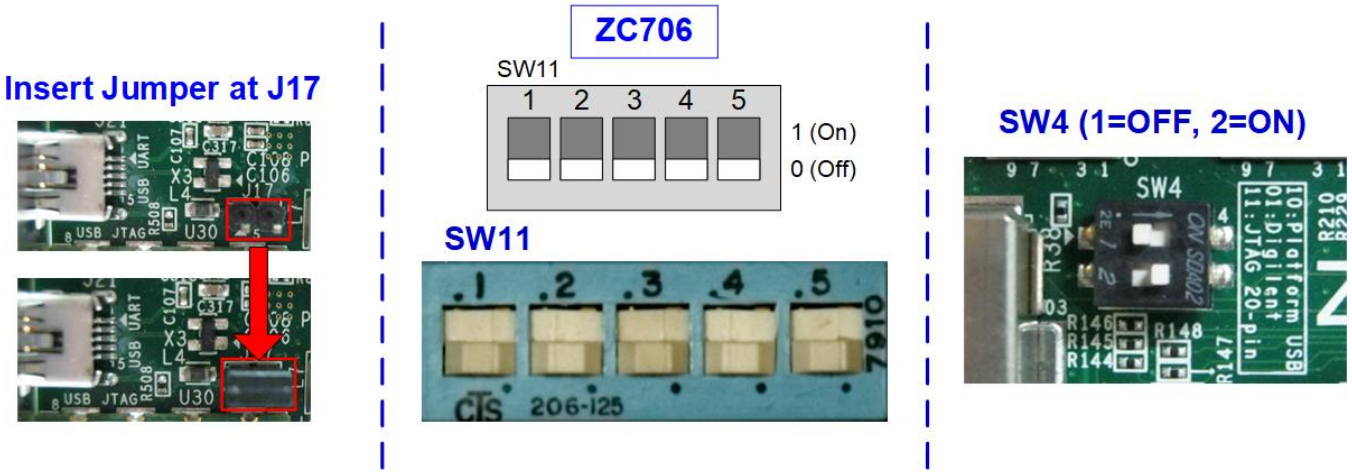

Figure 1-6 ZC706 board setting

   b) Board setting on ZCU102/ZCU106 board is shown in Figure 1-7.
      - Set SW6=all ONs to use USB-JTAG
      - Only ZCU102, insert jumper to J16 to enable Tx SFP+

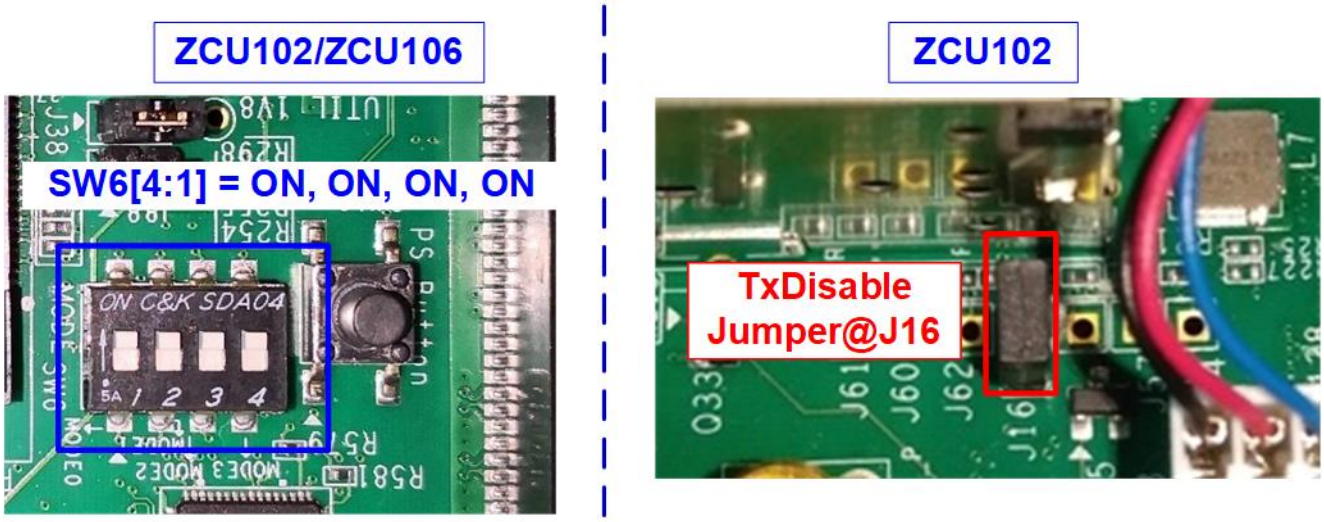

Figure 1-7 ZCU102 board setting

c) Board setting on KCU105 board is shown in Figure 1-8. Insert jumper to J6 to enable Tx SFP+.

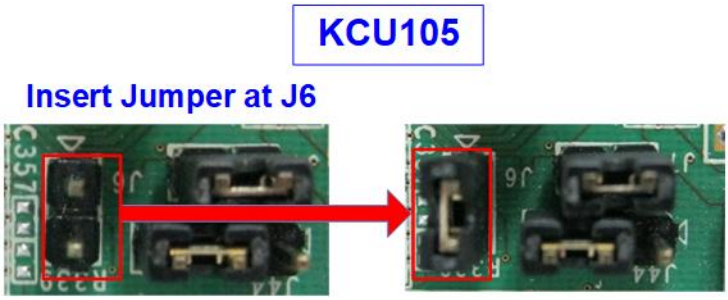

Figure 1-8 Insert jumper to enable SFP+ on KCU105

2) Connect micro USB cable from FPGA board to PC for JTAG programming.
3) Connect micro USB cable (ZCU102/KCU105/VCU118 board) or mini USB cable (ZC706 board) from FPGA board to PC for USB UART.
4) Connect power supply to FPGA development board.
5) Connect 10Gb Ethernet cable between FPGA board and PC.
   a) For ZCU102/ZCU106/KCU105/ZC706, insert 10 Gb SFP+ DAC (Length<1m), AOC or SFP+ transceiver with LC-LC cable. Some boards have many SFP connectors, use the channel as shown in Figure 1-9.

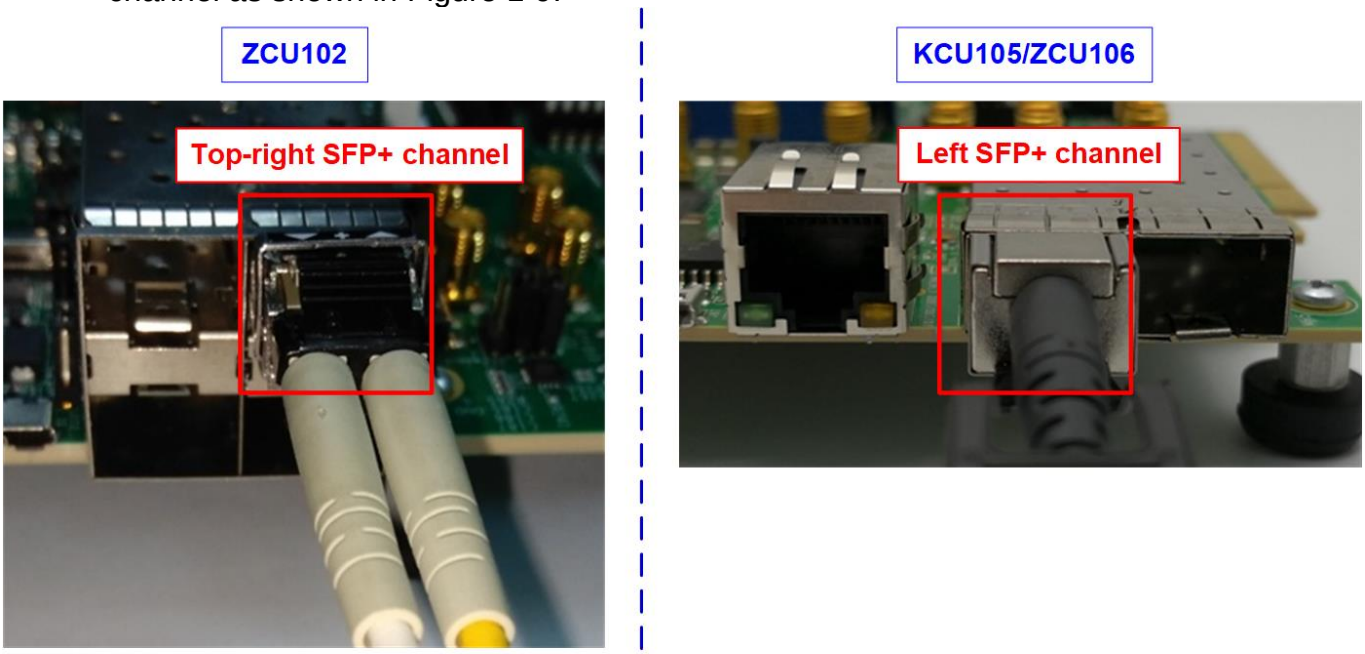

Figure 1-9 SFP+ channel using on ZCU102/ZCU106/KCU105 board

b) For VCU118, insert QSFP+ to 4 SFP+ cable between FPGA board and PC. Use SFP+ no.1 to connect to QSFP1, connector on the right side, as shown in Figure 1-10.

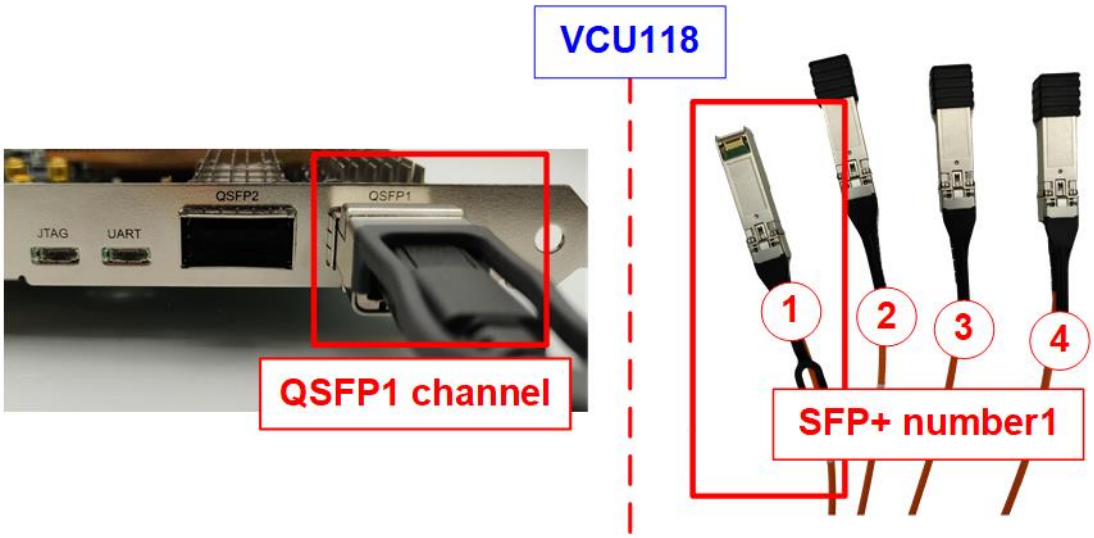

Figure 1-10 QSFP+ channel using on VCU118 board

6) Power on FPGA board.
7) Open Serial console. When connecting FPGA board to PC, many COM ports from FPGA connection are detected and displayed on Device Manager.
In case of KCU105/VCU118, select Standard COM port.
In case of ZCU102/ZCU106, select COM port number of Interface0.
On Serial console, use following setting: Baud rate=115,200, Data=8-bit, Non-Parity and Stop = 1.

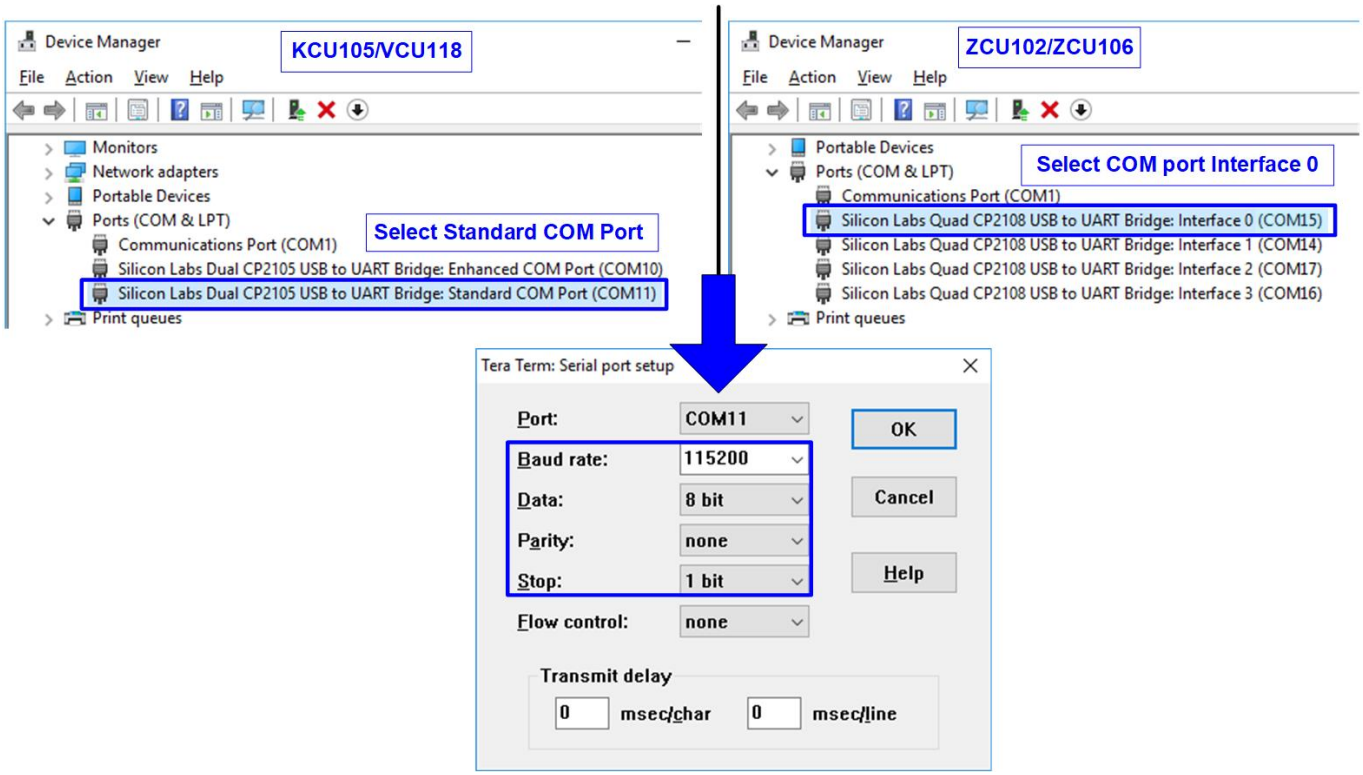

Figure 1-11 COM port number for Serial console

8) Download configuration file and firmware to FPGA board
   a) For ZCU102/ZCU106/ZC706 board, open Vivado TCL shell and change current directory to download folder which includes demo configuration file. Type "XXX10gtest_boardname.bat, as shown in Figure 1-12.

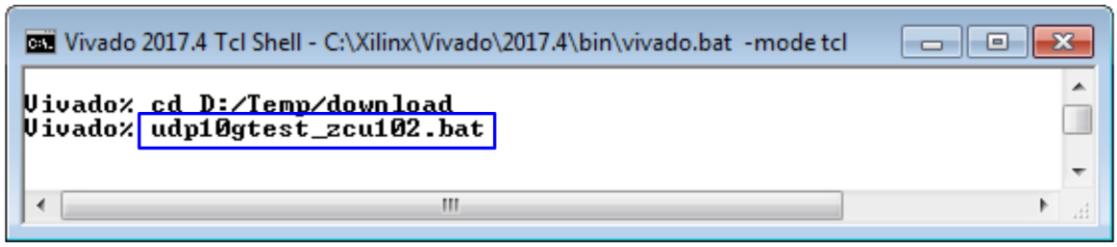

Figure 1-12 Example command script for download to ZCU102/ZCU106/ZC706 by Vivado tool

   b) For KCU105/VCU118 board, use Vivado tool to program configuration file, as shown in Figure 1-13.

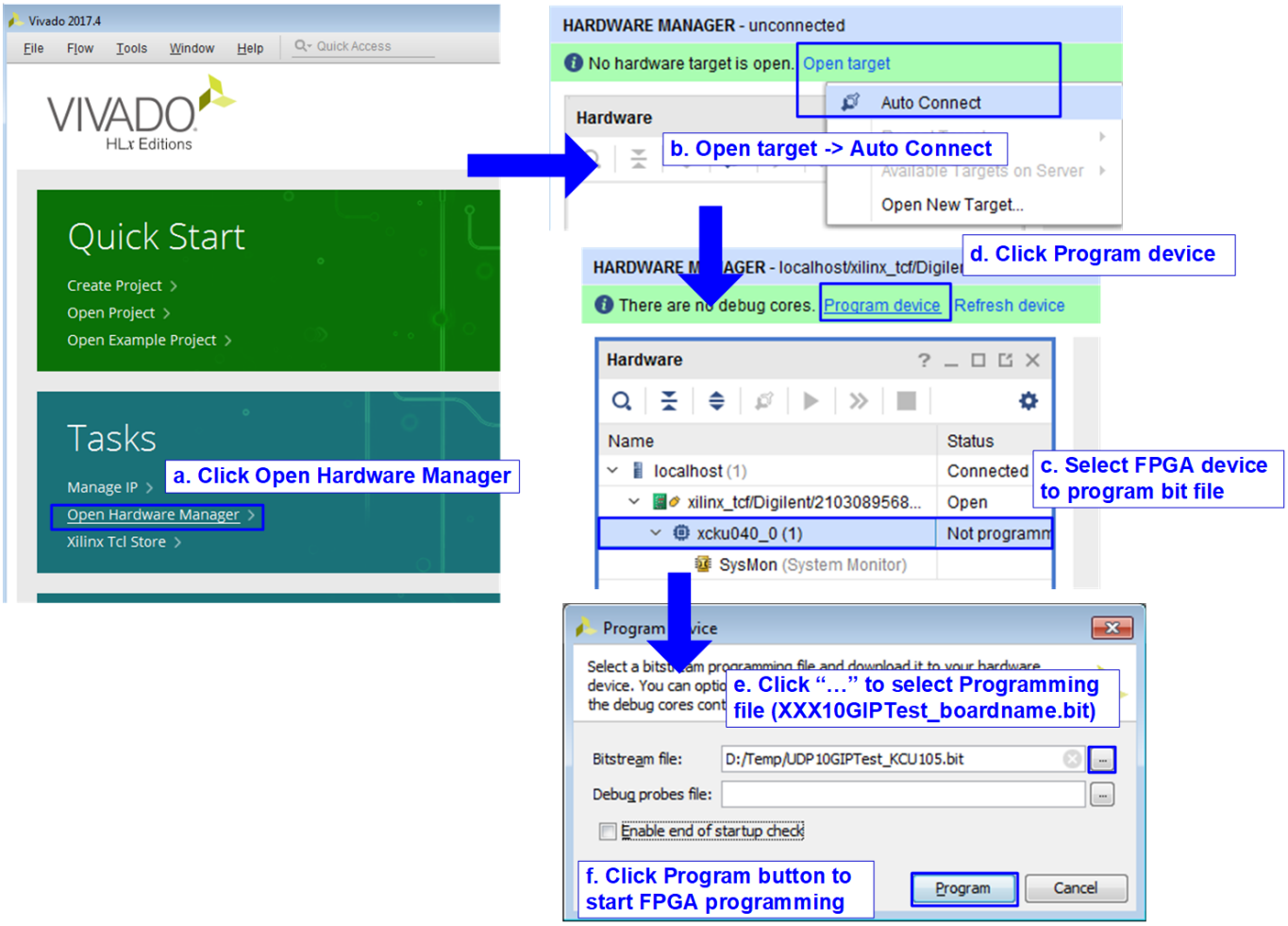

Figure 1-13 Program FPGA by Vivado

9) On Serial console, welcome message is displayed.
   i. Input '0' to initialize TOE10G-IP/UDP10G-IP in client mode (asking PC MAC address by sending ARP request).
   ii. Default parameter in client mode is displayed on the console.

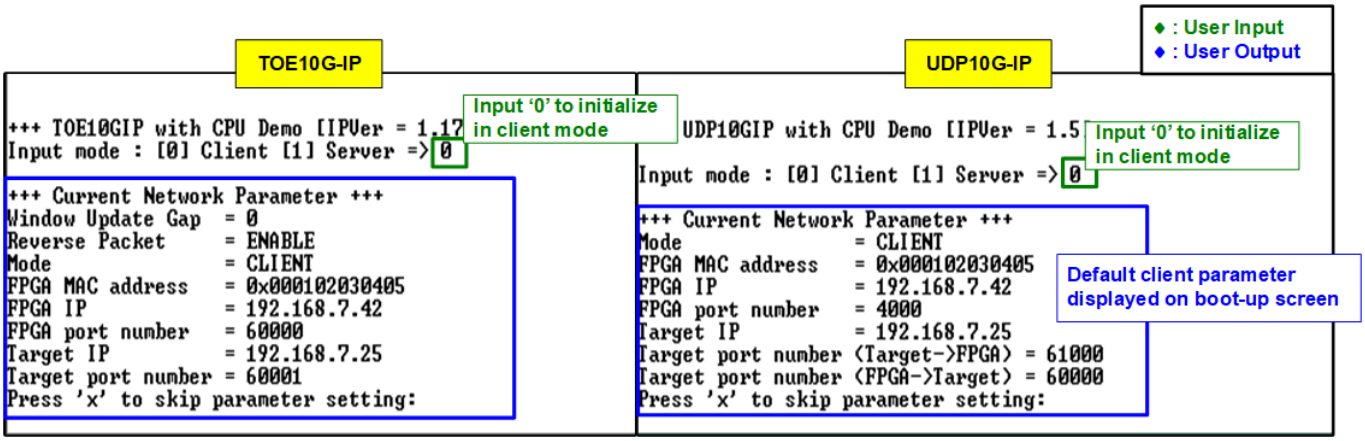

Figure 1-14 Message after system boot-up

If Ethernet connection has the problem and the status is linked down, the error message will be displayed on the console instead of welcome message, as shown in Figure 1-15.

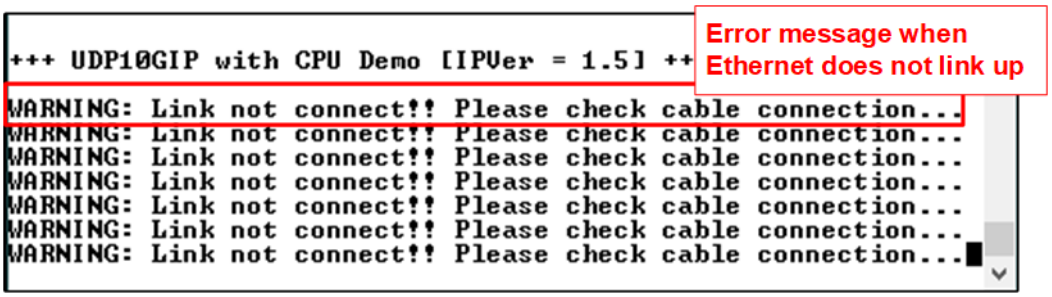

Figure 1-15 Error message when cable is linked down

iii. User enters 'x' to skip parameter setting for using default parameters to begin system initialization, as shown in Figure 1-16. If user enters other keys, the menu for changing parameter is displayed, similar to "Reset TCPIP/UDPIP parameters" menu. The example when running the main menu is described in "dg_toe10gip_cpu_instruction" or "dg_udp10gip_cpu_instruction" document.

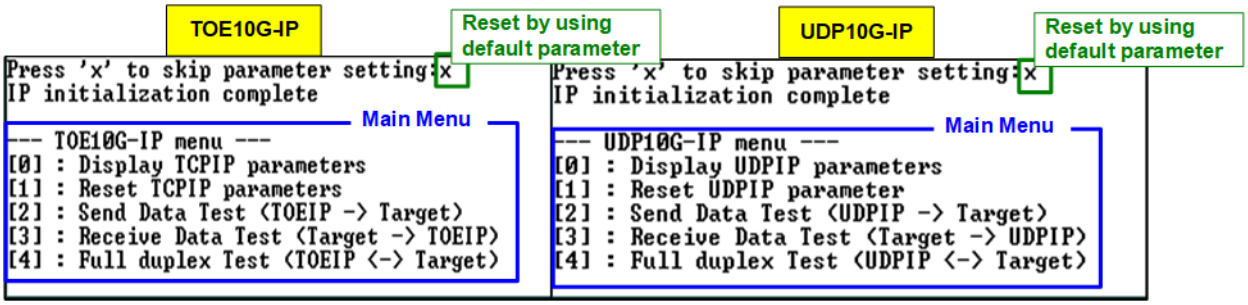

Figure 1-16 Initialization complete

Note: Transfer performance in the demo depends on Test PC resource in Test platform.

2 Test environment setup when using two FPGAs

Before running the test, please prepare following test environment.

- Two FPGA development boards which are the same board or different board, ZC706/ZCU102/ZCU106/KCU105/VCU118
- 10Gb Ethernet cable:
  a) 10 Gb SFP+ Active Optical Cable (AOC)
  b) 2x10 Gb SFP+ transceiver (10G BASE-R) with optical cable (LC to LC, Multimode)
  c) For VCU118, use QSFP+ to 4 SFP+ cable
- micro USB cables for programming FPGA, connecting between FPGA board and PC
- mini USB cable (ZC706 board) or micro USB cable (ZCU102/KCU105/VCU118 board) for Serial console, connecting between FPGA board and PC
- Serial console software such as TeraTerm, installed on PC. The setting on the console is Baudrate=115,200, Data=8-bit, Non-parity, and Stop=1.
- Vivado tool for programming FPGA, installed on PC

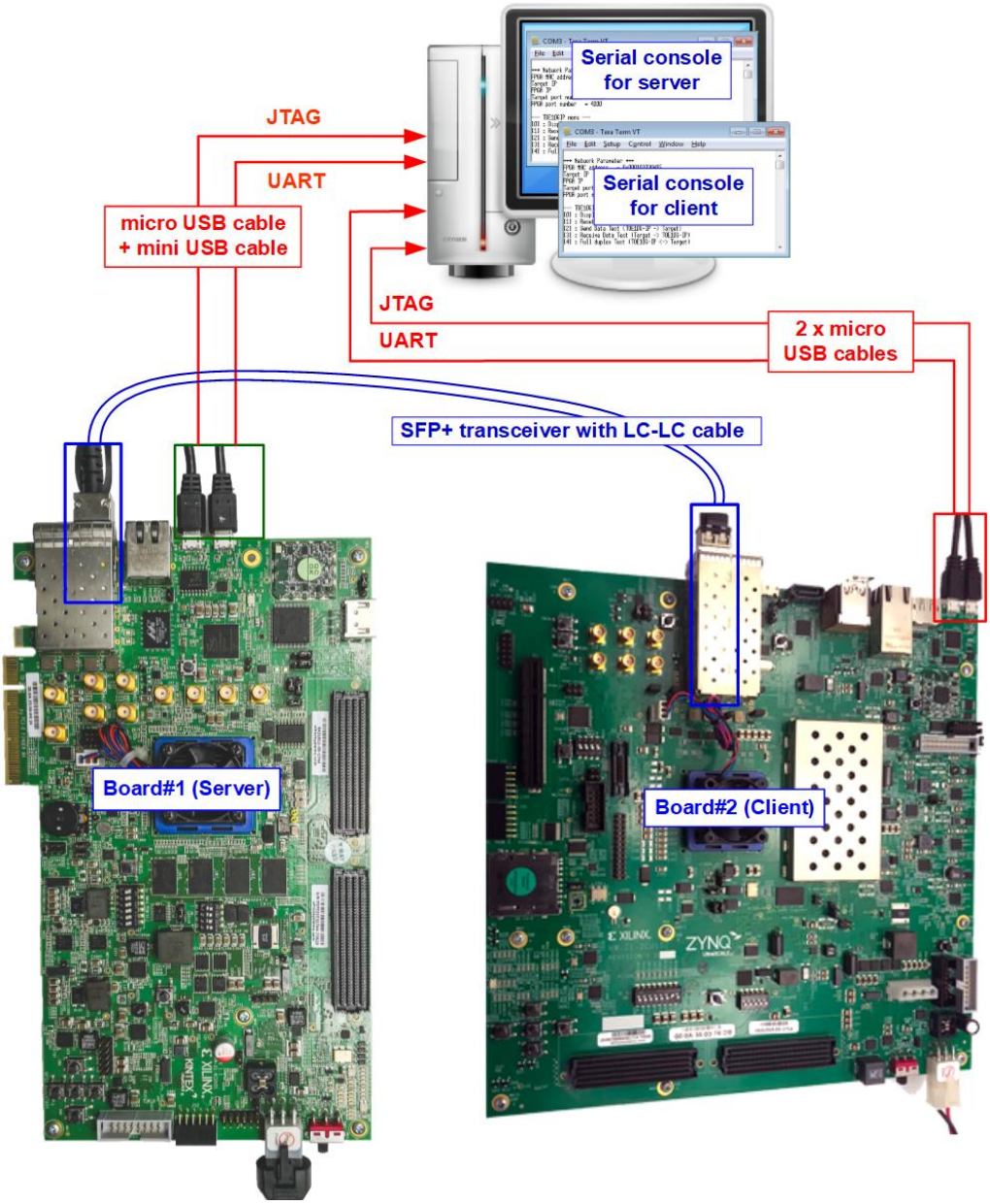

Figure 2-1 TOE10G-IP/UDP10G-IP with CPU demo (FPGA<->FPGA)

The step to setup test environment by using two FPGAs is described in more details as follows.

Follow step 1) – 8) of topic 1 (Test environment setup when using FPGA and PC) to prepare FPGA board and SFP+ connection for running the demo. After two FPGA boards have been configured completely, Serial console displays the menu to select client mode or server mode. The step after FPGA configuration is described as follows.

1) Open Serial console for board#1 and board#2 which are set to initialize in server mode and client mode respectively.
   i) Set '1' on Serial console of FPGA board#1 for running server mode.
   ii) Set '0' on Serial console of FPGA board#2 for running client mode.
   iii) Default parameters for server or client are displayed on the console, as shown in Figure 2-2.

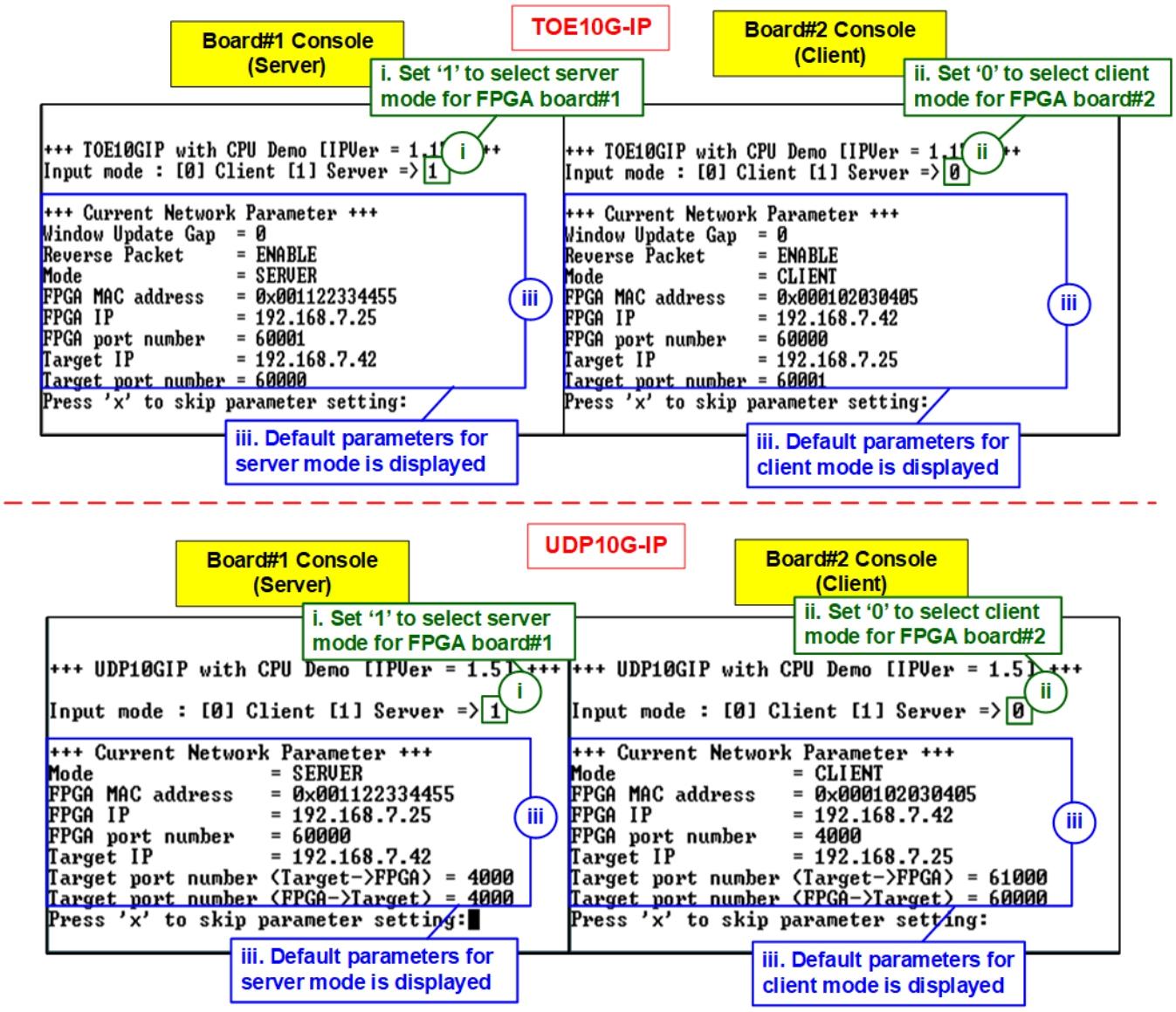

Figure 2-2 Input mode

2) Input 'x' to use default parameters or other keys to change parameters. The parameters of server mode must be set before client mode.

   When running TOE10G-IP,
   i) Set parameters on server Serial console.
   ii) Set parameters on client Serial console to start IP initialization by transferring ARP packet.
   iii) After finishing initialization process. "IP initialization complete" and main menu are displayed on server console and client console.

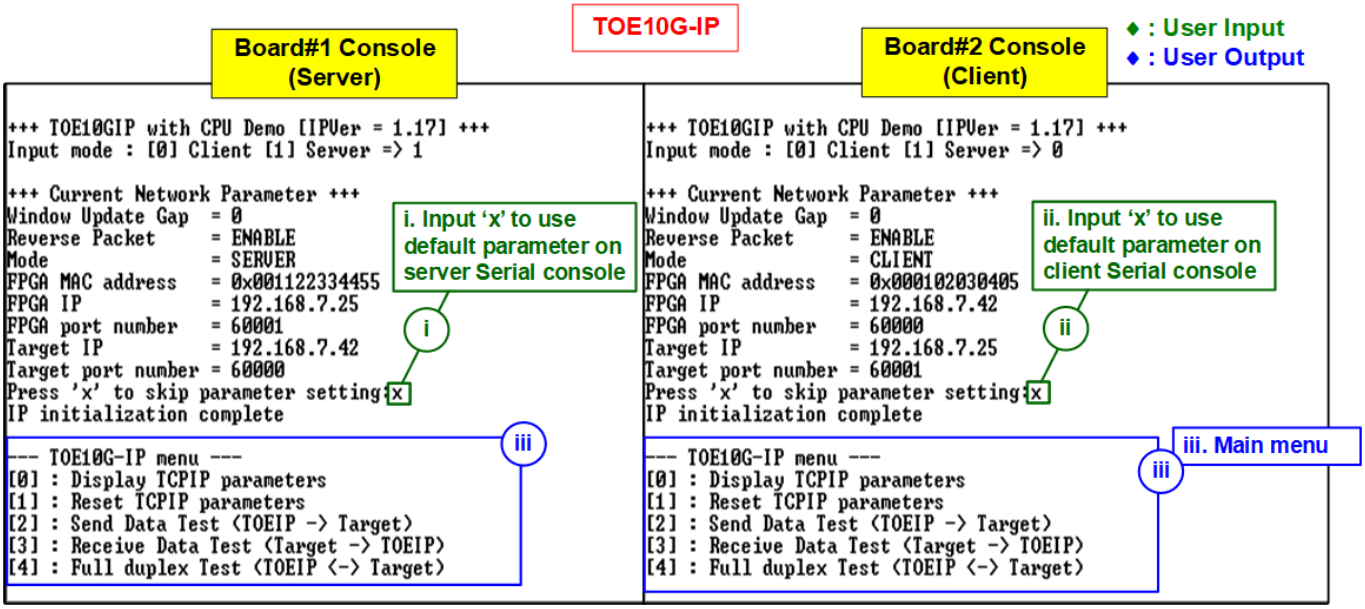

Figure 2-3 Main menu of TOE10G-IP

When running UDP10G-IP,

i) For server mode, if user does not change default parameters, input ‘x’ to skip parameter setting.

ii) For client mode, user must change target port number (Target->FPGA) to use same value as target port number (FPGA->Target).

iii) After finishing initialization process. “IP initialization complete” and main menu are displayed on server console and client console.

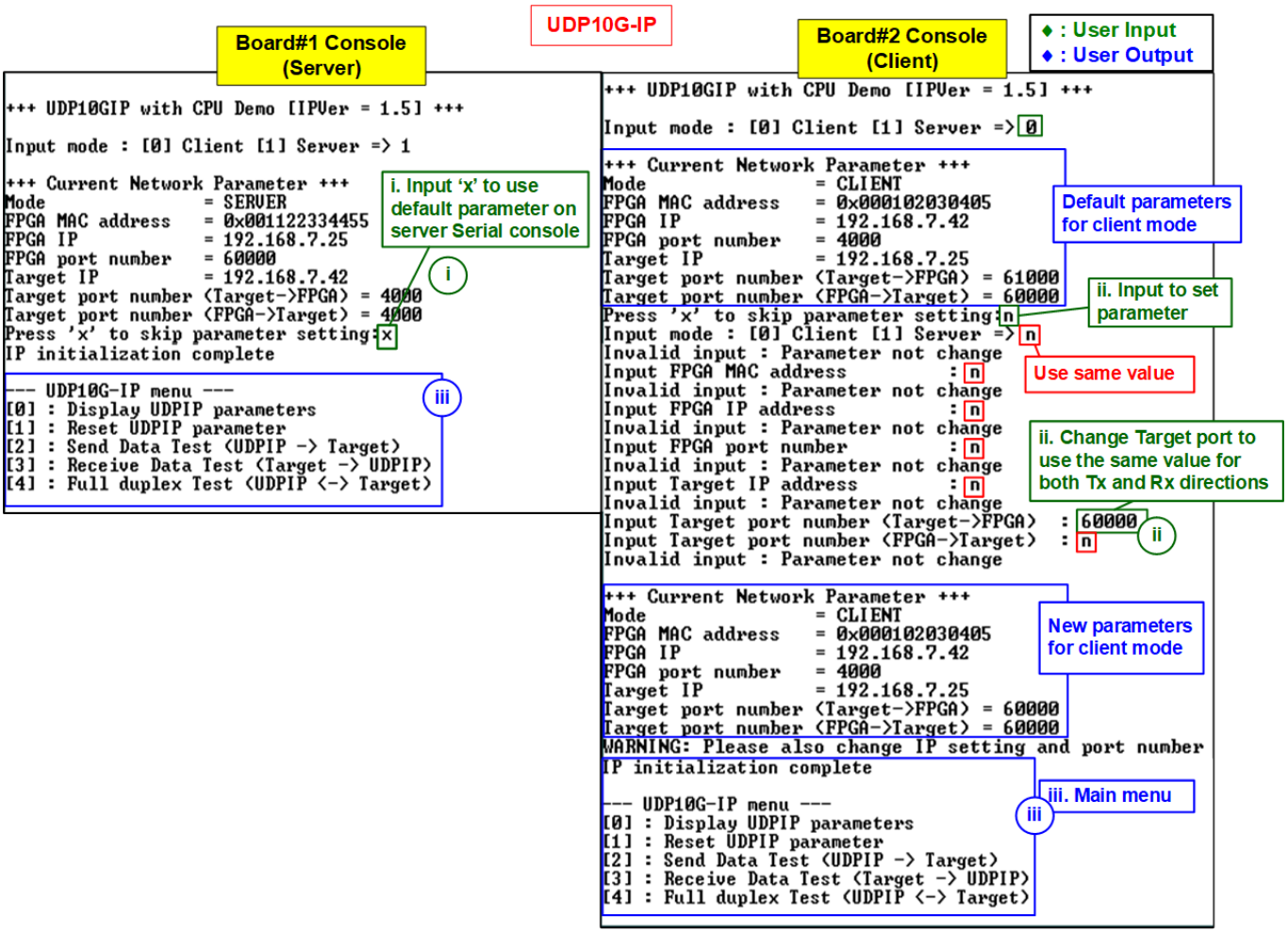

Figure 2-4 Main menu of UDP10G-IP

3 Revision History

Revision	Date	Description
1.0	15-Sep-17	Initial version release
1.1	8-Mar-19	Support FPGA <-> FPGA test and ZCU102
2.0	21-Jul-20	Remove test result on the console
3.0	21-Aug-20	TOE10G-IP and UDP10G-IP
3.1	15-Mar-22	Update Figure 1-14, Figure 2-2, and Figure 2-3