

UDP-IP Demo Instruction

Rev1.0 6-Jan-16

This document describes the instruction to run UDP-IP for transferring data between FPGA development board and PC through Gigabit Ethernet.

1 Environment Setup

As shown in Figure 1-1, to run UDP-IP demo, please prepare

- 1) FPGA Development board (AC701)
- 2) iMPACT ver 14.4 or later
- 3) Ethernet cable (Cat5e or Cat6) for network connection between FPGA Development board and PC
- 4) PC with Gigabit Ethernet support
- 5) micro USB cable for programming FPGA connecting between FPGA Development board and PC
- 6) "send_udp_client.exe" and "recv_udp_client.exe", provided by Design Gateway, which are test application on Windows PC

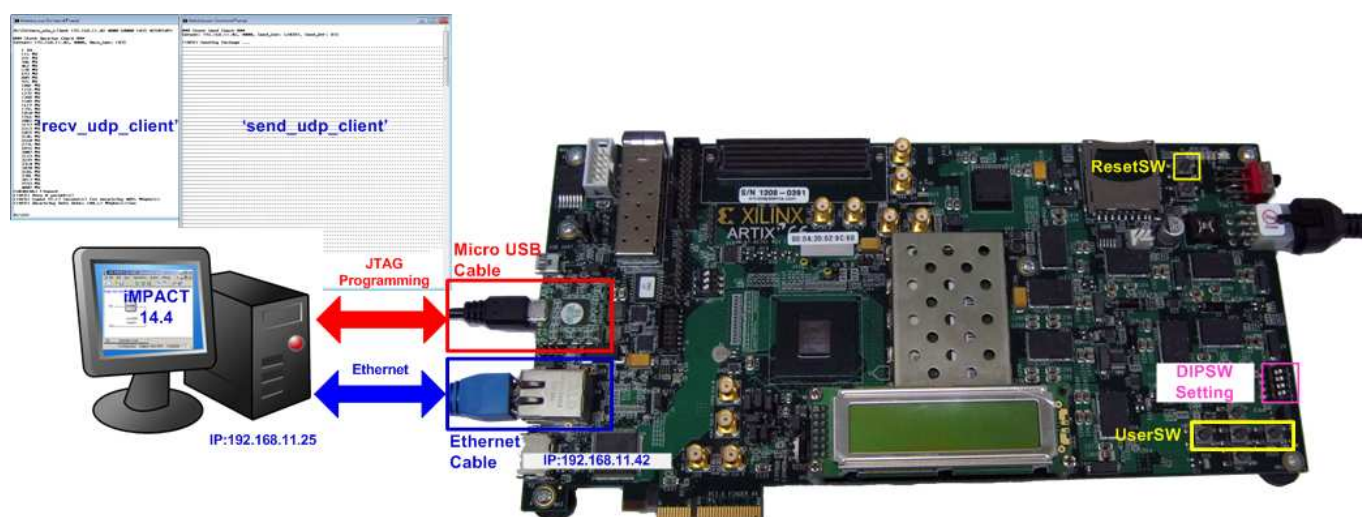


Figure 1-1 UDP-IP Demo Environment Setup on AC701

2 Demo description

The demo is designed by pure-hardware logic, so DIPSWs, push buttons, and LEDs are used to be user inputs and outputs on FPGA board.

2.1 DIPSW

Bit1 and bit3 of DIPSW are used to set packet size for IP sending data and enable data verification for IP receiving data, like TOE2-IP demo. More details are described in Table 2-1.

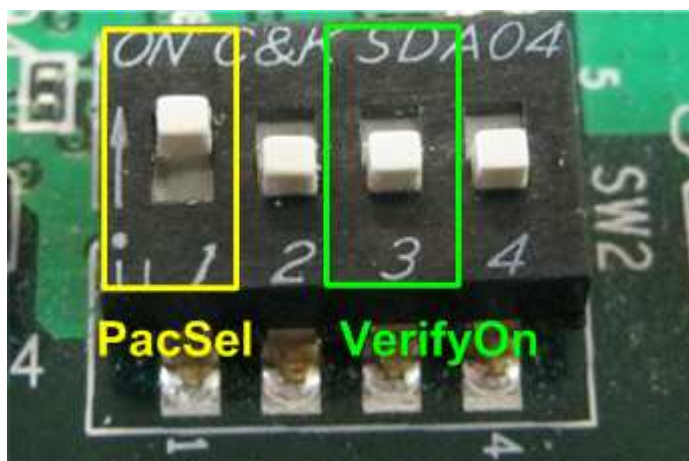


Figure 2-1 DIPSW setting in the demo

DIPSW	OFF	ON
Bit 1	Sending mode by using non-Jumbo frame (1472 bytes)	Sending mode by using Jumbo frame (8972 bytes)
Bit 3	Receiving mode without data verification	Receiving mode with data verification

Table 2-1 DIPSW setting definition

2.2 LED

4 LEDs are used to show operation status of the demo such as IP in initialization, sending data, receiving data. More details of each LED description are shown in Table 2-2.

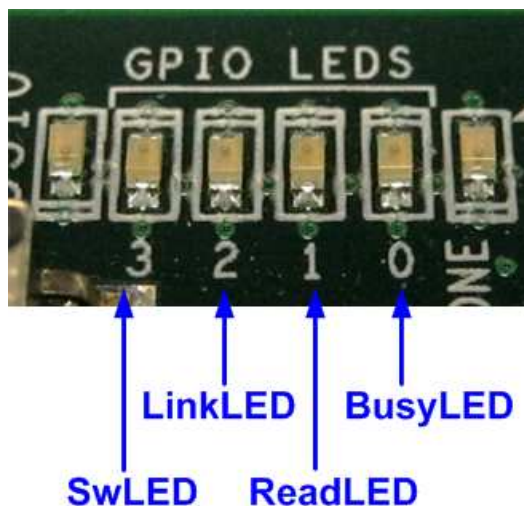


Figure 2-2 LED setting in the demo

LED	ON	OFF	BLINK
0	IP is busy from initialization or sending data.	IP is in Idle condition.	IP interrupt is found.
1	IP receives data.	No received data available in IP.	Data verification is failed.
2	Sending mode in Jumbo frame.	Sending mode in non-jumbo frame	Ethernet is not link-up. Please check Ethernet cable.
3	User presses one of three push buttons.	No push button is pressed.	N/A

Table 2-2 LED Definition

2.3 Push button

Three push buttons are used in the demo, i.e. West, Center, and East SW, as shown in Figure 2-3. The button is used to start IP initialization, data sending, and reset pattern verification. More details of each button are described as follows.

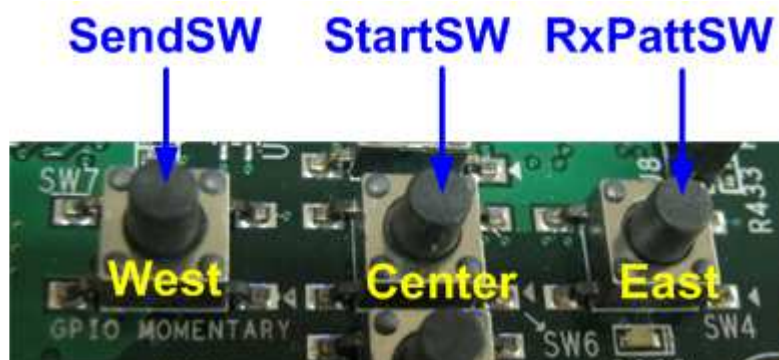


Figure 2-3 Push button setting in the demo

- StartSW (Center): After power-on system, user needs to press this SW to start IP initialization. User can start data sending or receiving test only after complete IP initialization.
- SendSW (West): Press this SW to start IP sending data to PC. Please confirm that BusyLED is OFF before pressing this SW.
- RxPattSW (East): Press this SW to reset start value of test pattern within data verification module. So, user needs to press this SW before re-run IP receiving data test with enable data verification.

Note:

- DIPSW setting must not be changed during operation.
- Before pressing StartSW, please confirm that LinkLED is not blinked to wait Ethernet PHY ready.
- Before pressing SendSW, please confirm that IP is in Idle state by monitoring BusyLED status.

3 PC Setup

Similar to TOE2-IP, please confirm network setting on TestPC that is correct setting before running the demo.

3.1 IP Setting

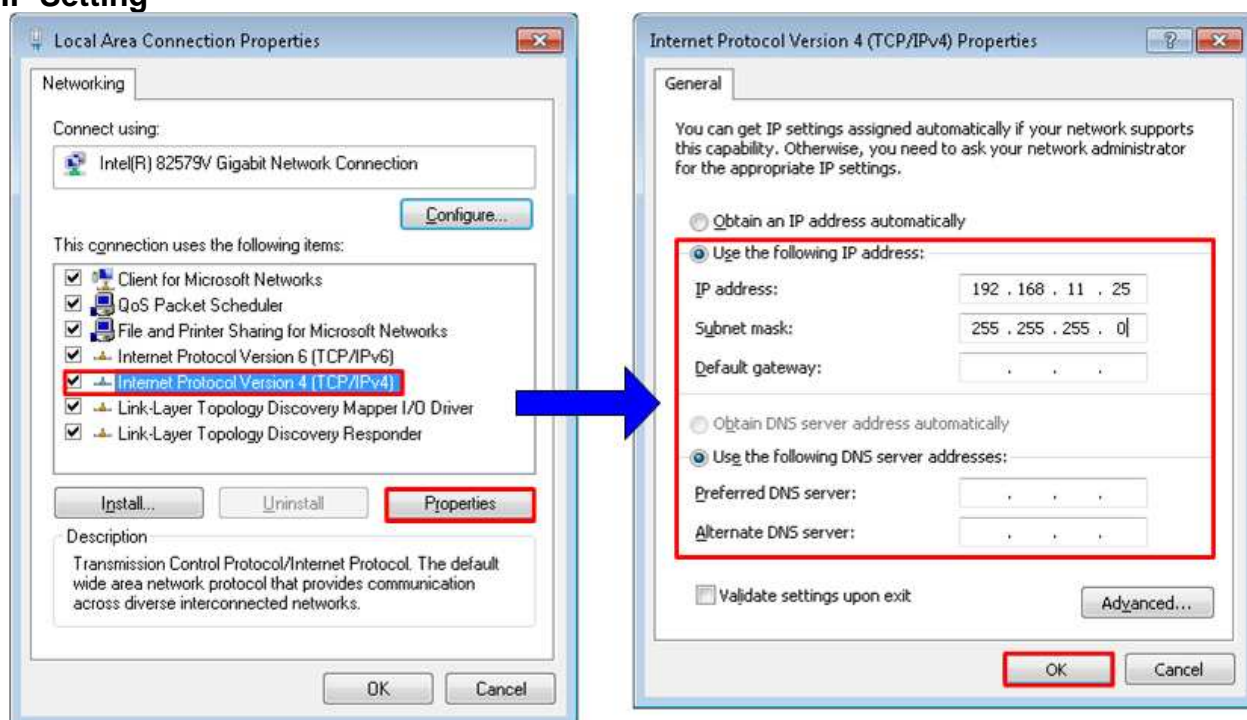


Figure 3-1 IPv4 Setting

- Open Local Area Connection Properties of Ethernet test connection, as shown in left window of Figure 3-1.
- Select "TCP/IPv4" and then click Properties.
- Set IP address = 192.168.11.25, and Subnet mask = 255.255.255.0, as shown in right window of Figure 3-1.

3.2 Speed and Frame Setting

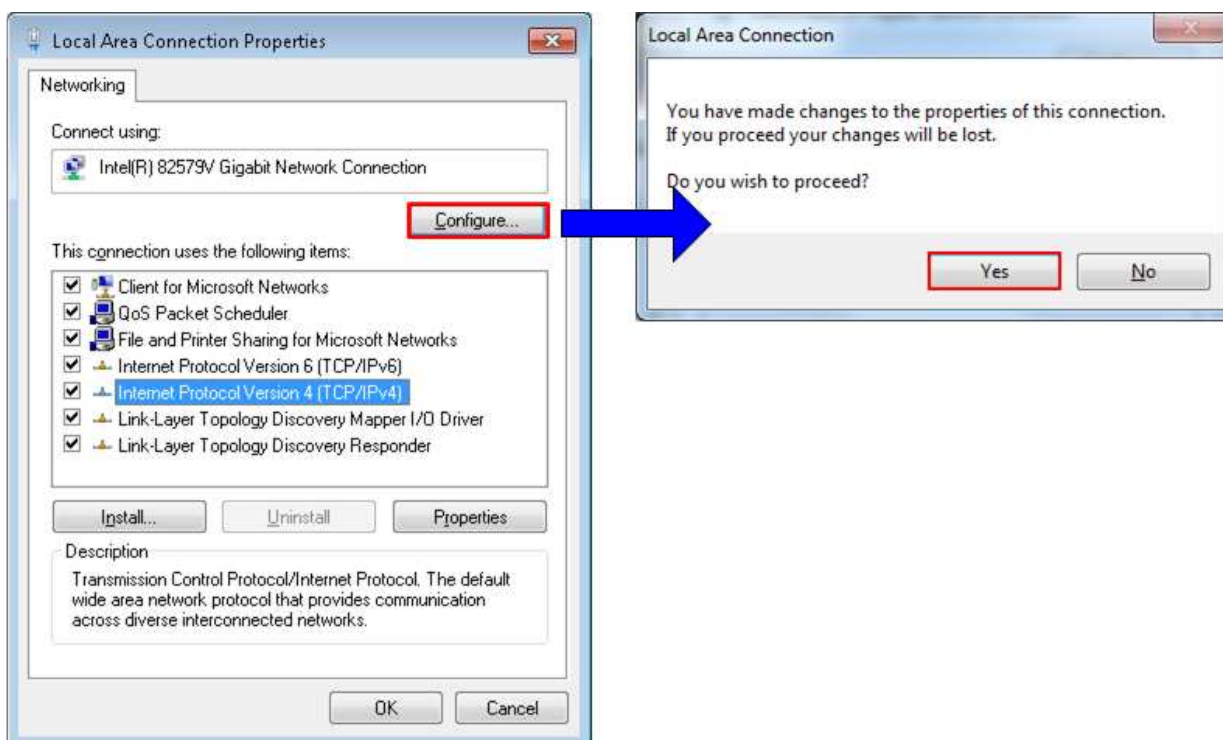


Figure 3-2 Network Configure

- On Local Area Connection Properties window, click “Configure”, as shown in Figure 3-2.
- On Advance tab, Jumbo Packet = 9014 Bytes to enable jumbo frame, as shown in Figure 3-3.

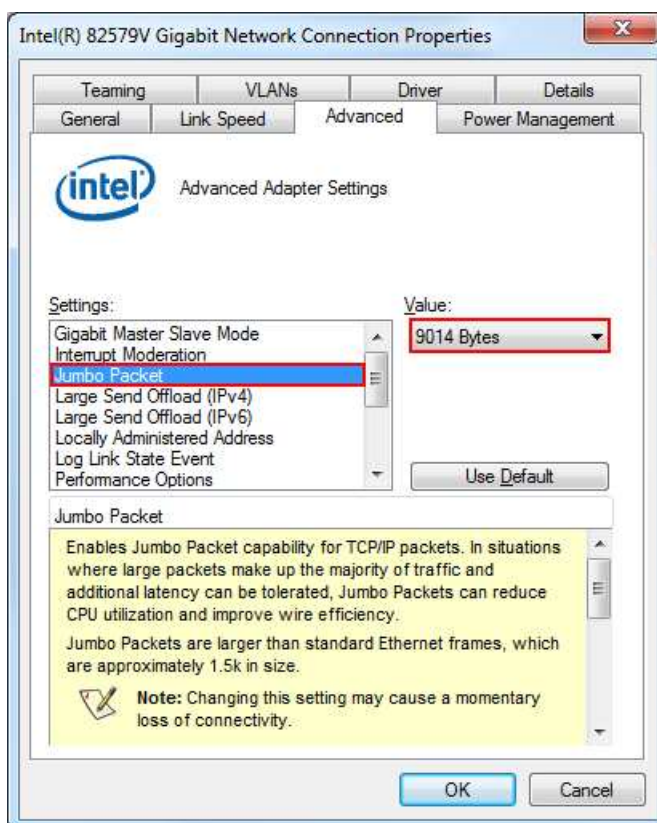


Figure 3-3 Jumbo Frame Setting

- On Link Speed tab, select “1.0 Gbps Full Duplex” for running Gigabit transfer test, as shown in left window of Figure 3-4.
- On Advance tab, Settings=Interrupt Moderation and Value= “Enabled”, as shown in right window of Figure 3-4.

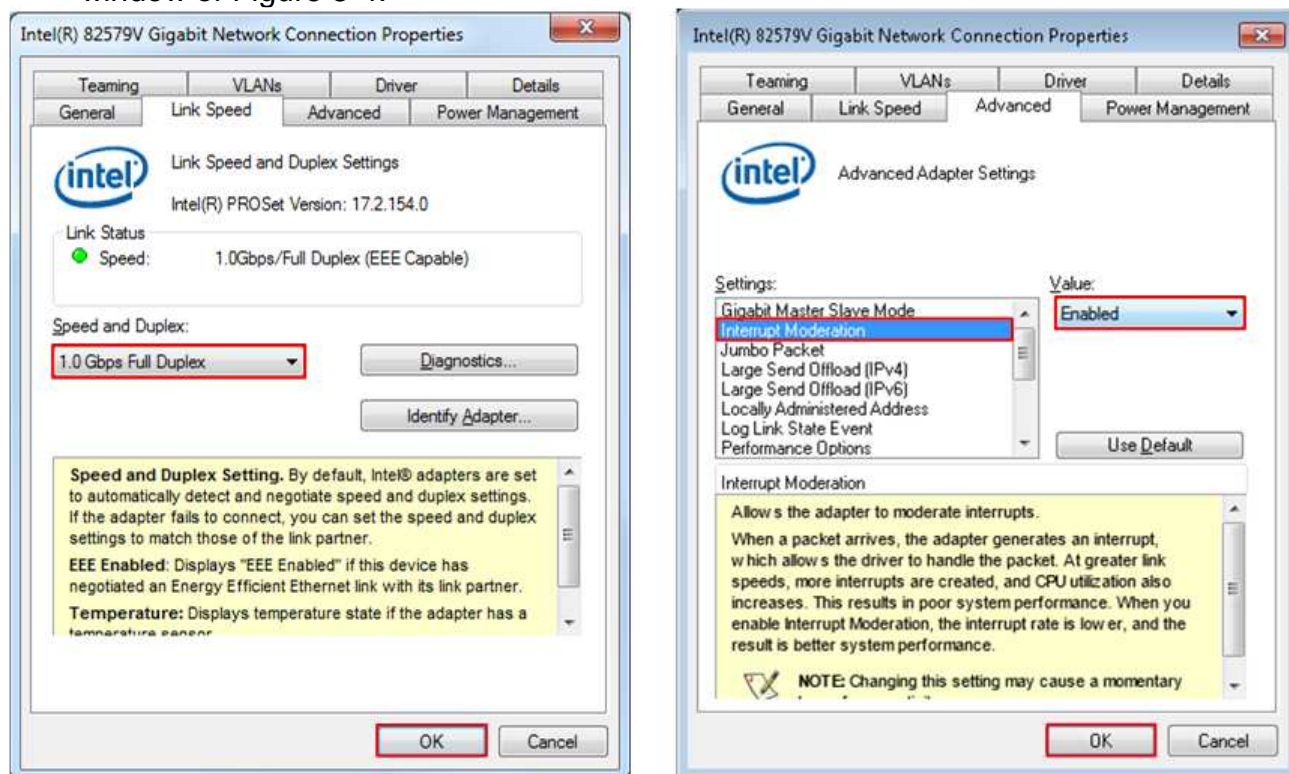


Figure 3-4 Link speed and Jumbo frame setup

- For Intel LAN controller, Performance Options in “Advanced” tab should be set for better performance as shown in Figure 3-5. “Interrupt Moderation Rate” in “Performance Options” windows must be set to “Off”.

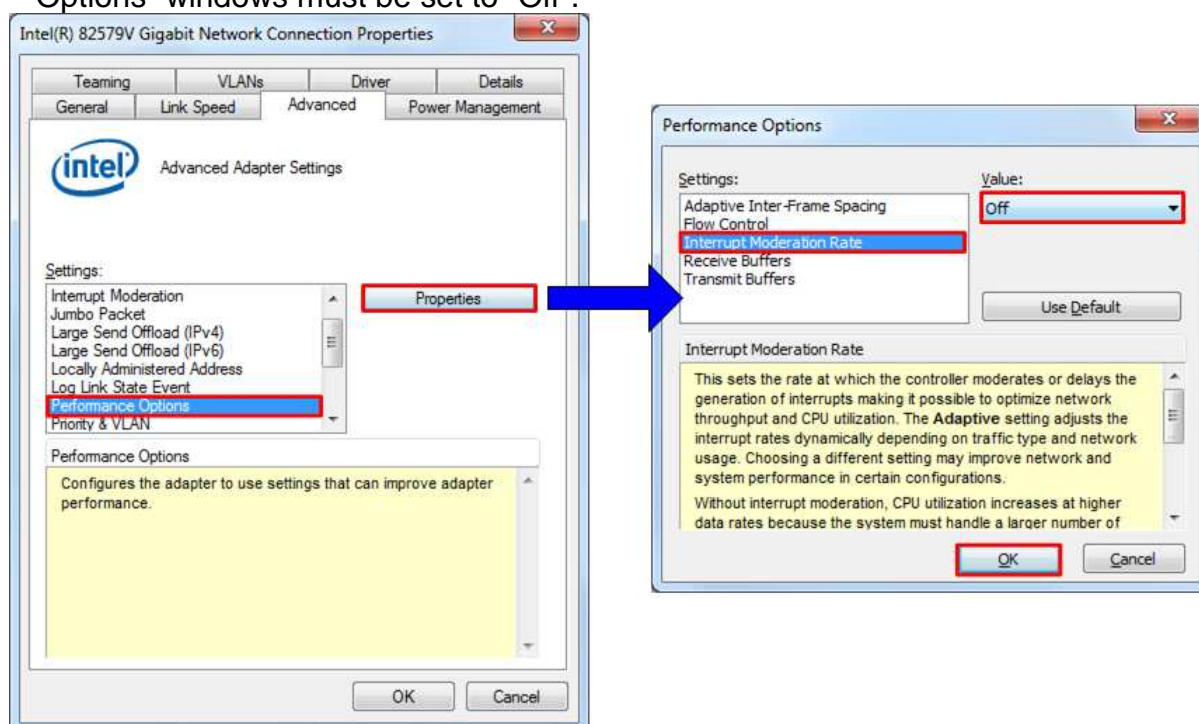


Figure 3-5 Enable Interrupt Moderation

4 How to run demo

4.1 Initialization

Before running IP sending and receiving data test, please follow below steps to setup and initialize test system.

- Connect micro USB cable from FPGA development board to PC and connect power supply to FPGA board.
- Connect Ethernet cable between FPGA development board and PC.
- Set up network setting on PC, following Topic 3.
- Power on FPGA development board.
- Open iMPACT and download “udpiptest_ac701.bit” to FPGA development board, as shown in Figure 4-1.

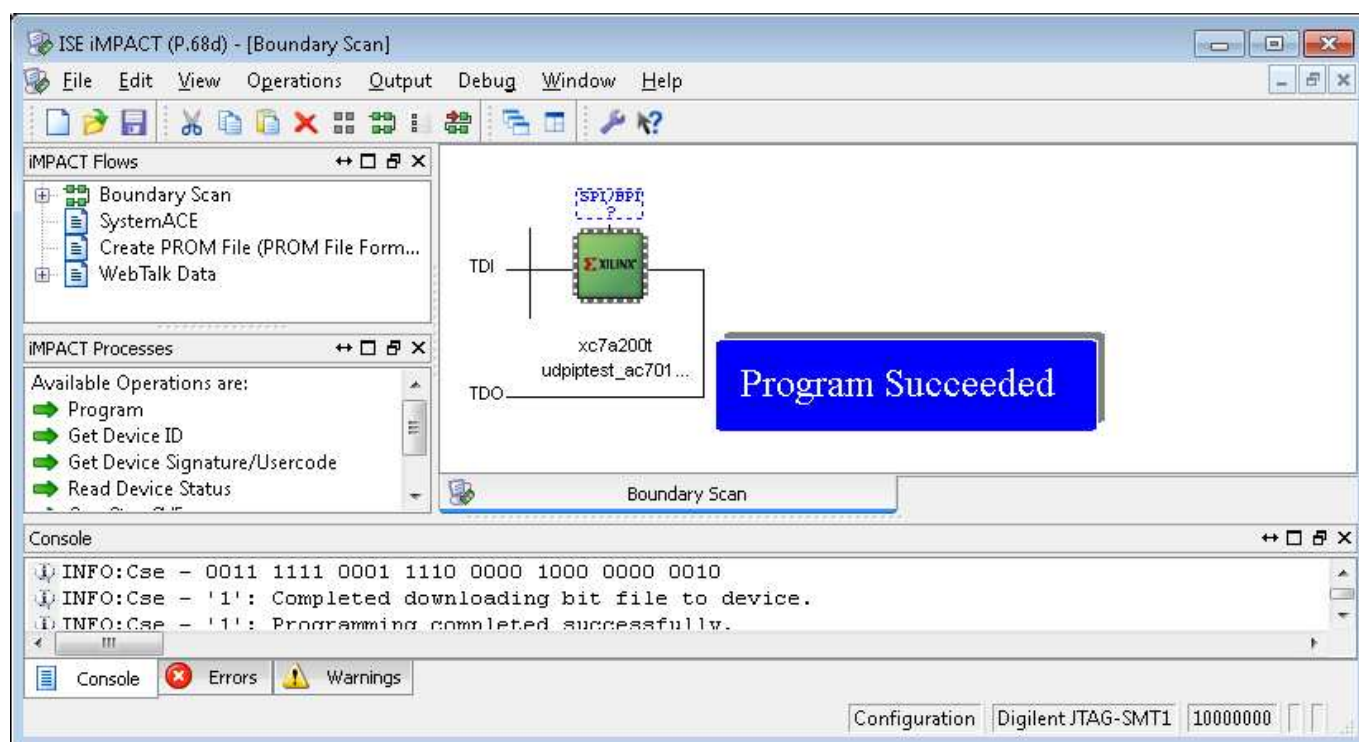


Figure 4-1 Programmer Environment

- Monitor LED2 status on FPGA development board that should change from BLINK to be ON/OFF status following DIPSW1 setting.
Note: If LED2 still be BLINK, please check Ethernet cable connection between FPGA and PC.



Blink -> ON/OFF

Figure 4-2 LED status after programming bit file and ethernet can linkup

- Press StartSW at Center-SW to start IP initialization process. LED0 will change from ON to OFF after IP initialization complete, as shown in Figure 4-3.
Note: If LED0 is not ON and change to BLINK status instead, please check that IP address on PC is correct or Ethernet cable is in good status.
To re-initialize system, user needs to press CPU RESET button, wait until LED2 changing from BLINK to ON/OFF, and press StartSW again.



ON -> OFF

Figure 4-3 LED status after press StartSW and IP initialization complete

Now system is ready to run IP sending data and receiving data. More details are described in the next topic.

Note: Transfer performance on the demo depends on Test PC specification.

4.2 IP Sending Data Test

Hardware logic designs to support two different packet sizes to show performance when running non-jumbo frame and jumbo frame size. Hardware setting and parameter input of test application should be matched. More details about each mode are described as follows.

4.2.1 Non-Jumbo frame mode

- Set DIPSW[1] = OFF and confirm that LED2 status is OFF.
- Open "command prompt" on PC, and run "recv_udp_client" test application by using command as shown in Figure 4-4.

Note: This demo fixes IP address, port number, and received size. So, please do not change any value without HDL code modification.

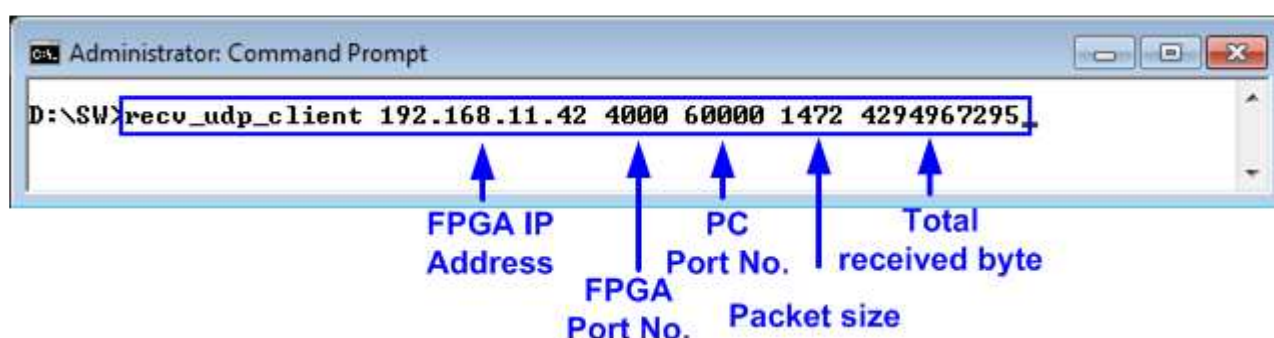


Figure 4-4 "recv_udp_client" command with non-jumbo frame

- Confirm that IP is in Idle condition by monitoring LED0 = OFF. Then, press SendSW at West-SW to start data sending from FPGA.
- LED0 will change to ON status, as shown in Figure 4-5. LED0 will be OFF after all data are transferred completely.



OFF: OFF -> ON
Non-jumbo frame

Figure 4-5 LED status during running "recv_udp_client" with non-jumbo frame

- During receiving data, test application will display total received byte on the console every second. Finally, it will show total dropped packet, and performance as shown in Figure 4-6.
Note: Total performance output from test application will include delay time from running "recv_udp_client" to pressing SendSW, so user should press SendSW immediately after running "recv_udp_client" for output performance accuracy.

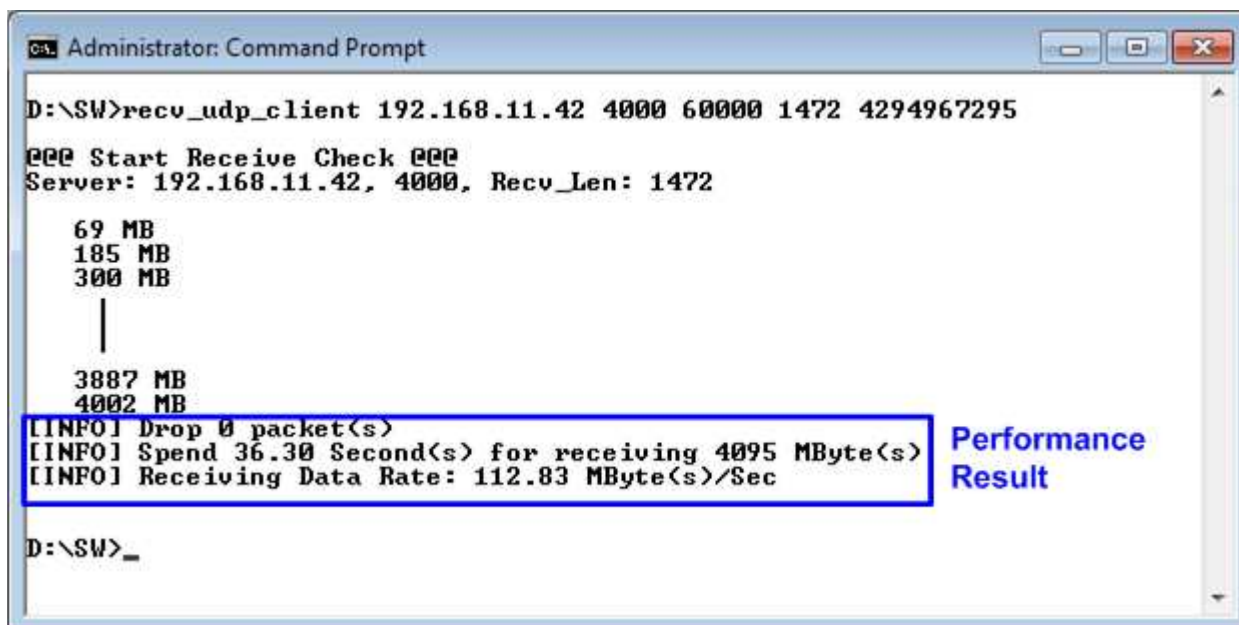


Figure 4-6 Output performance when running "recv_udp_client" with non-jumbo frame

- As shown in Figure 4-7, if packet dropped is found, "Drop Expect" message will be displayed on the console. Final result will show total dropped packet, and test application will be ended by 0.5 sec timeout. "[WARNING] Timeout" message will be displayed when test application is exit from timeout condition.

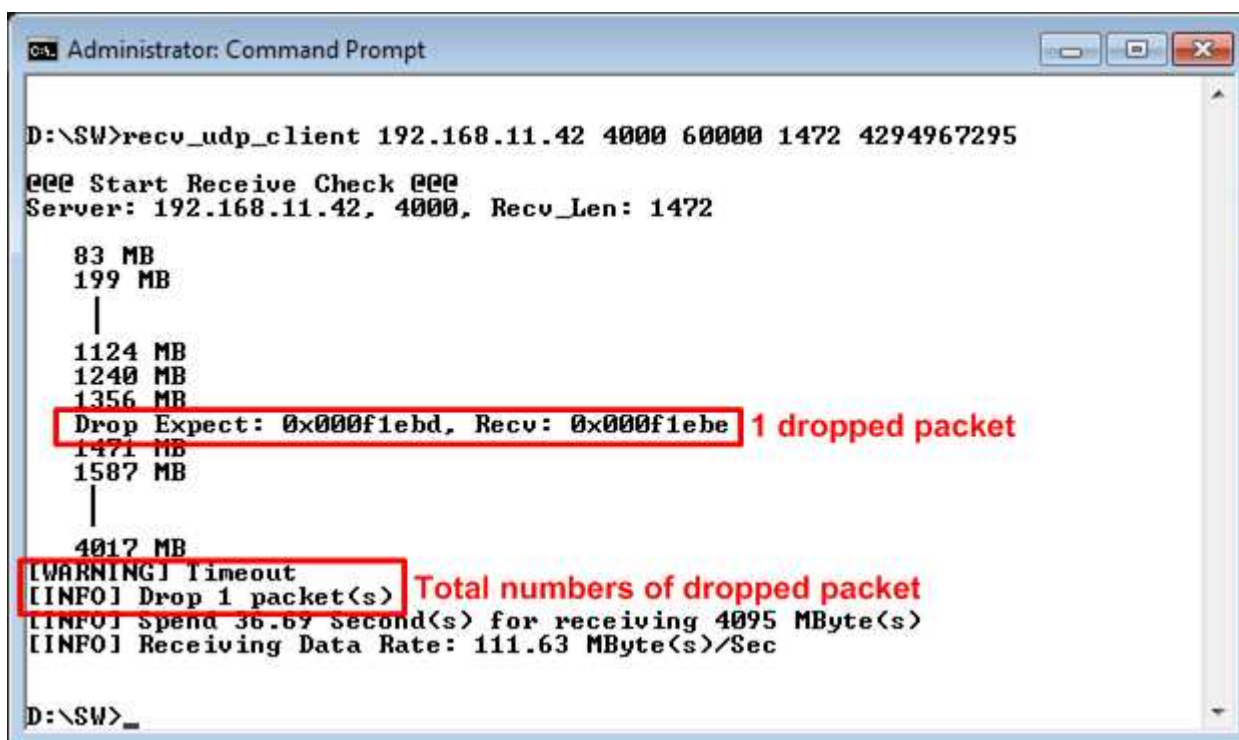


Figure 4-7 Warning message when packet dropped is found

4.2.2 Jumbo frame mode

- Set DIPSW[1] = ON and confirm that LED2 status is ON.
- Open "command prompt" on PC, and run "recv_udp_client" test application by using command as shown in Figure 4-8. Parameter inputs are same as non-jumbo frame except packet size which is set to 8972 instead of 1472.

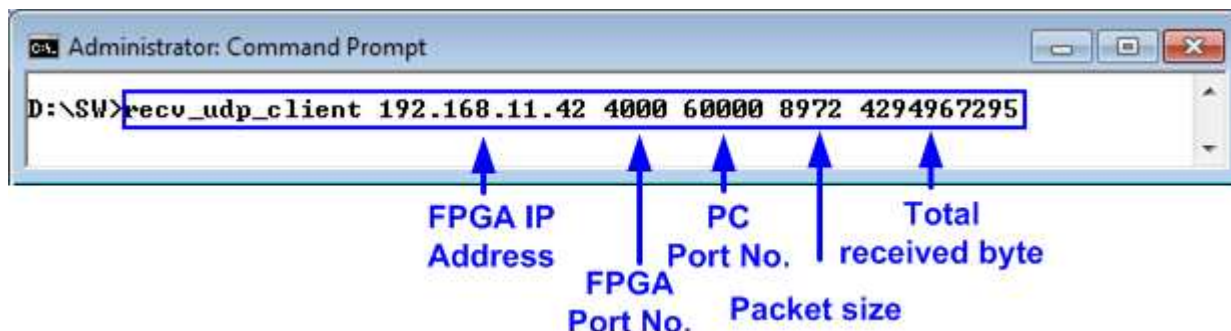


Figure 4-8 "recv_udp_client" command with jumbo frame

- Demo steps are same as non-jumbo frame mode. Please follow the step described in non-jumbo frame mode.
- As shown in Figure 4-10, test performance when using jumbo frame will be better than non-jumbo frame.



ON: OFF -> ON
Jumbo frame

Figure 4-9 LED status during running "recv_udp_client" with jumbo frame

```

Administrator: Command Prompt
D:\SW>recv_udp_client 192.168.11.42 4000 60000 8972 4294967295
@@@ Start Receive Check @@@
Server: 192.168.11.42, 4000, Recv_Len: 8972

 79 MB
199 MB
319 MB
|
3919 MB
4039 MB
[INFO] Drop 0 packet(s)
[INFO] Spend 34.94 Second(s) for receiving 4095 MByte(s)
[INFO] Receiving Data Rate: 117.22 MByte(s)/Sec
D:\SW>_
  
```

**Performance
Result**

Figure 4-10 Output performance when running "recv_udp_client" with jumbo frame

4.3 IP Receiving Data Test

Hardware logic designs to support enable/disable data verification module. Disable is used when test application sends dummy data to FPGA for higher performance. Enable is used when test application sends increment data to FPGA to check data valid. More details of each mode are described as follows.

4.3.1 Disable verification mode

- Set DIPSW[3] = OFF to disable data verification.
- Open "command prompt" on PC, and run "send_udp_client" test application by following command
 - >> send_udp_client <FPGA IP address> <FPGA port number> <PC port number> <numbers of 8kbyte packet > <mode>
 - o Similar to sending application, IP address and port number cannot change without HDL code modification.
 - o User can set numbers of 8kbyte packet which is valid from 1- 524287. Total transfer size will be calculated by numbers of packet x 8 x 1024 byte. So, maximum transfer size is 524287x8x1024 byte
 - o Mode: '0'- All '0' pattern are sent for high performance.

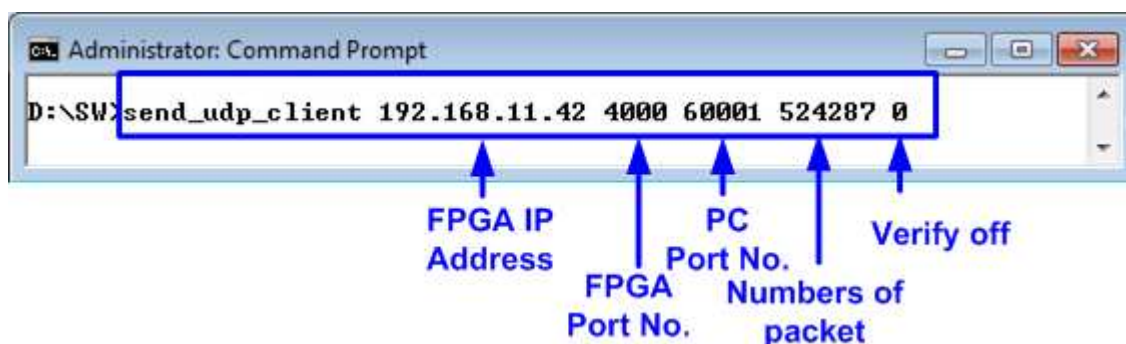


Figure 4-11 Example "send_udp_client" command when disable verification

- After running test application, LED[1] status will change from OFF to ON as shown in Figure 4-12.

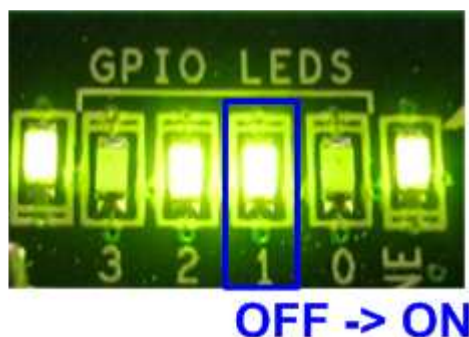


Figure 4-12 LED status during running "send_udp_client"

- Test application displays “...” during transferring packet. Time usage with performance will be displayed when complete data transfer, as shown in Figure 4-13.

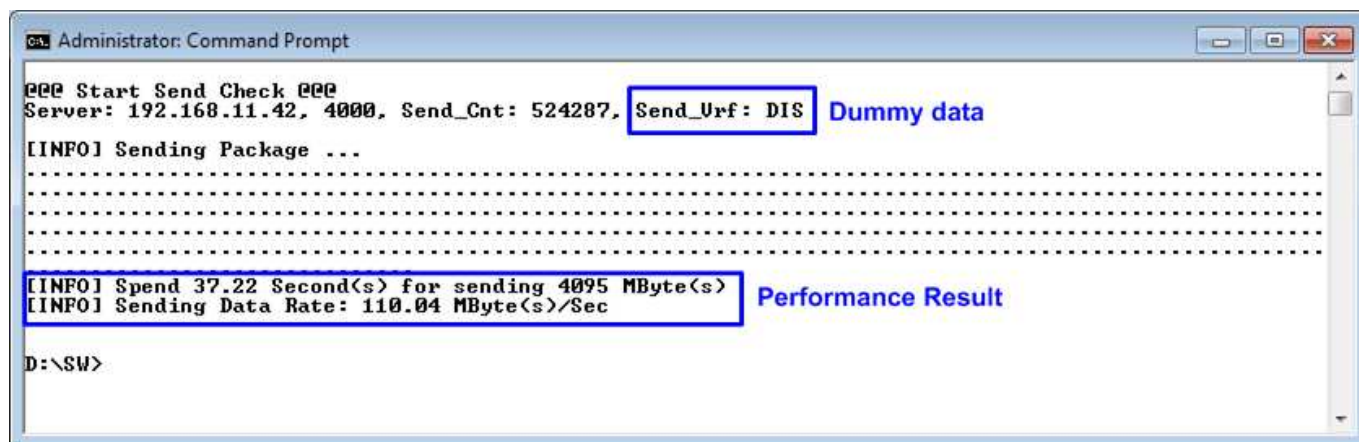


Figure 4-13 Test performance of “send_udp_client” when disable verification

4.3.2 Enable Verification mode

- Set DIPSW[3] = ON to enable data verification.
- Press RxPattSW at West-SW to reset test pattern for data verification.
- Open “command prompt” on PC, and run “send_udp_client” test application by setting mode = 1 to generate 32-bit increment data. The example command is shown in Figure 4-14.

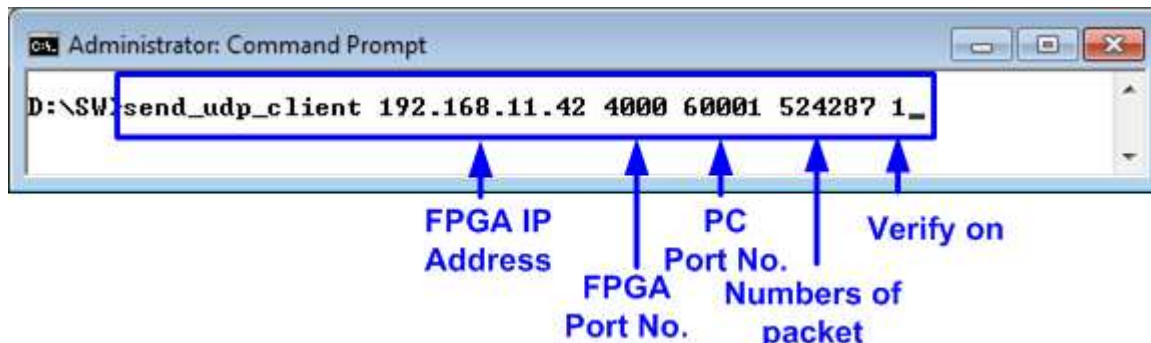


Figure 4-14 Example "send_udp_client" command when enable verification

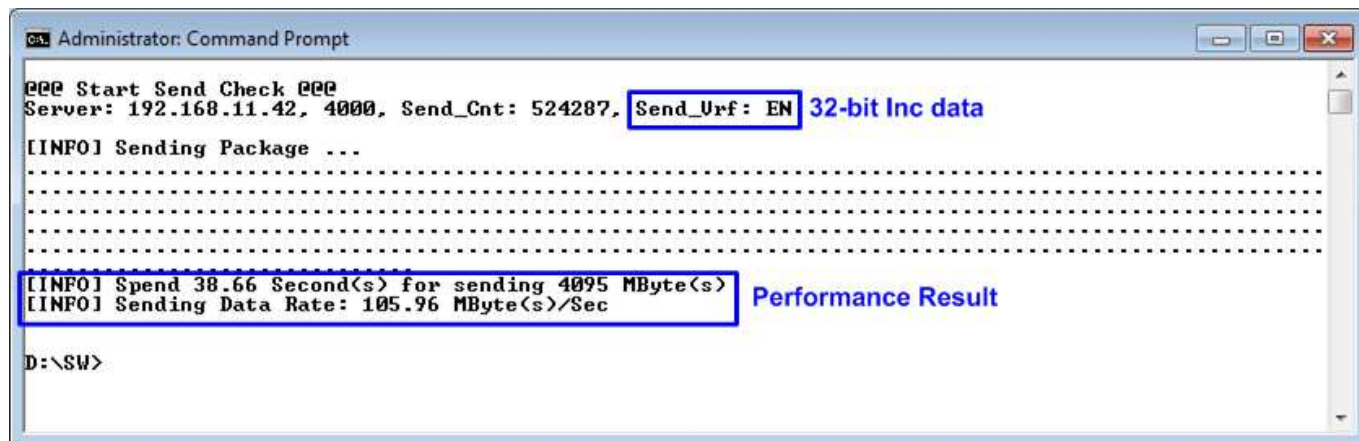


Figure 4-15 Test performance of “send_udp_client” when enable verification

- LED2 will blink if any error data is detected from Verification module.

4.4 Run two applications

In the demo, sending and receiving data test use different port number on PC, so user can run both tests at the same time. When running two applications at the same time, it will take much resource on PC. So, performance may be reduced for receiving data test and packet dropped may be much found for sending data test.

The example command and LED status during run both tests at the same time are shown in Figure 4-16 and Figure 4-17.

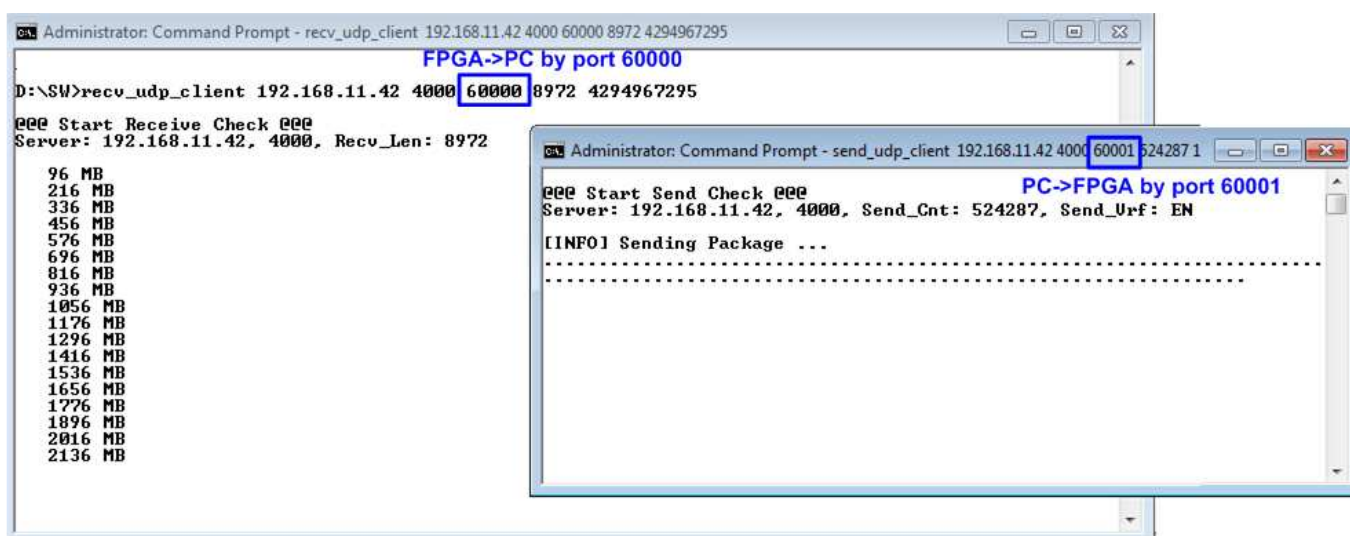


Figure 4-16 Run recv_udp_client and send_udp_client at the same time



OFF -> ON OFF -> ON

Figure 4-17 LED status when run both tests at the same time

5 Revision History

Revision	Date	Description
1.0	6-Jan-16	Initial version release