

SDLink User Manual [Ver 2.1]

Introduction

Thank you very much for purchasing SDLink (SL). This SL is a configuration module for SRAM based FPGA from Intel or Xilinx products. microSD Card is used to be configuration ROM space for SL.

This SL can be inserted into 2 rows x 10-Pin socket or soldered directly on the user circuit board. These pins are connected to configured signal of up to 8 FPGAs in Passive-Serial mode (PS) for Intel devices or Slave-Serial mode (SS) for Xilinx devices. This SL also supports 1-FPGA in Fast Passive-Parallel (FPP) for Intel or Slave-Parallel (SelectMAP8) for Xilinx devices. To program and/or verify data on microSD Card, microSD Card must be moved from SL to card reader for connecting with Host-PC. Then, exclusive software will be used to transfer data between Host-PC and microSD Card.

Reference documents

Please refer to the technical document listed below when user board is designed for SL.

Doc No	Document Name
SL-AN01	User board design for SDLink
SL-DS	SDLink data sheet

Documents can be downloaded from URL below.
https://dqway.com/SDLink_E.html

Notice of the application

Please observe the following notices.

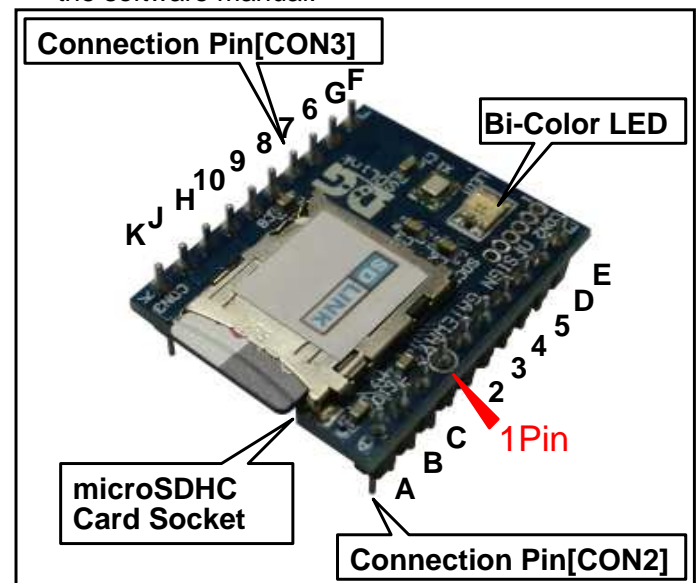
- [1] Do not remove microSD Card from SL while configuration is in progress (LED status: Orange Blinking).
- [2] The maximum voltage of the power supply to SL is +3.3V (+/-10%). **If the voltage is +5V, SL will be damaged.**
- [3] When insert new microSD Card to Host-PC and run the exclusive software, **please be careful to select correct removable drive name because data in that drive will be overwritten by configuration data.**

Usage

1. Program / Verify operation

- [1] To program configuration data to microSD, exclusive software and its manual are necessary. So download them from the following URL.
 URL: https://dqway.com/SDLink_E.html

- [2] Insert microSD Card into the card reader connected to the Host-PC.
- [3] Run exclusive software and check that software recognizes card reader drive as removable drive.
- [4] To execute load or verify by the software, refer to the software manual.



[fig.1] SDLink Module outline

2. Connecting with User Board

Insert SL to the 20pin connector on the user board so that each 1PIN position is aligned. (See fig1.) Refer to the data sheet (SL-DS) for detail of each configuration pin assignment.

When user board is powered-up, SL automatically executes initial (power up) configuration to the FPGA device.

LED Lighting

The lighting of Bi-Color LED on SL is shown in table below.

Color	Configuration status
Green	Success (CONF_DONE/DONE=H)
Red	Failure (all retry times have been failed.)
Red Blink	microSD format is incorrect.
Orange	No SD Card or cannot recognize microSD
Orange Blink	Configuration is in progress
None	Power off

Specification

(Refer to Datasheet SL-DS for more detail.)

- Size: L28mm x W23mm x H12mm
- Weight: 10gram
- Supply Power Voltage:
 - microSD: +3.3V (+/-10%)
 - Configuration +1.8V, +2.5V, or +3.3V
- Current consumption (Typical data)
 - Configuration/programming state: 85mA
 - Idle state: 55mA
- User data capacity
 - Up to 2 GB microSD Card
 - (it depends on microSD capacity)
 - (System area requires 1MB reserve space)
- Configuration speed:
 - 1-4 PS/SS mode: 40/20/10/5Mbps
 - 5-8 PS/SS mode: 20/10/5/2.5Mbps
 - FPP/SP mode: 160/80/40/20Mbps
 - (1-4: Setting on file#1-4 at software)
- Delay settings (from microSD initialization finish)
 - 0ms – 2550ms delay in 10ms step before start configuration
- Configuration error retry function:
 - 0-15 retry count
- Supported devices:
 - Please refer “Support Device List” on website https://dgway.com/SDLink_E.html
- Supported configuration file type:
 - Intel Device: RBF file
 - Xilinx Device: BIT file, BIN file
- Programming environment:
 - Exclusive software+microSD Card reader
- Attached part:
 - 1 SDHC microSD (4GB or more)

Exemption from responsibility

Notwithstanding any damages that any devices or parts on user board might incur for any reason whatsoever, Design Gateway Co.,Ltd. shall be exempted from any responsibility for the above damage. Any guarantee for any functional, electrical, physical quality of SL is lapsed whenever any reconstruction is made to SL.

Design Gateway Co.,Ltd. shall also be exempted from any responsibility for any data corruption in the drive by the mis-operation of exclusive software use.

Inquiry

URL: <http://www.design-gateway.com>
<https://dgway.com>

Email: info@dgway.com

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